



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



### Analog Peripherals

- **10-Bit ADC (C8051F310/1/2/3/6 only)**
  - Up to 200 ksp/s
  - Up to 21, 17, or 13 external single-ended or differential inputs
  - VREF from external pin or V<sub>DD</sub>
  - Built-in temperature sensor
  - External conversion start input
- **Comparators**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source (Comparator0)
  - Low current (< 0.5 μA)

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-Chips, target pods, and sockets
- Complete development kit

### Supply Voltage 2.7 to 3.6 V

- Typical operating current: 5 mA at 25 MHz;  
11 μA at 32 kHz
- Typical stop mode current: 0.1 μA
- Temperature range: -40 to +85 °C

### High Speed 8051 μC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 1280 bytes internal data RAM (1024 + 256)
- 16 kB (C8051F310/1/6/7) or 8 kB (C8051F312/3/4/5) Flash; In-system programmable in 512-byte sectors

### Digital Peripherals

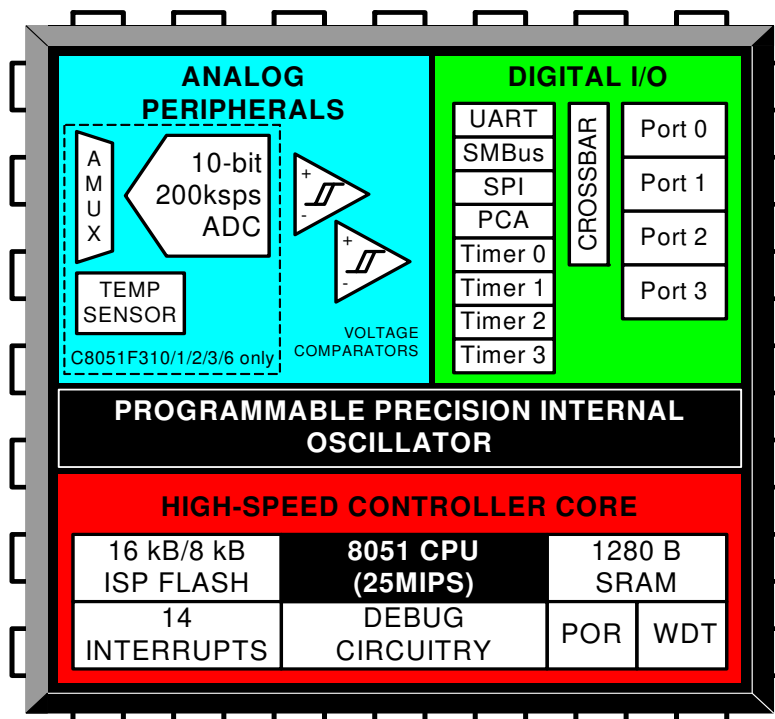
- 29/25/21 Port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART, SMBus™, and SPI™ serial ports
- Four general purpose 16-bit counter/timers
- 16-bit programmable counter array (PCA) with five capture/compare modules
- Real time clock capability using PCA or timer and external clock source

### Clock Sources

- Internal oscillator: 24.5 MHz with ±2% accuracy supports crystal-less UART operation
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly; useful in power saving modes

### Packages

- 32-pin LQFP (C8051F310/2/4)
- 28-pin QFN (C8051F311/3/5)
- 24-pin QFN (C8051F316/7)



# C8051F310/1/2/3/4/5/6/7

---

**NOTES:**

---

## Table Of Contents

<b>1. System Overview</b>	<b>17</b>
1.1. CIP-51™ Microcontroller Core	27
1.1.1. Fully 8051 Compatible	27
1.1.2. Improved Throughput	27
1.1.3. Additional Features	28
1.2. On-Chip Memory	29
1.3. On-Chip Debug Circuitry	30
1.4. Programmable Digital I/O and Crossbar	31
1.5. Serial Ports	32
1.6. Programmable Counter Array	32
1.7. 10-Bit Analog to Digital Converter	33
1.8. Comparators	34
<b>2. Absolute Maximum Ratings</b>	<b>35</b>
<b>3. Global DC Electrical Characteristics</b>	<b>36</b>
<b>4. Pinout and Package Definitions</b>	<b>39</b>
<b>5. 10-Bit ADC (ADC0, C8051F310/1/2/3/6 only)</b>	<b>51</b>
5.1. Analog Multiplexer	51
5.2. Temperature Sensor	52
5.3. Modes of Operation	54
5.3.1. Starting a Conversion	54
5.3.2. Tracking Modes	55
5.3.3. Settling Time Requirements	56
5.4. Programmable Window Detector	61
5.4.1. Window Detector In Single-Ended Mode	63
5.4.2. Window Detector In Differential Mode	64
<b>6. Voltage Reference (C8051F310/1/2/3/6 only)</b>	<b>67</b>
<b>7. Comparators</b>	<b>69</b>
<b>8. CIP-51 Microcontroller</b>	<b>79</b>
8.1. Instruction Set	80
8.1.1. Instruction and CPU Timing	80
8.1.2. MOVX Instruction and Program Memory	81
8.2. Memory Organization	85
8.2.1. Program Memory	85
8.2.2. Data Memory	86
8.2.3. General Purpose Registers	86
8.2.4. Bit Addressable Locations	86
8.2.5. Stack	86
8.2.6. Special Function Registers	87
8.2.7. Register Descriptions	90
8.3. Interrupt Handler	93
8.3.1. MCU Interrupt Sources and Vectors	94
8.3.2. External Interrupts	95
8.3.3. Interrupt Priorities	95

# C8051F310/1/2/3/4/5/6/7

---

8.3.4. Interrupt Latency .....	95
8.3.5. Interrupt Register Descriptions.....	97
8.4. Power Management Modes .....	102
8.4.1. Idle Mode.....	102
8.4.2. Stop Mode .....	103
<b>9. Reset Sources.....</b>	<b>105</b>
9.1. Power-On Reset .....	106
9.2. Power-Fail Reset / $V_{DD}$ Monitor.....	106
9.3. External Reset .....	107
9.4. Missing Clock Detector Reset.....	108
9.5. Comparator0 Reset.....	108
9.6. PCA Watchdog Timer Reset.....	108
9.7. Flash Error Reset.....	108
9.8. Software Reset .....	108
<b>10. Flash Memory .....</b>	<b>111</b>
10.1. Programming The Flash Memory .....	111
10.1.1. Flash Lock and Key Functions.....	111
10.1.2. Flash Erase Procedure .....	111
10.1.3. Flash Write Procedure .....	112
10.2. Non-volatile Data Storage .....	112
10.3. Security Options .....	113
10.4. Flash Write and Erase Guidelines .....	115
10.4.1. $V_{DD}$ Maintenance and the $V_{DD}$ Monitor .....	115
10.4.2. PSWE Maintenance .....	115
10.4.3. System Clock .....	116
<b>11. External RAM .....</b>	<b>119</b>
<b>12. Oscillators.....</b>	<b>121</b>
12.1. Programmable Internal Oscillator .....	121
12.2. External Oscillator Drive Circuit.....	124
12.3. System Clock Selection.....	124
12.4. External Crystal Example .....	126
12.5. External RC Example .....	127
12.6. External Capacitor Example .....	127
<b>13. Port Input/Output .....</b>	<b>129</b>
13.1. Priority Crossbar Decoder .....	131
13.2. Port I/O Initialization .....	133
13.3. General Purpose Port I/O .....	135
<b>14. SMBus .....</b>	<b>145</b>
14.1. Supporting Documents.....	146
14.2. SMBus Configuration.....	146
14.3. SMBus Operation .....	146
14.3.1. Arbitration.....	147
14.3.2. Clock Low Extension.....	148
14.3.3. SCL Low Timeout.....	148
14.3.4. SCL High (SMBus Free) Timeout .....	148

---

---

14.4.Using the SMBus.....	149
14.4.1.SMBus Configuration Register.....	150
14.4.2.SMB0CN Control Register .....	153
14.4.3.Data Register .....	156
14.5.SMBus Transfer Modes.....	157
14.5.1.Master Transmitter Mode .....	157
14.5.2.Master Receiver Mode .....	158
14.5.3.Slave Receiver Mode .....	159
14.5.4.Slave Transmitter Mode .....	160
14.6.SMBus Status Decoding.....	161
<b>15. UART0.....</b>	<b>163</b>
15.1.Enhanced Baud Rate Generation.....	164
15.2.Operational Modes .....	165
15.2.1.8-Bit UART .....	165
15.2.2.9-Bit UART .....	166
15.3.Multiprocessor Communications .....	167
<b>16. Enhanced Serial Peripheral Interface (SPI0).....</b>	<b>173</b>
16.1.Signal Descriptions.....	174
16.1.1.Master Out, Slave In (MOSI).....	174
16.1.2.Master In, Slave Out (MISO).....	174
16.1.3.Serial Clock (SCK) .....	174
16.1.4.Slave Select (NSS) .....	174
16.2.SPI0 Master Mode Operation .....	175
16.3.SPI0 Slave Mode Operation .....	177
16.4.SPI0 Interrupt Sources .....	177
16.5.Serial Clock Timing.....	178
16.6.SPI Special Function Registers .....	180
<b>17. Timers .....</b>	<b>187</b>
17.1.Timer 0 and Timer 1 .....	187
17.1.1.Mode 0: 13-bit Counter/Timer .....	187
17.1.2.Mode 1: 16-bit Counter/Timer .....	189
17.1.3.Mode 2: 8-bit Counter/Timer with Auto-Reload.....	189
17.1.4.Mode 3: Two 8-bit Counter/Timers (Timer 0 Only).....	190
17.2.Timer 2 .....	195
17.2.1.16-bit Timer with Auto-Reload.....	195
17.2.2.8-bit Timers with Auto-Reload.....	196
17.3.Timer 3 .....	199
17.3.1.16-bit Timer with Auto-Reload.....	199
17.3.2.8-bit Timers with Auto-Reload.....	200
<b>18. Programmable Counter Array .....</b>	<b>203</b>
18.1.PCA Counter/Timer .....	204
18.2.Capture/Compare Modules .....	205
18.2.1.Edge-triggered Capture Mode.....	206
18.2.2.Software Timer (Compare) Mode.....	207

---

# C8051F310/1/2/3/4/5/6/7

---

18.2.3.High-Speed Output Mode .....	208
18.2.4.Frequency Output Mode .....	209
18.2.5.8-Bit Pulse Width Modulator Mode.....	210
18.2.6.16-Bit Pulse Width Modulator Mode.....	211
18.3.Watchdog Timer Mode .....	212
18.3.1.Watchdog Timer Operation .....	212
18.3.2.Watchdog Timer Usage .....	213
18.4.Register Descriptions for PCA.....	215
<b>19. Revision Specific Behavior .....</b>	<b>221</b>
19.1.Revision Identification.....	221
19.2.Reset Behavior .....	221
19.2.1.Weak Pullups on <u>GPIO Pins</u> .....	221
19.2.2.V <sub>DD</sub> Monitor and the <u>RST</u> Pin .....	221
19.3.PCA Counter .....	222
<b>20. C2 Interface .....</b>	<b>223</b>
20.1.C2 Interface Registers.....	223
20.2.C2 Pin Sharing .....	225
<b>Document Change List.....</b>	<b>226</b>
<b>Contact Information.....</b>	<b>228</b>

---

## List of Figures

### 1. System Overview

Figure 1.1. C8051F310 Block Diagram .....	19
Figure 1.2. C8051F311 Block Diagram .....	20
Figure 1.3. C8051F312 Block Diagram .....	21
Figure 1.4. C8051F313 Block Diagram .....	22
Figure 1.5. C8051F314 Block Diagram .....	23
Figure 1.6. C8051F315 Block Diagram .....	24
Figure 1.7. C8051F316 Block Diagram .....	25
Figure 1.8. C8051F317 Block Diagram .....	26
Figure 1.9. Comparison of Peak MCU Execution Speeds .....	27
Figure 1.10. On-Chip Clock and Reset.....	28
Figure 1.11. On-Board Memory Map.....	29
Figure 1.12. Development/In-System Debug Diagram.....	30
Figure 1.13. Digital Crossbar Diagram .....	31
Figure 1.14. PCA Block Diagram.....	32
Figure 1.15. 10-Bit ADC Block Diagram.....	33
Figure 1.16. Comparator0 Block Diagram.....	34

### 2. Absolute Maximum Ratings

### 3. Global DC Electrical Characteristics

### 4. Pinout and Package Definitions

Figure 4.1. LQFP-32 Pinout Diagram (Top View) .....	41
Figure 4.2. LQFP-32 Package Diagram.....	42
Figure 4.3. QFN-28 Pinout Diagram (Top View) .....	43
Figure 4.4. QFN-28 Package Drawing .....	44
Figure 4.5. Typical QFN-28 Landing Diagram.....	45
Figure 4.6. QFN-28 Solder Paste Recommendation.....	46
Figure 4.7. QFN-24 Pinout Diagram (Top View) .....	47
Figure 4.8. QFN-24 Package Drawing .....	48
Figure 4.9. Typical QFN-24 Landing Diagram.....	49
Figure 4.10. QFN-24 Solder Paste Recommendation.....	50

### 5. 10-Bit ADC (ADC0, C8051F310/1/2/3/6 only)

Figure 5.1. ADC0 Functional Block Diagram.....	51
Figure 5.2. Typical Temperature Sensor Transfer Function.....	52
Figure 5.3. Temperature Sensor Error with 1-Point Calibration .....	53
Figure 5.4. 10-Bit ADC Track and Conversion Example Timing .....	55
Figure 5.5. ADC0 Equivalent Input Circuits.....	56
Figure 5.6. ADC Window Compare Example: Right-Justified Single-Ended Data ...	63
Figure 5.7. ADC Window Compare Example: Left-Justified Single-Ended Data .....	63
Figure 5.8. ADC Window Compare Example: Right-Justified Differential Data .....	64
Figure 5.9. ADC Window Compare Example: Left-Justified Differential Data .....	64

### 6. Voltage Reference (C8051F310/1/2/3/6 only)

Figure 6.1. Voltage Reference Functional Block Diagram .....	67
--	----



# C8051F310/1/2/3/4/5/6/7

---

<b>7. Comparators</b>	
Figure 7.1. Comparator0 Functional Block Diagram .....	69
Figure 7.2. Comparator1 Functional Block Diagram .....	70
Figure 7.3. Comparator Hysteresis Plot .....	71
<b>8. CIP-51 Microcontroller</b>	
Figure 8.1. CIP-51 Block Diagram.....	79
Figure 8.2. Memory Map .....	85
<b>9. Reset Sources</b>	
Figure 9.1. Reset Sources.....	105
Figure 9.2. Power-On and $V_{DD}$ Monitor Reset Timing .....	106
<b>10. Flash Memory</b>	
Figure 10.1. Flash Program Memory Map.....	113
<b>11. External RAM</b>	
<b>12. Oscillators</b>	
Figure 12.1. Oscillator Diagram.....	121
Figure 12.2. 32.768 kHz External Crystal Example.....	126
<b>13. Port Input/Output</b>	
Figure 13.1. Port I/O Functional Block Diagram .....	129
Figure 13.2. Port I/O Cell Block Diagram .....	130
Figure 13.3. Crossbar Priority Decoder with No Pins Skipped.....	131
Figure 13.4. Crossbar Priority Decoder with Crystal Pins Skipped .....	132
<b>14. SMBus</b>	
Figure 14.1. SMBus Block Diagram .....	145
Figure 14.2. Typical SMBus Configuration .....	146
Figure 14.3. SMBus Transaction .....	147
Figure 14.4. Typical SMBus SCL Generation.....	151
Figure 14.5. Typical Master Transmitter Sequence.....	157
Figure 14.6. Typical Master Receiver Sequence.....	158
Figure 14.7. Typical Slave Receiver Sequence.....	159
Figure 14.8. Typical Slave Transmitter Sequence.....	160
<b>15. UART0</b>	
Figure 15.1. UART0 Block Diagram .....	163
Figure 15.2. UART0 Baud Rate Logic .....	164
Figure 15.3. UART Interconnect Diagram .....	165
Figure 15.4. 8-Bit UART Timing Diagram.....	165
Figure 15.5. 9-Bit UART Timing Diagram.....	166
Figure 15.6. UART Multi-Processor Mode Interconnect Diagram .....	167
<b>16. Enhanced Serial Peripheral Interface (SPI0)</b>	
Figure 16.1. SPI Block Diagram .....	173
Figure 16.2. Multiple-Master Mode Connection Diagram .....	176
Figure 16.3. 3-Wire Single Master and Slave Mode Connection Diagram .....	176
Figure 16.4. 4-Wire Single Master and Slave Mode Connection Diagram .....	176
Figure 16.5. Master Mode Data/Clock Timing .....	178
Figure 16.6. Slave Mode Data/Clock Timing (CKPHA = 0) .....	179
Figure 16.7. Slave Mode Data/Clock Timing (CKPHA = 1) .....	179

---

---

Figure 16.8. SPI Master Timing (CKPHA = 0).....	183
Figure 16.9. SPI Master Timing (CKPHA = 1).....	183
Figure 16.10. SPI Slave Timing (CKPHA = 0).....	184
Figure 16.11. SPI Slave Timing (CKPHA = 1).....	184
<b>17. Timers</b>	
Figure 17.1. T0 Mode 0 Block Diagram.....	188
Figure 17.2. T0 Mode 2 Block Diagram.....	189
Figure 17.3. T0 Mode 3 Block Diagram.....	190
Figure 17.4. Timer 2 16-Bit Mode Block Diagram .....	195
Figure 17.5. Timer 2 8-Bit Mode Block Diagram .....	196
Figure 17.6. Timer 3 16-Bit Mode Block Diagram .....	199
Figure 17.7. Timer 3 8-Bit Mode Block Diagram .....	200
<b>18. Programmable Counter Array</b>	
Figure 18.1. PCA Block Diagram.....	203
Figure 18.2. PCA Counter/Timer Block Diagram.....	204
Figure 18.3. PCA Interrupt Block Diagram .....	205
Figure 18.4. PCA Capture Mode Diagram.....	206
Figure 18.5. PCA Software Timer Mode Diagram .....	207
Figure 18.6. PCA High Speed Output Mode Diagram.....	208
Figure 18.7. PCA Frequency Output Mode .....	209
Figure 18.8. PCA 8-Bit PWM Mode Diagram .....	210
Figure 18.9. PCA 16-Bit PWM Mode.....	211
Figure 18.10. PCA Module 4 with Watchdog Timer Enabled .....	212
<b>19. Revision Specific Behavior</b>	
Figure 19.1. Reading Package Marking .....	221
<b>20. C2 Interface</b>	
Figure 20.1. Typical C2 Pin Sharing.....	225

# C8051F310/1/2/3/4/5/6/7

---

NOTES:

---

## List of Tables

<b>1. System Overview</b>	
Table 1.1. Product Selection Guide .....	18
<b>2. Absolute Maximum Ratings</b>	
Table 2.1. Absolute Maximum Ratings .....	35
<b>3. Global DC Electrical Characteristics</b>	
Table 3.1. Global DC Electrical Characteristics .....	36
Table 3.2. Electrical Characteristics Quick Reference .....	38
<b>4. Pinout and Package Definitions</b>	
Table 4.1. Pin Definitions for the C8051F31x .....	39
Table 4.2. LQFP-32 Package Dimensions .....	42
Table 4.3. QFN-28 Package Dimensions .....	44
Table 4.4. QFN-24 Package Dimensions .....	48
<b>5. 10-Bit ADC (ADC0, C8051F310/1/2/3/6 only)</b>	
Table 5.1. ADC0 Electrical Characteristics .....	65
<b>6. Voltage Reference (C8051F310/1/2/3/6 only)</b>	
Table 6.1. External Voltage Reference Circuit Electrical Characteristics .....	68
<b>7. Comparators</b>	
Table 7.1. Comparator Electrical Characteristics .....	78
<b>8. CIP-51 Microcontroller</b>	
Table 8.1. CIP-51 Instruction Set Summary .....	81
Table 8.2. Special Function Register (SFR) Memory Map .....	87
Table 8.3. Special Function Registers .....	88
Table 8.4. Interrupt Summary .....	96
<b>9. Reset Sources</b>	
Table 9.1. Reset Electrical Characteristics .....	110
<b>10. Flash Memory</b>	
Table 10.1. Flash Electrical Characteristics .....	112
Table 10.2. Flash Security Summary .....	114
<b>11. External RAM</b>	
<b>12. Oscillators</b>	
Table 12.1. Internal Oscillator Electrical Characteristics .....	123
<b>13. Port Input/Output</b>	
Table 13.1. Port I/O DC Electrical Characteristics .....	143
<b>14. SMBus</b>	
Table 14.1. SMBus Clock Source Selection .....	150
Table 14.2. Minimum SDA Setup and Hold Times .....	151
Table 14.3. Sources for Hardware Changes to SMB0CN .....	155
Table 14.4. SMBus Status Decoding .....	161

# C8051F310/1/2/3/4/5/6/7

---

## 15. UART0

Table 15.1. Timer Settings for Standard Baud Rates Using the Internal Oscillator .....	170
Table 15.2. Timer Settings for Standard Baud Rates Using an External 25 MHz Oscillator .....	170
Table 15.3. Timer Settings for Standard Baud Rates Using an External 22.1184 MHz Oscillator .....	171
Table 15.4. Timer Settings for Standard Baud Rates Using an External 18.432 MHz Oscillator .....	171
Table 15.5. Timer Settings for Standard Baud Rates Using an External 11.0592 MHz Oscillator .....	172
Table 15.6. Timer Settings for Standard Baud Rates Using an External 3.6864 MHz Oscillator .....	172

## 16. Enhanced Serial Peripheral Interface (SPI0)

Table 16.1. SPI Slave Timing Parameters .....	185
---	-----

## 17. Timers

### 18. Programmable Counter Array

Table 18.1. PCA Timebase Input Options .....	204
Table 18.2. PCA0CPM Register Settings for PCA Capture/Compare Modules ....	205
Table 18.3. Watchdog Timer Timeout Intervals .....	214

## 19. Revision Specific Behavior

## 20. C2 Interface

## List of Registers

SFR Definition 5.1. AMX0P: AMUX0 Positive Channel Select .....	57
SFR Definition 5.2. AMX0N: AMUX0 Negative Channel Select .....	58
SFR Definition 5.3. ADC0CF: ADC0 Configuration .....	59
SFR Definition 5.4. ADC0H: ADC0 Data Word MSB .....	59
SFR Definition 5.5. ADC0L: ADC0 Data Word LSB .....	59
SFR Definition 5.6. ADC0CN: ADC0 Control .....	60
SFR Definition 5.7. ADC0GTH: ADC0 Greater-Than Data High Byte .....	61
SFR Definition 5.8. ADC0GTL: ADC0 Greater-Than Data Low Byte .....	61
SFR Definition 5.9. ADC0LTH: ADC0 Less-Than Data High Byte .....	62
SFR Definition 5.10. ADC0LTL: ADC0 Less-Than Data Low Byte .....	62
SFR Definition 6.1. REF0CN: Reference Control .....	68
SFR Definition 7.1. CPT0CN: Comparator0 Control .....	72
SFR Definition 7.2. CPT0MX: Comparator0 MUX Selection .....	73
SFR Definition 7.3. CPT0MD: Comparator0 Mode Selection .....	74
SFR Definition 7.4. CPT1CN: Comparator1 Control .....	75
SFR Definition 7.5. CPT1MX: Comparator1 MUX Selection .....	76
SFR Definition 7.6. CPT1MD: Comparator1 Mode Selection .....	77
SFR Definition 8.1. DPL: Data Pointer Low Byte .....	90
SFR Definition 8.2. DPH: Data Pointer High Byte .....	91
SFR Definition 8.3. SP: Stack Pointer .....	91
SFR Definition 8.4. PSW: Program Status Word .....	92
SFR Definition 8.5. ACC: Accumulator .....	92
SFR Definition 8.6. B: B Register .....	93
SFR Definition 8.7. IE: Interrupt Enable .....	97
SFR Definition 8.8. IP: Interrupt Priority .....	98
SFR Definition 8.9. EIE1: Extended Interrupt Enable 1 .....	99
SFR Definition 8.10. EIP1: Extended Interrupt Priority 1 .....	100
SFR Definition 8.11. IT01CF: INT0/INT1 Configuration .....	101
SFR Definition 8.12. PCON: Power Control .....	103
SFR Definition 9.1. VDM0CN: V <sub>DD</sub> Monitor Control .....	107
SFR Definition 9.2. RSTSRC: Reset Source .....	109
SFR Definition 10.1. PSCTL: Program Store R/W Control .....	116
SFR Definition 10.2. FLKEY: Flash Lock and Key .....	117
SFR Definition 10.3. FLSCL: Flash Scale .....	117
SFR Definition 11.1. EMI0CN: External Memory Interface Control .....	119
SFR Definition 12.1. OSCICL: Internal Oscillator Calibration .....	122
SFR Definition 12.2. OSCICN: Internal Oscillator Control .....	122
SFR Definition 12.3. CLKSEL: Clock Select .....	123
SFR Definition 12.4. OSCXCN: External Oscillator Control .....	125
SFR Definition 13.1. XBR0: Port I/O Crossbar Register 0 .....	134
SFR Definition 13.2. XBR1: Port I/O Crossbar Register 1 .....	135
SFR Definition 13.3. P0: Port0 .....	136
SFR Definition 13.4. P0MDIN: Port0 Input Mode .....	136

# C8051F310/1/2/3/4/5/6/7

---

SFR Definition 13.5. P0MDOUT: Port0 Output Mode	137
SFR Definition 13.6. P0SKIP: Port0 Skip	137
SFR Definition 13.7. P1: Port1	138
SFR Definition 13.8. P1MDIN: Port1 Input Mode	138
SFR Definition 13.9. P1MDOUT: Port1 Output Mode	139
SFR Definition 13.10. P1SKIP: Port1 Skip	139
SFR Definition 13.11. P2: Port2	140
SFR Definition 13.12. P2MDIN: Port2 Input Mode	140
SFR Definition 13.13. P2MDOUT: Port2 Output Mode	141
SFR Definition 13.14. P2SKIP: Port2 Skip	141
SFR Definition 13.15. P3: Port3	142
SFR Definition 13.16. P3MDIN: Port3 Input Mode	142
SFR Definition 13.17. P3MDOUT: Port3 Output Mode	143
SFR Definition 14.1. SMB0CF: SMBus Clock/Configuration	152
SFR Definition 14.2. SMB0CN: SMBus Control	154
SFR Definition 14.3. SMB0DAT: SMBus Data	156
SFR Definition 15.1. SCON0: Serial Port 0 Control	168
SFR Definition 15.2. SBUF0: Serial (UART0) Port Data Buffer	169
SFR Definition 16.1. SPI0CFG: SPI0 Configuration	180
SFR Definition 16.2. SPI0CN: SPI0 Control	181
SFR Definition 16.3. SPI0CKR: SPI0 Clock Rate	182
SFR Definition 16.4. SPI0DAT: SPI0 Data	182
SFR Definition 17.1. TCON: Timer Control	191
SFR Definition 17.2. TMOD: Timer Mode	192
SFR Definition 17.3. CKCON: Clock Control	193
SFR Definition 17.4. TL0: Timer 0 Low Byte	194
SFR Definition 17.5. TL1: Timer 1 Low Byte	194
SFR Definition 17.6. TH0: Timer 0 High Byte	194
SFR Definition 17.7. TH1: Timer 1 High Byte	194
SFR Definition 17.8. TMR2CN: Timer 2 Control	197
SFR Definition 17.9. TMR2RLL: Timer 2 Reload Register Low Byte	198
SFR Definition 17.10. TMR2RLH: Timer 2 Reload Register High Byte	198
SFR Definition 17.11. TMR2L: Timer 2 Low Byte	198
SFR Definition 17.12. TMR2H: Timer 2 High Byte	198
SFR Definition 17.13. TMR3CN: Timer 3 Control	201
SFR Definition 17.14. TMR3RLL: Timer 3 Reload Register Low Byte	202
SFR Definition 17.15. TMR3RLH: Timer 3 Reload Register High Byte	202
SFR Definition 17.16. TMR3L: Timer 3 Low Byte	202
SFR Definition 17.17. TMR3H: Timer 3 High Byte	202
SFR Definition 18.1. PCA0CN: PCA Control	215
SFR Definition 18.2. PCA0MD: PCA Mode	216
SFR Definition 18.3. PCA0CPMn: PCA Capture/Compare Mode Registers	217
SFR Definition 18.4. PCA0L: PCA Counter/Timer Low Byte	218
SFR Definition 18.5. PCA0H: PCA Counter/Timer High Byte	218
SFR Definition 18.6. PCA0CPLn: PCA Capture Module Low Byte	218

---

# C8051F310/1/2/3/4/5/6/7

---

SFR Definition 18.7. PCA0CPHn: PCA Capture Module High Byte .....	219
C2 Register Definition 20.1. C2ADD: C2 Address .....	223
C2 Register Definition 20.2. DEVICEID: C2 Device ID .....	223
C2 Register Definition 20.3. REVID: C2 Revision ID .....	224
C2 Register Definition 20.4. FPCTL: C2 Flash Programming Control .....	224
C2 Register Definition 20.5. FPDAT: C2 Flash Programming Data .....	224



# C8051F310/1/2/3/4/5/6/7

---

**NOTES:**

---

## 1. System Overview

C8051F31x devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 10-bit 200 ksps 25-channel single-ended/differential ADC with analog multiplexer (C8051F310/1/2/3/6)
- Precision programmable 25 MHz internal oscillator
- 16 kB (C8051F310/1/6/7) or 8 kB (C8051F312/3/4/5) of on-chip Flash memory
- 1280 bytes of on-chip RAM
- SMBus/I2C, Enhanced UART, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with five capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset,  $V_{DD}$  Monitor, and Temperature Sensor
- On-chip Voltage Comparators (2)
- 29/25/21 Port I/O (5 V tolerant)

With on-chip Power-On Reset,  $V_{DD}$  monitor, Watchdog Timer, and clock oscillator, the C8051F31x devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system programming and debugging without occupying package pins.

Each device is specified for 2.7-to-3.6 V operation over the industrial temperature range ( $-45$  to  $+85$  °C). The Port I/O and RST pins are tolerant of input signals up to 5 V. The C8051F31x are available in 32-pin LQFP, 28-pin QFN, and 24-pin QFN packages. See Table 1.1 for ordering part numbers. Note: QFN packages are also referred to as MLP or MLF packages.

# C8051F310/1/2/3/4/5/6/7

**Table 1.1. Product Selection Guide**

Ordering Part Number	MIPS (Peak)	Flash Memory	RAM	Calibrated Internal 24.5 MHz Oscillator	SMBus/I2C	Enhanced SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 200 ksps ADC	Temperature Sensor	Analog Comparators	Lead-free (RoHS Compliant)	Package
C8051F310	25	16	1280	✓	✓	✓	✓	✓	✓	29	✓	✓	2	-	LQFP-32
C8051F310-GQ	25	16	1280	✓	✓	✓	✓	✓	✓	29	✓	✓	2	✓	LQFP-32
C8051F311	25	16	1280	✓	✓	✓	✓	✓	✓	25	✓	✓	2	-	QFN-28
C8051F311-GM	25	16	1280	✓	✓	✓	✓	✓	✓	25	✓	✓	2	✓	QFN-28
C8051F312	25	8	1280	✓	✓	✓	✓	✓	✓	29	✓	✓	2	-	LQFP-32
C8051F312-GQ	25	8	1280	✓	✓	✓	✓	✓	✓	29	✓	✓	2	✓	LQFP-32
C8051F313	25	8	1280	✓	✓	✓	✓	✓	✓	25	✓	✓	2	-	QFN-28
C8051F313-GM	25	8	1280	✓	✓	✓	✓	✓	✓	25	✓	✓	2	✓	QFN-28
C8051F314	25	8	1280	✓	✓	✓	✓	✓	✓	29	-	-	2	-	LQFP-32
C8051F314-GQ	25	8	1280	✓	✓	✓	✓	✓	✓	29	-	-	2	✓	LQFP-32
C8051F315	25	8	1280	✓	✓	✓	✓	✓	✓	25	-	-	2	-	QFN-28
C8051F315-GM	25	8	1280	✓	✓	✓	✓	✓	✓	25	-	-	2	✓	QFN-28
C8051F316-GM	25	16	1280	✓	✓	✓	✓	✓	✓	21	✓	✓	2	✓	QFN-24
C8051F317-GM	25	16	1280	✓	✓	✓	✓	✓	✓	21	-	-	2	✓	QFN-24

# C8051F310/1/2/3/4/5/6/7

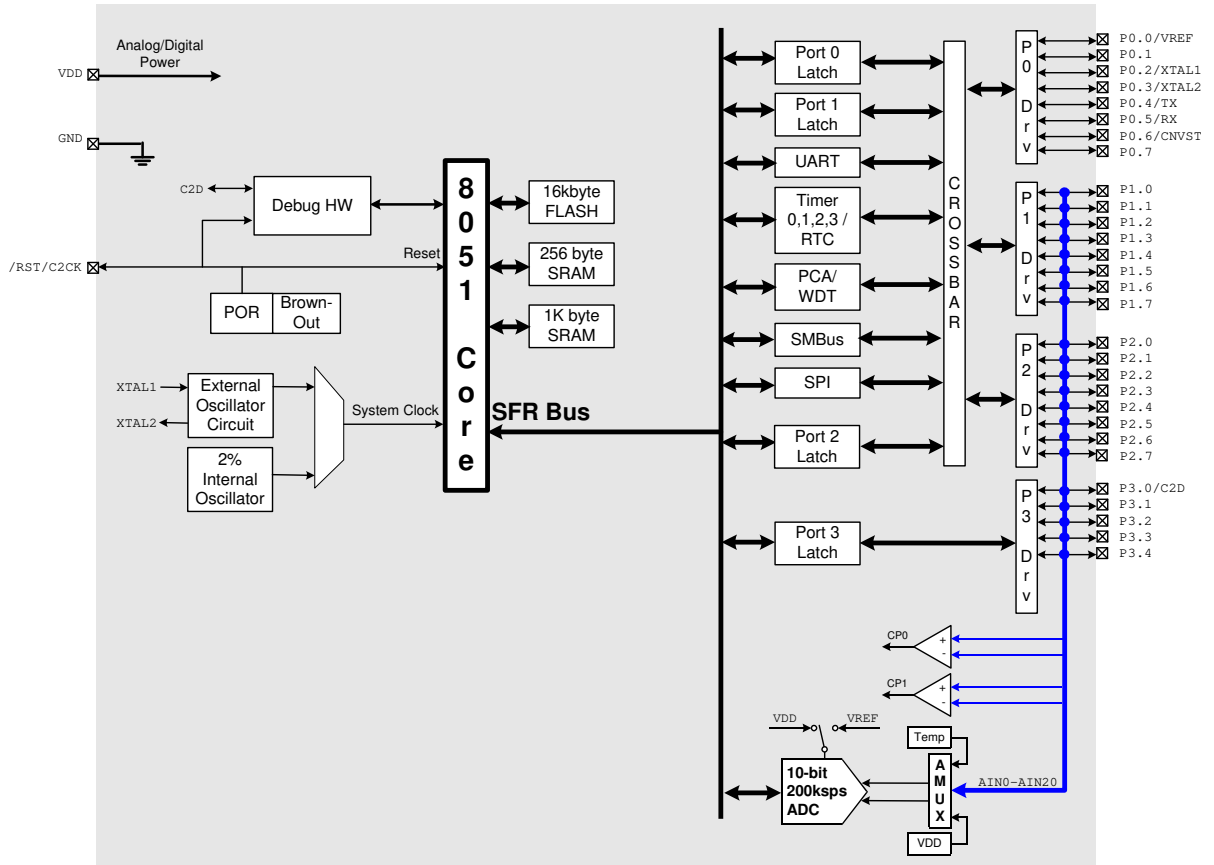


Figure 1.1. C8051F310 Block Diagram

# C8051F310/1/2/3/4/5/6/7

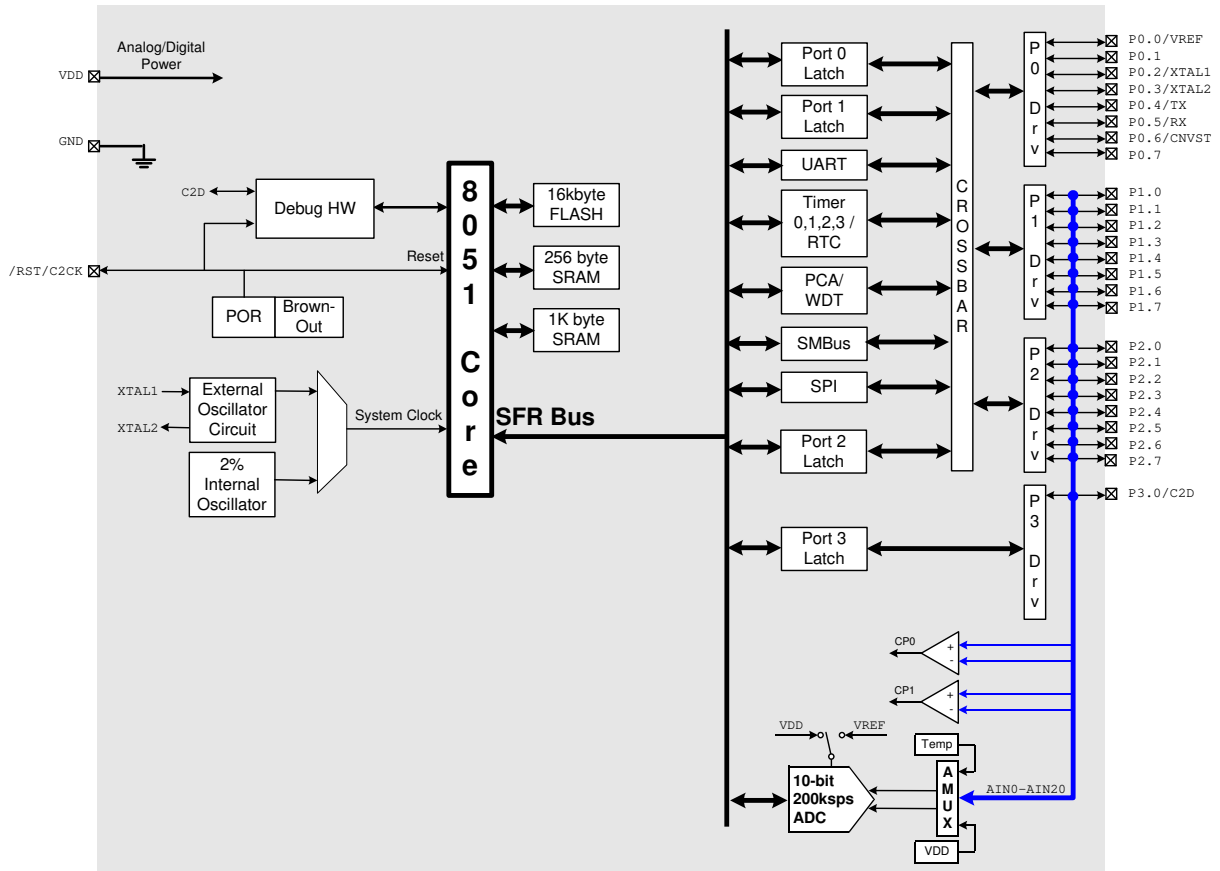


Figure 1.2. C8051F311 Block Diagram

# C8051F310/1/2/3/4/5/6/7

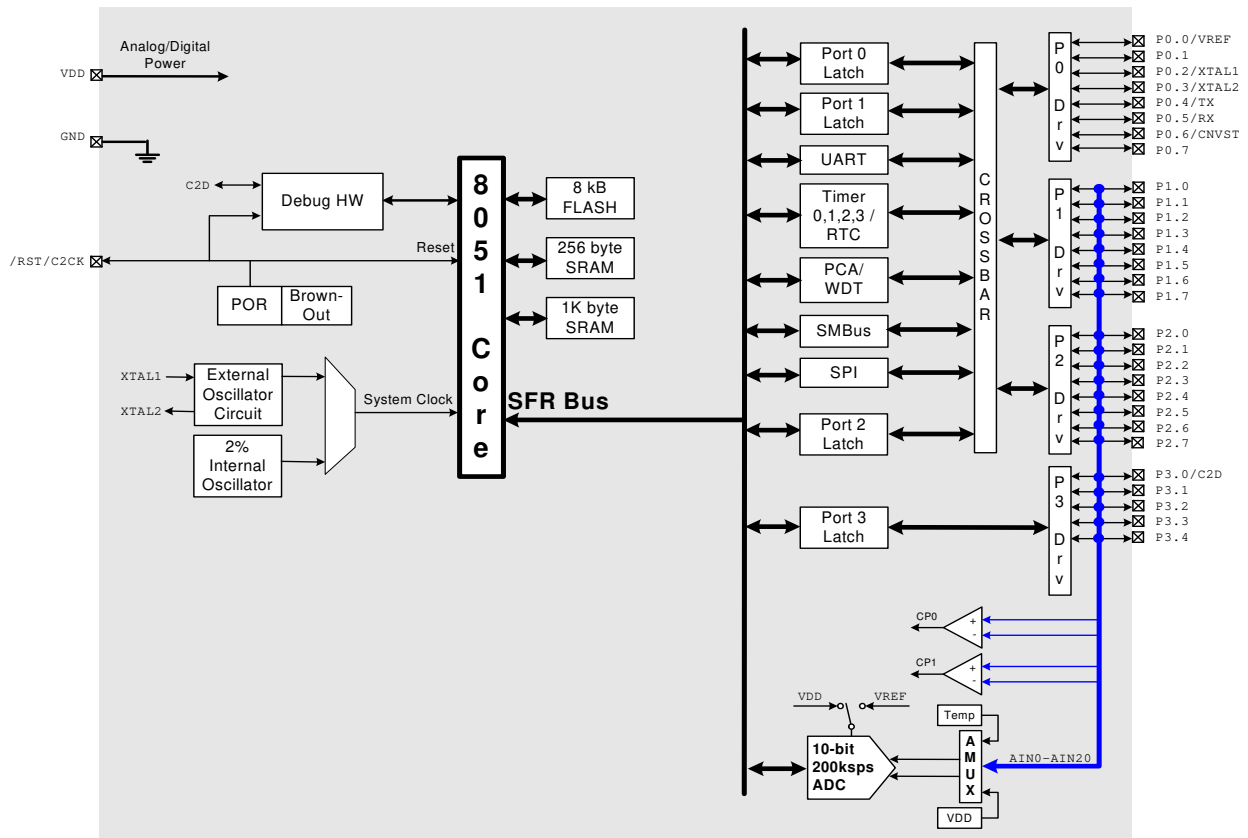


Figure 1.3. C8051F312 Block Diagram

# C8051F310/1/2/3/4/5/6/7

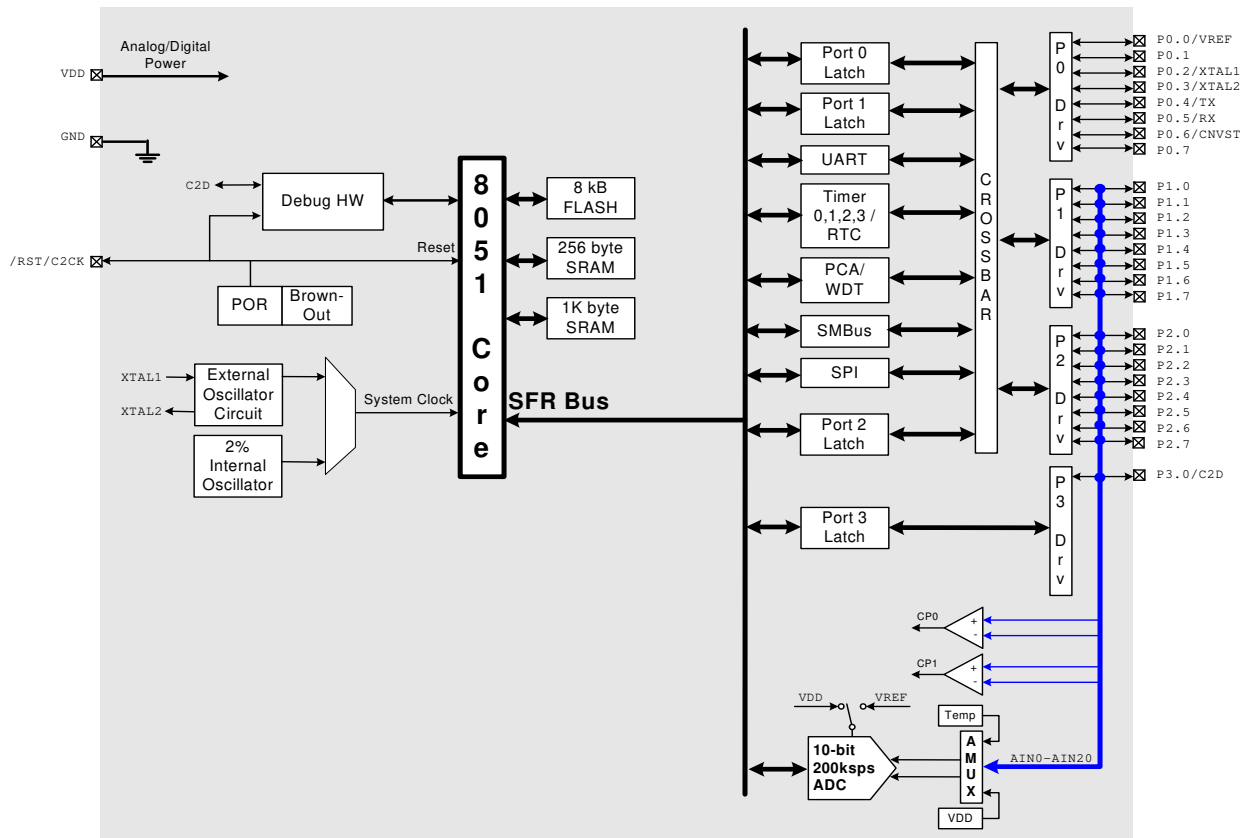


Figure 1.4. C8051F313 Block Diagram

# C8051F310/1/2/3/4/5/6/7

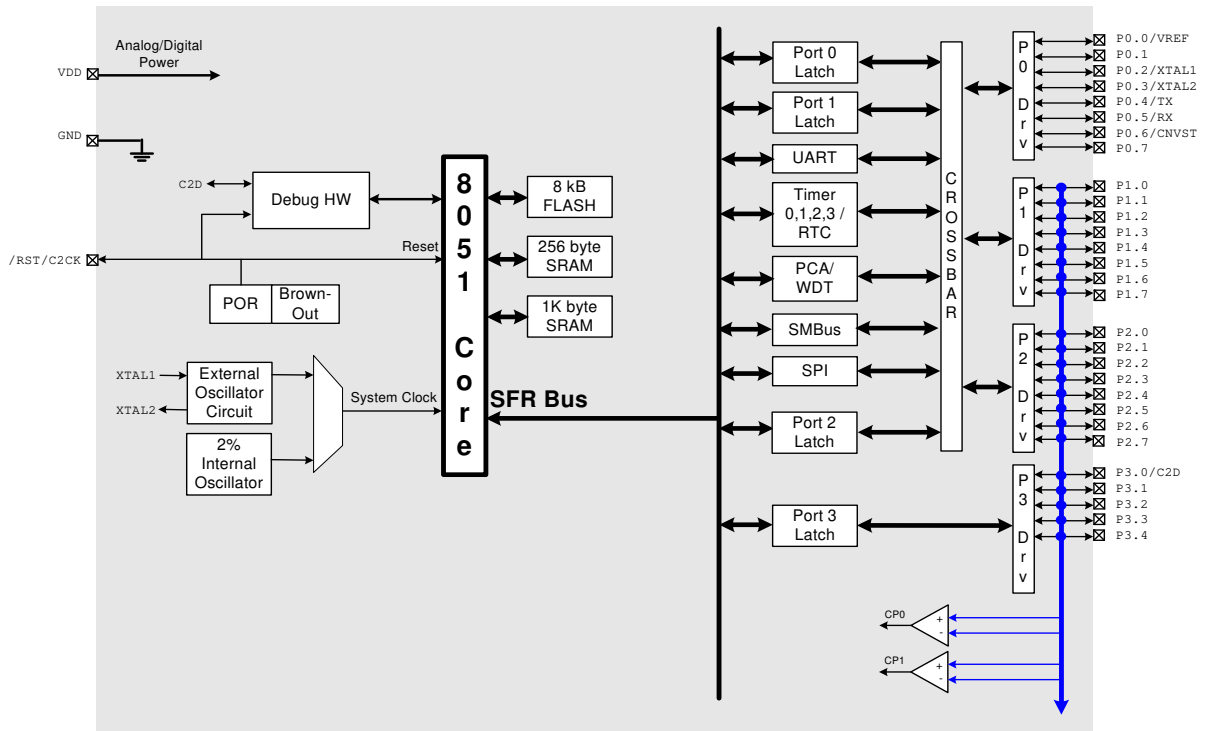


Figure 1.5. C8051F314 Block Diagram



# C8051F310/1/2/3/4/5/6/7

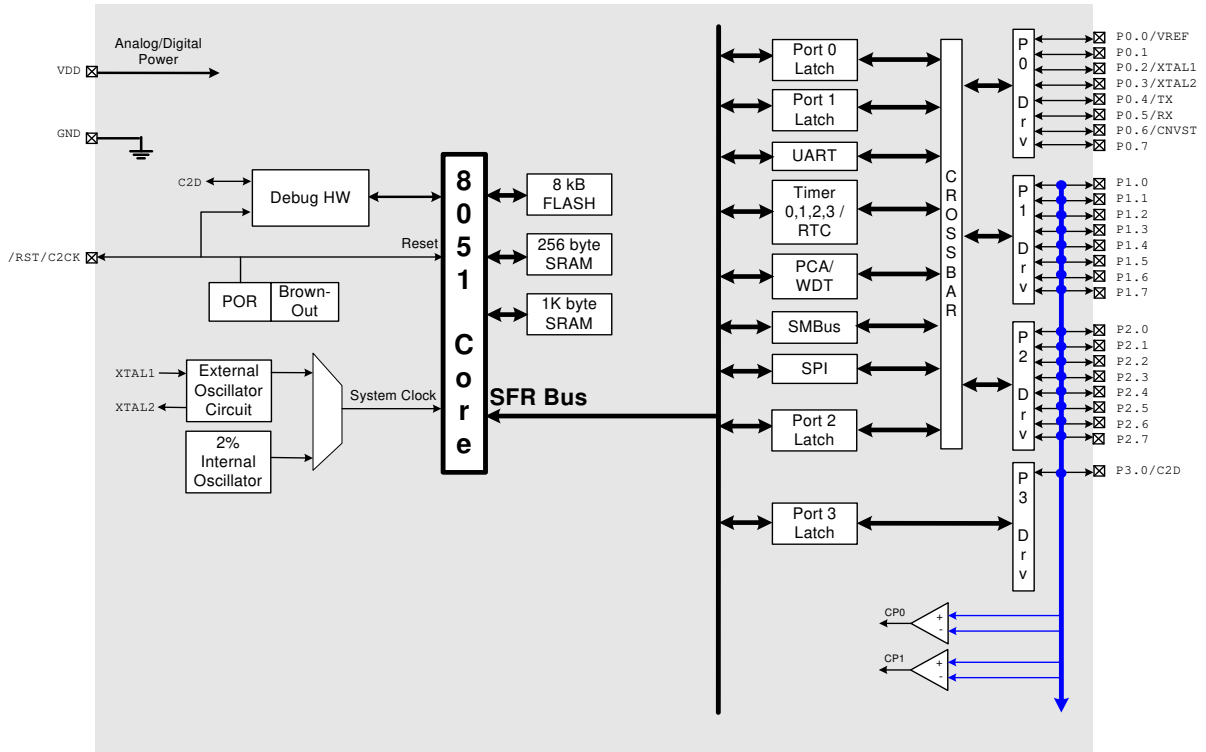


Figure 1.6. C8051F315 Block Diagram

# C8051F310/1/2/3/4/5/6/7

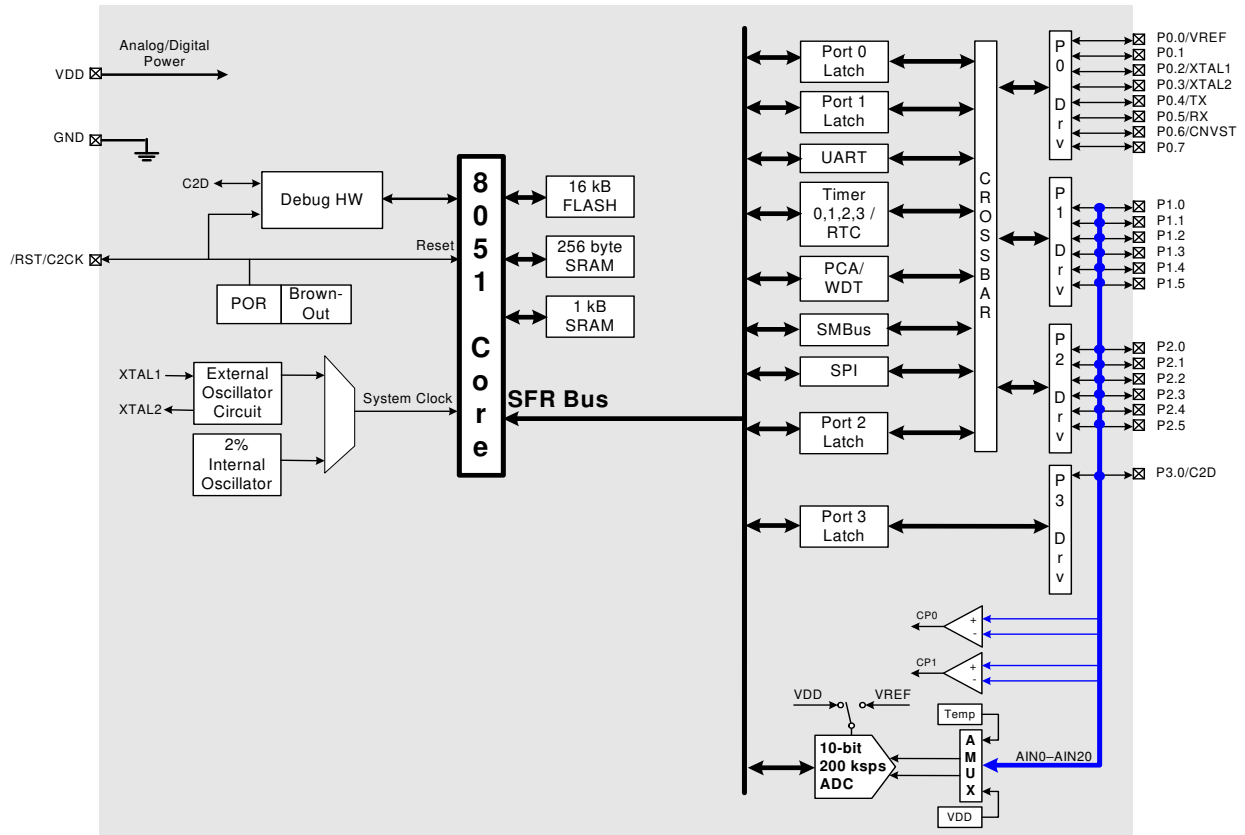


Figure 1.7. C8051F316 Block Diagram