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C8051F320/1

Full Speed USB, 16k ISP FLASH MCU Family

ANALOG PERIPHERALS
- **10-Bit ADC**
  - Up to 200 ksps
  - Up to 17 or 13 External Single-Ended or Differential Inputs
  - VREF from External Pin, Internal Reference, or VDD
  - Built-in Temperature Sensor
  - External Conversion Start Input
- **Two Comparators**
- **Internal Voltage Reference**
- **POR/Brown-Out Detector**

USB FUNCTION CONTROLLER
- USB Specification 2.0 Compliant
- Full Speed (12 Mbps) or Low Speed (1.5 Mbps) Operation
- Integrated Clock Recovery; No External Crystal Required for Full Speed or Low Speed
- Supports Eight Flexible Endpoints
- 1k Byte USB Buffer Memory
- Integrated Transceiver; No External Resistors Required

ON-CHIP DEBUG
- On-Chip Debug Circuitry Facilitates Full Speed, Non-Intrusive In-System Debug (No Emulator Required!)
- Provides Breakpoints, Single Stepping, Inspect/Modify Memory and Registers
- Superior Performance to Emulation Systems Using ICE-Chips, Target Pods, and Sockets

VOLTAGE REGULATOR INPUT: 4.0V TO 5.25V

HIGH SPEED 8051 µC Core
- Pipelined Instruction Architecture; Executes 70% of Instructions in 1 or 2 System Clocks
- Up to 25 MIPS Throughput with 25 MHz Clock
- Expanded Interrupt Handler

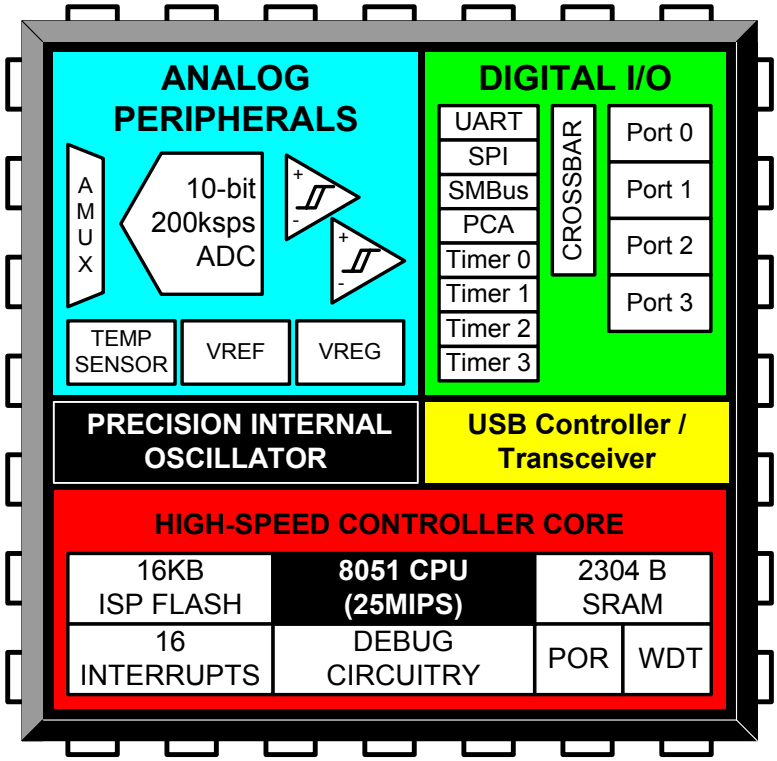
MEMORY
- 2304 Bytes Internal RAM (1k + 256 + 1k USB FIFO)
- 16k Bytes FLASH; In-system programmable in 512-byte Sectors

DIGITAL PERIPHERALS
- 25/21 Port I/O; All 5 V tolerant with High Sink Current
- Hardware Enhanced SPI™, Enhanced UART, and SMBus™ Serial Ports
- Four General Purpose 16-Bit Counter/Timers
- 16-Bit Programmable Counter Array (PCA) with Five Capture/Compare Modules
- Real Time Clock Mode using External Clock Source and PCA or Timer

CLOCK SOURCES
- Internal Oscillator: 0.25% Accuracy with Clock Recovery enabled. Supports all USB and UART Modes
- External Oscillator: Crystal, RC, C, or Clock (1 or 2 Pin Modes)
- Can Switch Between Clock Sources on-the-fly; Useful in Power Saving Strategies

PACKAGES
- 32-pin LQFP (C8051F320)
- 28-pin MLP (C8051F321)

TEMPERATURE RANGE: -40°C TO +85°C



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1. SYSTEM OVERVIEW

C8051F320/1 devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- Universal Serial Bus (USB) Function Controller with eight flexible endpoint pipes, integrated transceiver, and 1k FIFO RAM
- Supply Voltage Regulator (5V-to-3V)
- True 10-bit 200 ksps 17-channel single-ended/differential ADC with analog multiplexer
- On-chip Voltage Reference and Temperature Sensor
- On-chip Voltage Comparators (2)
- Precision programmable 12 MHz internal oscillator and 4x clock multiplier
- 16k bytes of on-chip FLASH memory
- 2304 total bytes of on-chip RAM (256 + 1k + 1k USB FIFO)
- SMBus/I^2C, Enhanced UART, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with five capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, VDD Monitor, and Missing Clock Detector
- 25/21 Port I/O (5V tolerant)

With on-chip Power-On Reset, VDD monitor, Voltage Regulator, Watchdog Timer, and clock oscillator, C8051F320/1 devices are truly stand-alone System-on-a-Chip solutions. The FLASH memory can be reprogrammed in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 2.7 V-to-3.6 V operation over the industrial temperature range (-40°C to +85°C). (Note that 3.0 V-to-3.6 V is required for USB communication.) The Port I/O and /RST pins are tolerant of input signals up to 5 V. C8051F320/1 are available in a 32-pin LQFP or a 28-pin MLP package.

Table 1.1. Product Selection Guide

	MIPS (Peak)	FLASH Memory	RAM	Calibrated Internal Oscillator	USB	Supply Voltage Regulator	SMBus/I^2C	Enhanced SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 200ksps ADC	Temperature Sensor	Voltage Reference	Analog Comparators	Package
C8051F320	25	16k	2304	✓	✓	✓	✓	✓	✓	4	✓	25	✓	✓	✓	2	LQFP-32
C8051F321	25	16k	2304	✓	✓	✓	✓	✓	✓	4	✓	21	✓	✓	✓	2	MLP-28

Figure 1.1. C8051F320 Block Diagram

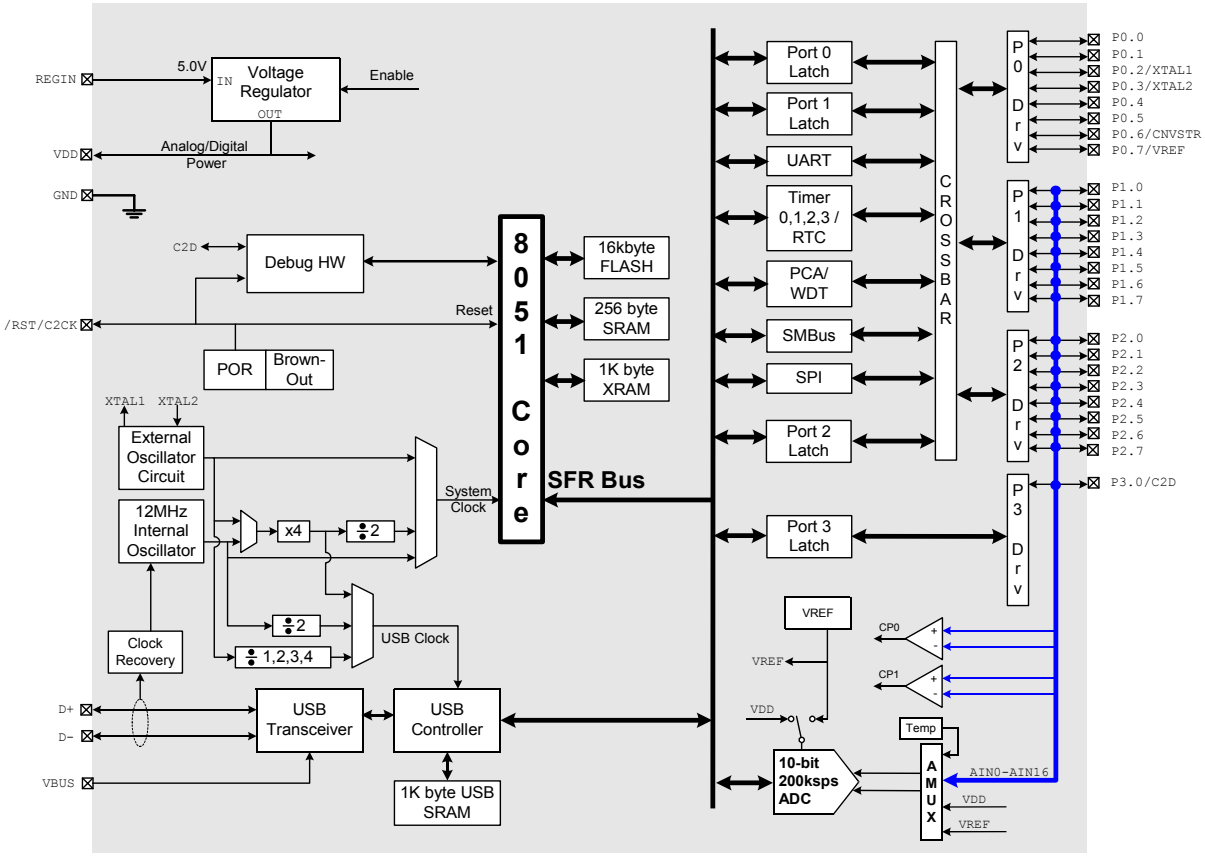
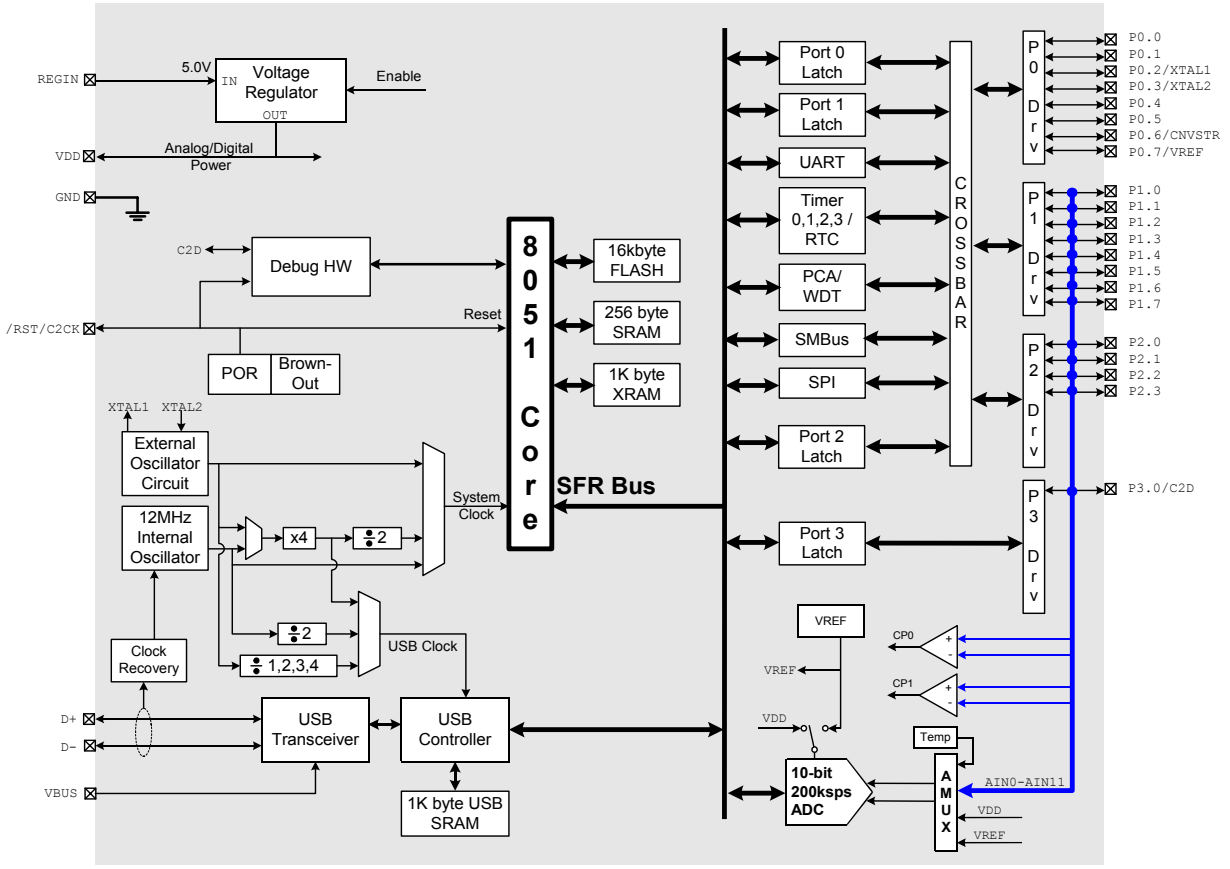


Figure 1.2. C8051F321 Block Diagram



1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F320/1 family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052, including four 16-bit counter/timers, a full-duplex UART with extended baud rate configuration, an enhanced SPI port, 2304 bytes of on-chip RAM, 128 byte Special Function Register (SFR) address space, and 25/21 I/O pins.

1.1.2. Improved Throughput

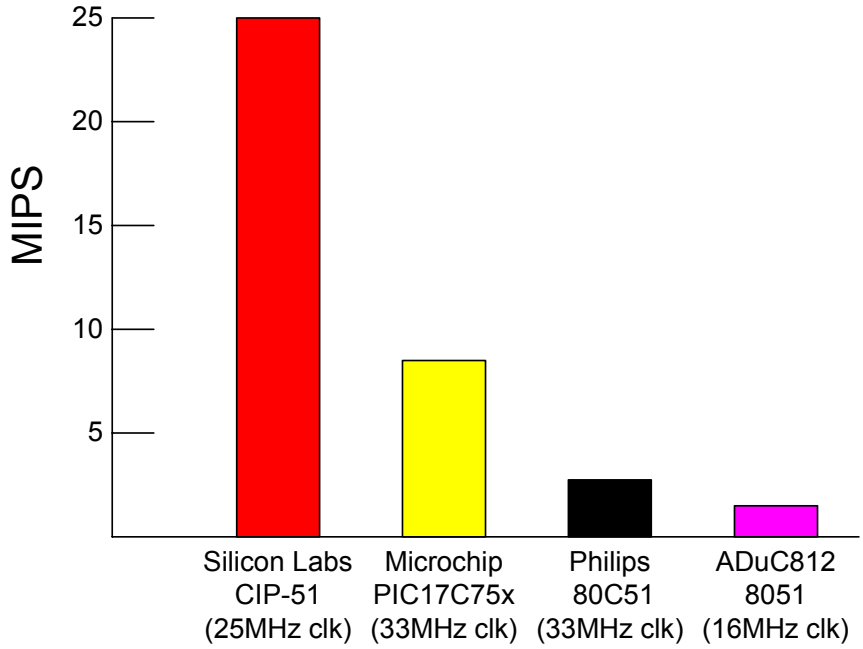
The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. Figure 1.3 shows a comparison of peak throughputs for various 8-bit microcontroller cores with their maximum system clocks.

Figure 1.3. Comparison of Peak MCU Execution Speeds



1.1.3. Additional Features

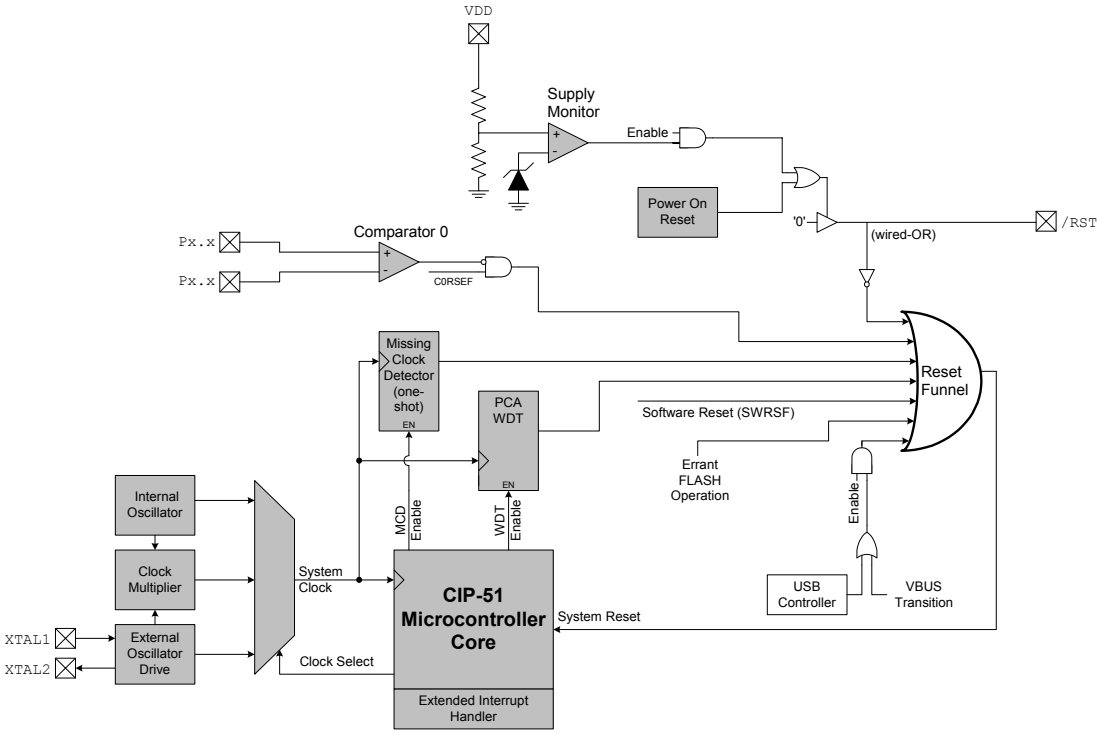
The C8051F320/1 SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides 16 interrupt sources into the CIP-51 (as opposed to 7 for the standard 8051), allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Nine reset sources are available: power-on reset circuitry (POR), an on-chip VDD monitor (forces reset when power supply voltage drops below V_{RST} as given in Table 10.1 on page 105), the USB controller (USB bus reset or a VBUS transition), a Watchdog Timer, a Missing Clock Detector, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an errant FLASH read/write protection circuit. Each reset source except for the POR, Reset Input Pin, or FLASH error may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The internal oscillator is factory calibrated to 12 MHz ±1.5%, and the internal oscillator period may be user programmed in ~0.25% increments. A clock recovery mechanism allows the internal oscillator to be used with the 4x Clock Multiplier as the USB clock source in Full Speed mode; the internal oscillator can also be used as the USB clock source in Low Speed mode. External oscillators may also be used with the 4x Clock Multiplier. An external oscillator drive circuit is also included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. The system clock may be configured to use the internal oscillator, external oscillator, or the Clock Multiplier output divided by 2. If desired, the system clock source may be switched on-the-fly between oscillator sources. An external oscillator can be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) external clock source, while periodically switching to the internal oscillator as needed.

Figure 1.4. On-Chip Clock and Reset

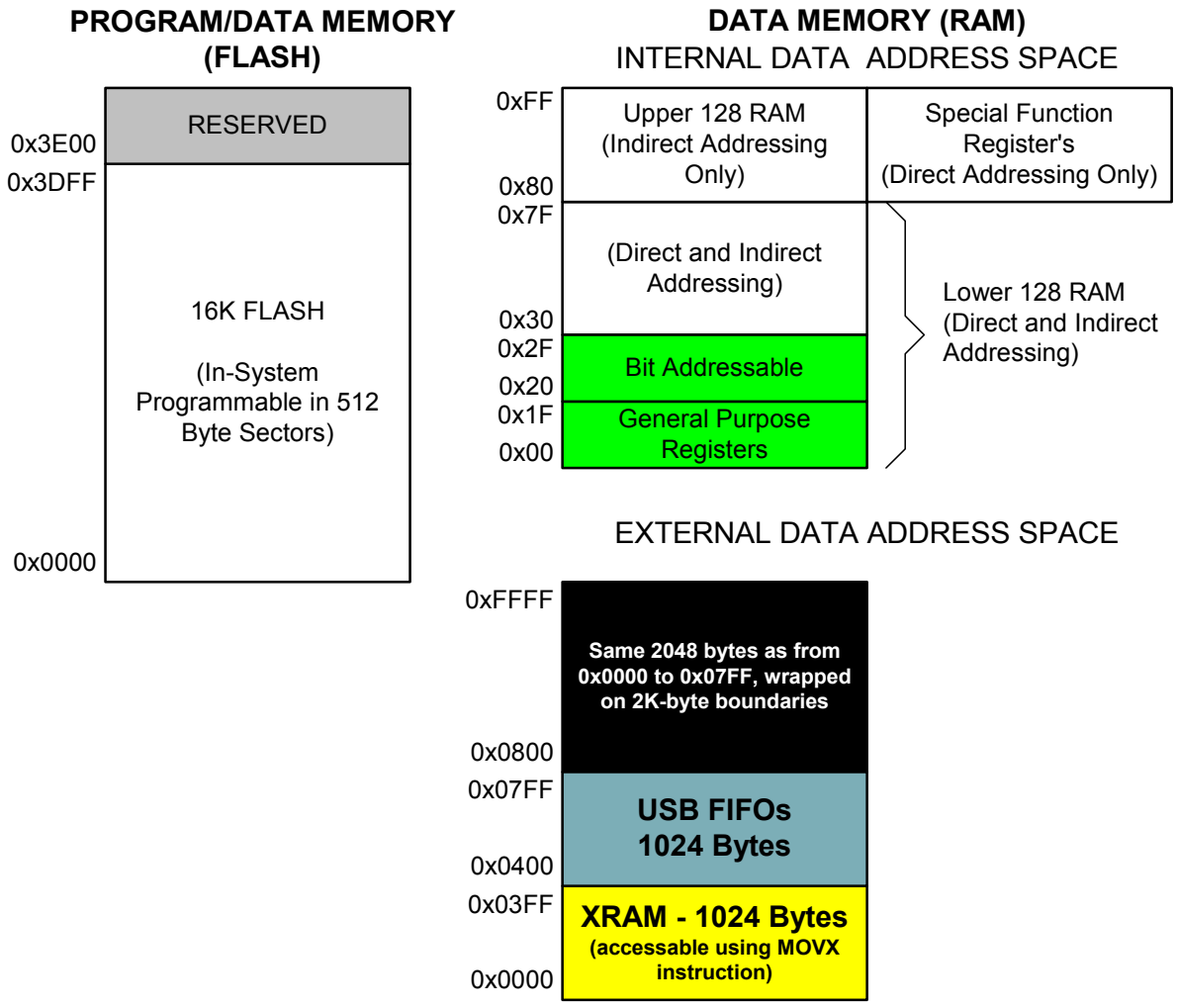


1.2. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

Program memory consists of 16k bytes of FLASH. This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. See Figure 1.5 for the MCU system memory map.

Figure 1.5. On-Board Memory Map



1.3. Universal Serial Bus Controller

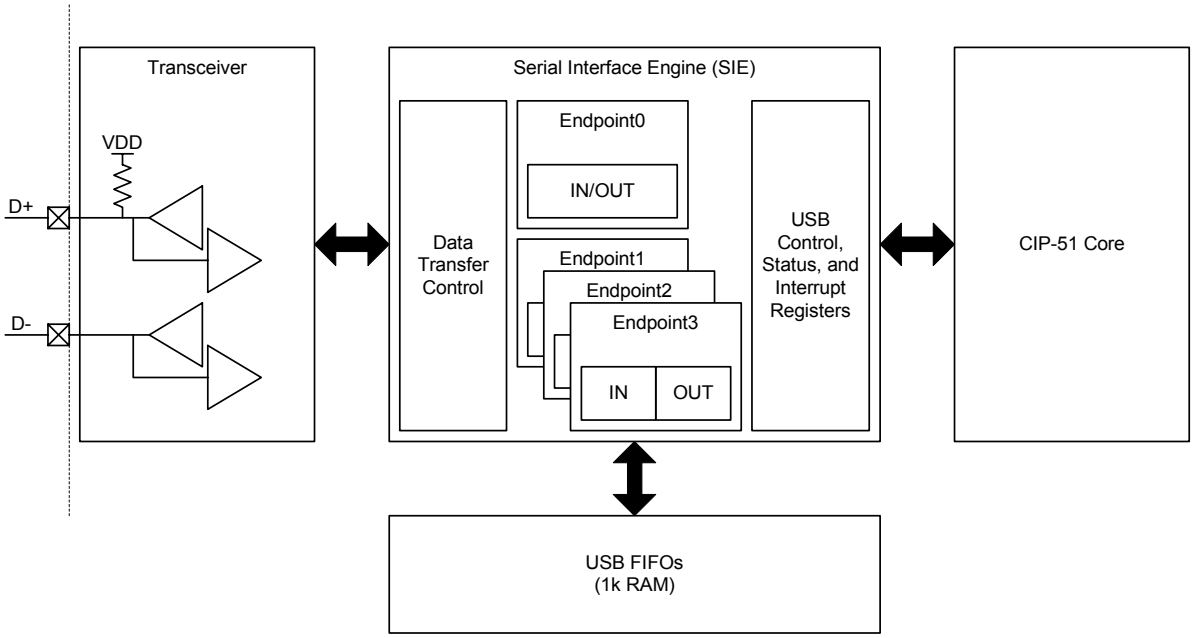
The Universal Serial Bus Controller (USB0) is a USB 2.0 compliant Full or Low Speed function with integrated transceiver and endpoint FIFO RAM. A total of eight endpoint pipes are available: a bi-directional control endpoint (Endpoint0) and three pairs of IN/OUT endpoints (Endpoints1-3 IN/OUT).

A 1k block of XRAM is used as dedicated USB FIFO space. This FIFO space is distributed among Endpoints0-3; Endpoint1-3 FIFO slots can be configured as IN, OUT, or both IN and OUT (split mode). The maximum FIFO size is 512 bytes (Endpoint3).

USB0 can be operated as a Full or Low Speed function. On-chip 4x Clock Multiplier and clock recovery circuitry allow both Full and Low Speed options to be implemented with the on-chip precision oscillator as the USB clock source. An external oscillator source can also be used with the 4x Clock Multiplier to generate the USB clock. The CPU clock source is independent of the USB clock.

The USB Transceiver is USB 2.0 compliant, and includes on-chip matching and pull-up resistors. The pull-up resistors can be enabled/disabled in software, and will appear on the D+ or D- pin according to the software-selected speed setting (Full or Low Speed).

Figure 1.6. USB Controller Block Diagram



1.4. Voltage Regulator

C8051F320/1 devices include a 5 V-to-3 V voltage regulator (REG0). When enabled, the REG0 output appears on the VDD pin and can be used to power external devices. REG0 can be enabled/disabled by software.

1.5. On-Chip Debug Circuitry

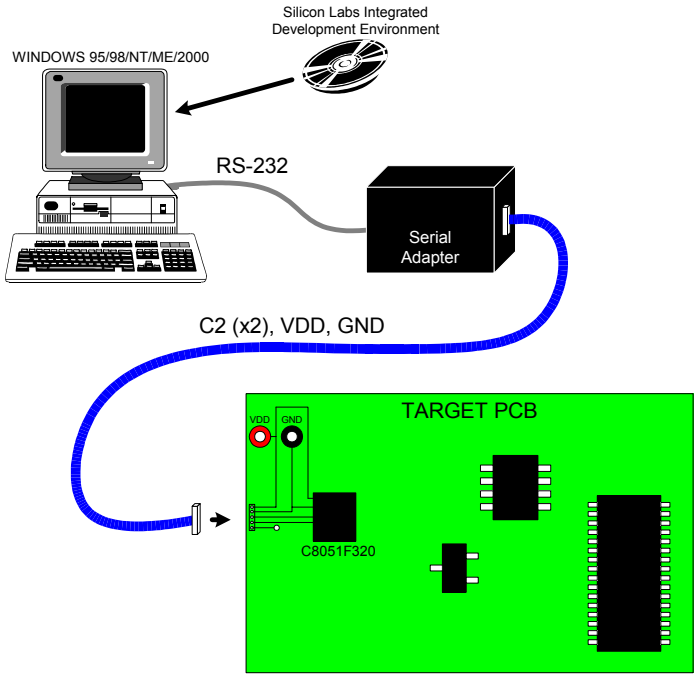
The C8051F320/1 devices include on-chip Silicon Labs 2-Wire (C2) debug circuitry that provides non-intrusive, full speed, in-circuit debugging of the production part *installed in the end application.*

Silicon Labs' debugging system supports inspection and modification of memory and registers, breakpoints, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the USB, ADC, and SMBus) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F310DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F320/1 MCUs. The kit includes software with a developer's studio and debugger, an integrated 8051 assembler, and an RS-232 to C2 serial adapter. It also has a target application board with the associated MCU installed and prototyping area, plus the RS-232 and C2 cables, and wall-mount power supply. The Development Kit requires a Windows 95/98/NT/ME/2000 computer with one available RS-232 serial port. As shown in Figure 1.7, the PC is connected via RS-232 to the Serial Adapter. A six-inch ribbon cable connects the Serial Adapter to the user's application board, picking up the two C2 pins and VDD and GND. The Serial Adapter takes its power from the application board. For applications where there is not sufficient power available from the target board, the provided power supply can be connected directly to the Serial Adapter.

The Silicon Labs IDE interface is a vastly superior developing and debugging configuration, compared to standard MCU emulators that use on-board "ICE Chips" and require the MCU in the application board to be socketed. Silicon Labs' debug paradigm increases ease of use and preserves the performance of the precision analog peripherals.

Figure 1.7. Development/In-System Debug Diagram

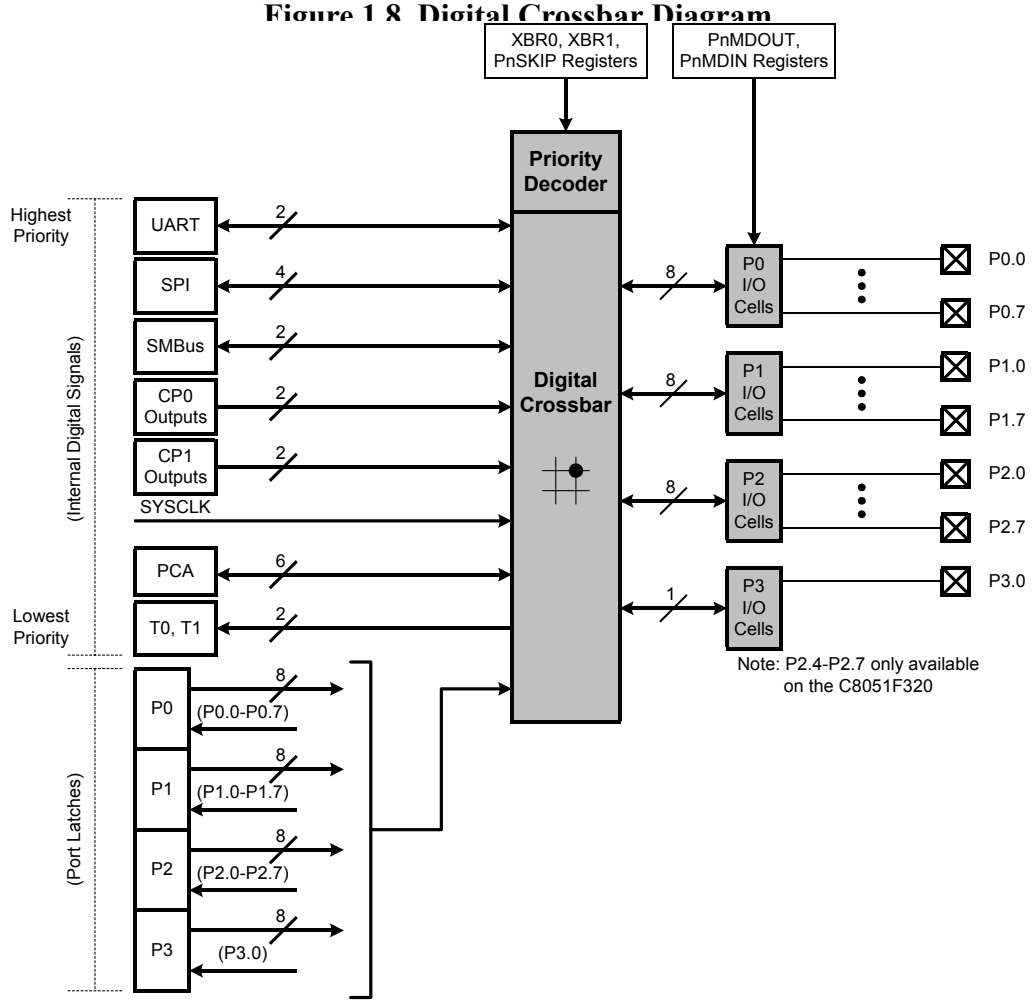


1.6. Programmable Digital I/O and Crossbar

C8051F320 devices include 25 I/O pins (three byte-wide Ports and one 1-bit-wide Port); C8051F321 devices include 21 I/O pins (two byte-wide Ports, one 4-bit-wide Port, and one 1-bit-wide Port). The C8051F320/1 Ports behave like typical 8051 Ports with a few enhancements. Each Port pin may be configured as an analog input or a digital I/O pin. Pins selected as digital I/Os may additionally be configured for push-pull or open-drain output. The "weak pull-ups" that are fixed on typical 8051 devices may be globally disabled, providing power savings capabilities.

The Digital Crossbar allows mapping of internal digital system resources to Port I/O pins (See Figure 1.8). On-chip counter/timers, serial buses, HW interrupts, comparator outputs, and other digital signals in the controller can be configured to appear on the Port I/O pins specified in the Crossbar Control registers. This allows the user to select the exact mix of general purpose Port I/O and digital resources needed for the particular application.

Figure 1.8. Digital Crossbar Diagram



1.7. Serial Ports

The C8051F320/1 Family includes an SMBus/I^2C interface, a full-duplex UART with enhanced baud rate configuration, and an Enhanced SPI interface. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.