Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

C8051F326/7

Full Speed USB, 16 kB Flash MCU Family

USB Function Controller
- USB specification 2.0 compliant
- Full speed (12 Mbps) or low speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for full speed or low speed
- Supports three fixed-function endpoints
- 256 Byte USB buffer memory
- Integrated transceiver; no external resistors required

On-Chip Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Voltage Supply Input: 2.7 to 5.25 V
- Voltages from 3.6 to 5.25 V supported using On-Chip Voltage Regulator

High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

Memory
- 1536 bytes internal RAM (1 k + 256 + 256 USB FIFO)
- 16k bytes Flash; In-system programmable in 512-byte sectors

Digital Peripherals
- 15 Port I/O; All 5 V tolerant with high sink current
- Enhanced UART
- Two general purpose 16-bit timers

Clock Sources
- Internal oscillator: 0.25% accuracy with clock recovery enabled. Supports all USB and UART modes
- External CMOS clock
- Can switch between clock sources on-the-fly; useful in power saving strategies

Packages
- 28-pin QFN
- Temperature Range: –40 to +85 °C

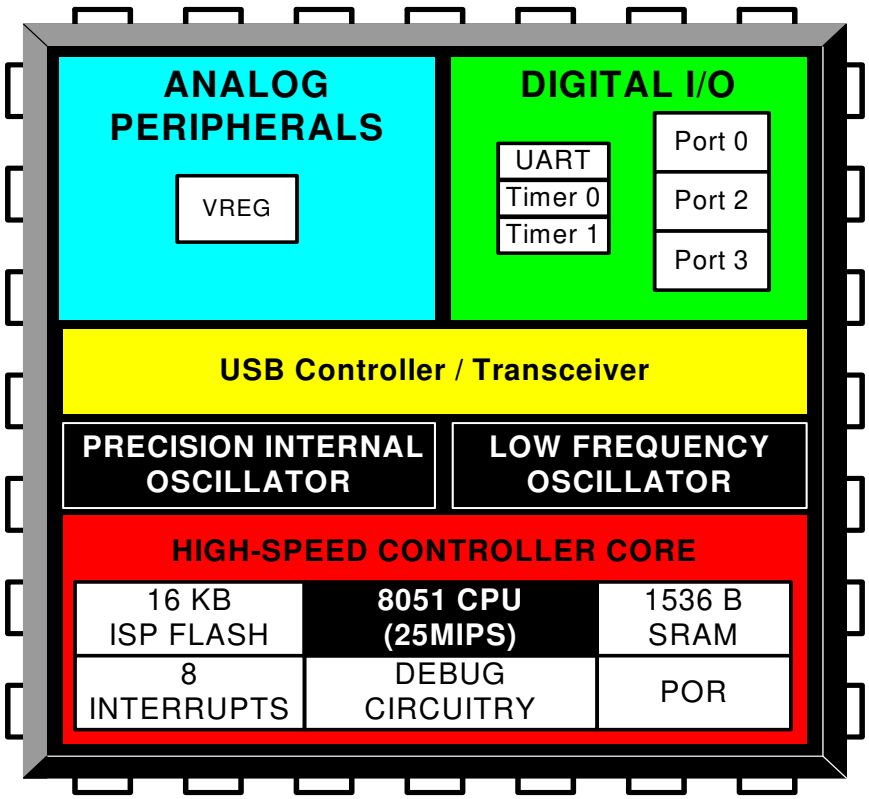

Table of Contents

List of Figures

List of Tables

List of Registers

1. System Overview

C8051F326/7 devices are fully integrated mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- Universal serial bus (USB) function controller with three fixed-function endpoint pipes, integrated transceiver, and 256B FIFO RAM
- Supply voltage regulator
- Precision programmable 12 MHz internal oscillator and 4x clock multiplier
- 16k kB of on-chip Flash memory
- 1536 total bytes of on-chip RAM (256 + 1 k + 256 USB FIFO)
- Enhanced UART, serial interfaces implemented in hardware
- Two general-purpose 16-bit timers
- On-chip power-on reset, VDD monitor, and missing clock detector
- 15 Port I/O (5 V tolerant)

With on-chip power-on reset, VDD monitor, voltage regulator, and clock oscillator, C8051F326/7 devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Laboratories 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 2.7–5.25 V operation over the industrial temperature range (–40 to +85 °C). For voltages above 3.6 V, the on-chip Voltage Regulator must be used. A minimum of 3.0 V is required for USB communication. The Port I/O and $\overline{\text{RST}}$ pins are tolerant of input signals up to 5 V. C8051F326/7 are available in two 28-pin QFN packages with different pinouts. The RoHS compliant devices are marked with a -GM suffix in the part number. The port I/O on C8051F326 devices is powered from a separate I/O supply allowing it to interface to low voltage logic.

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory	RAM	Calibrated Internal Oscillator	USB	Supply Voltage Regulator	UART	Timers (16-bit)	Digital Port I/Os	Separate I/O Supply	Package
C8051F326-GM	25	16k	1536	✓	✓	✓	✓	2	15	✓	QFN-28
C8051F327-GM	25	16k	1536	✓	✓	✓	✓	2	15	—	QFN-28

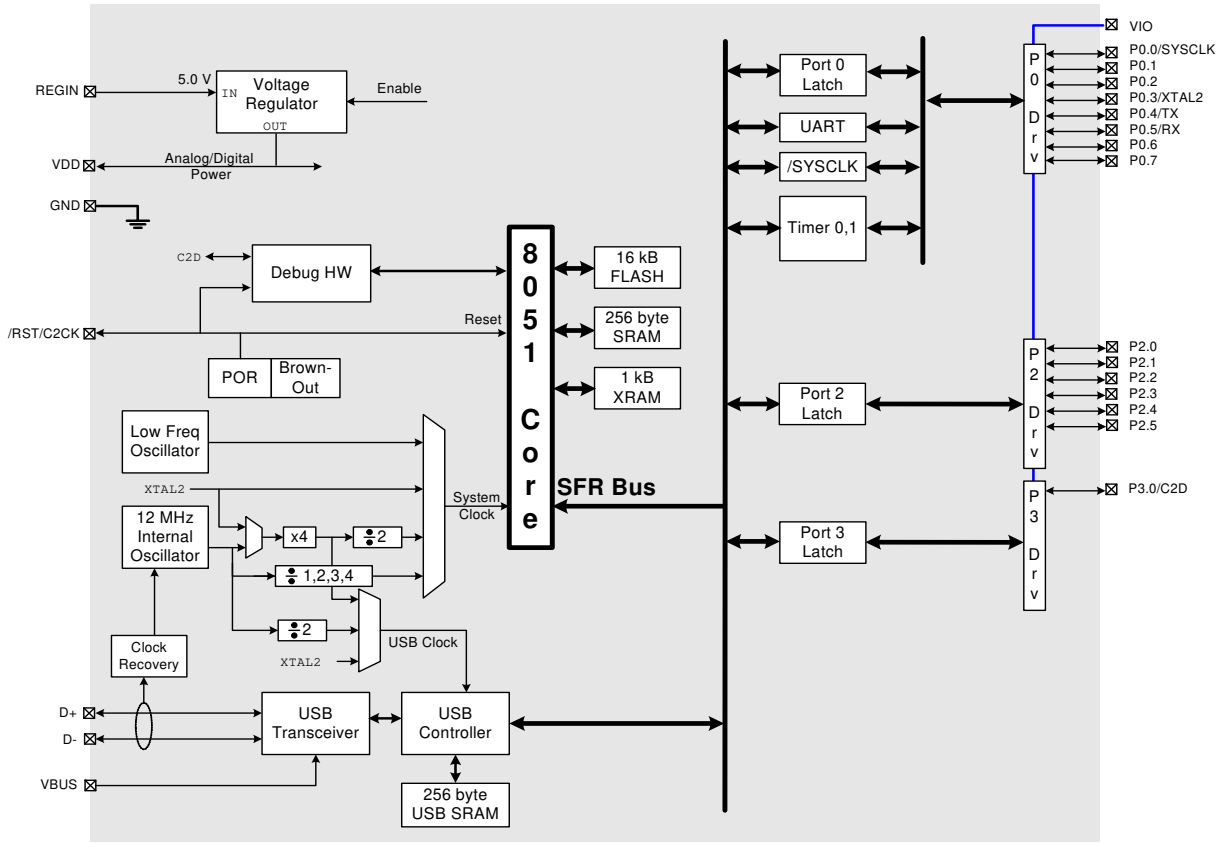

Figure 1.1. C8051F326 Block Diagram

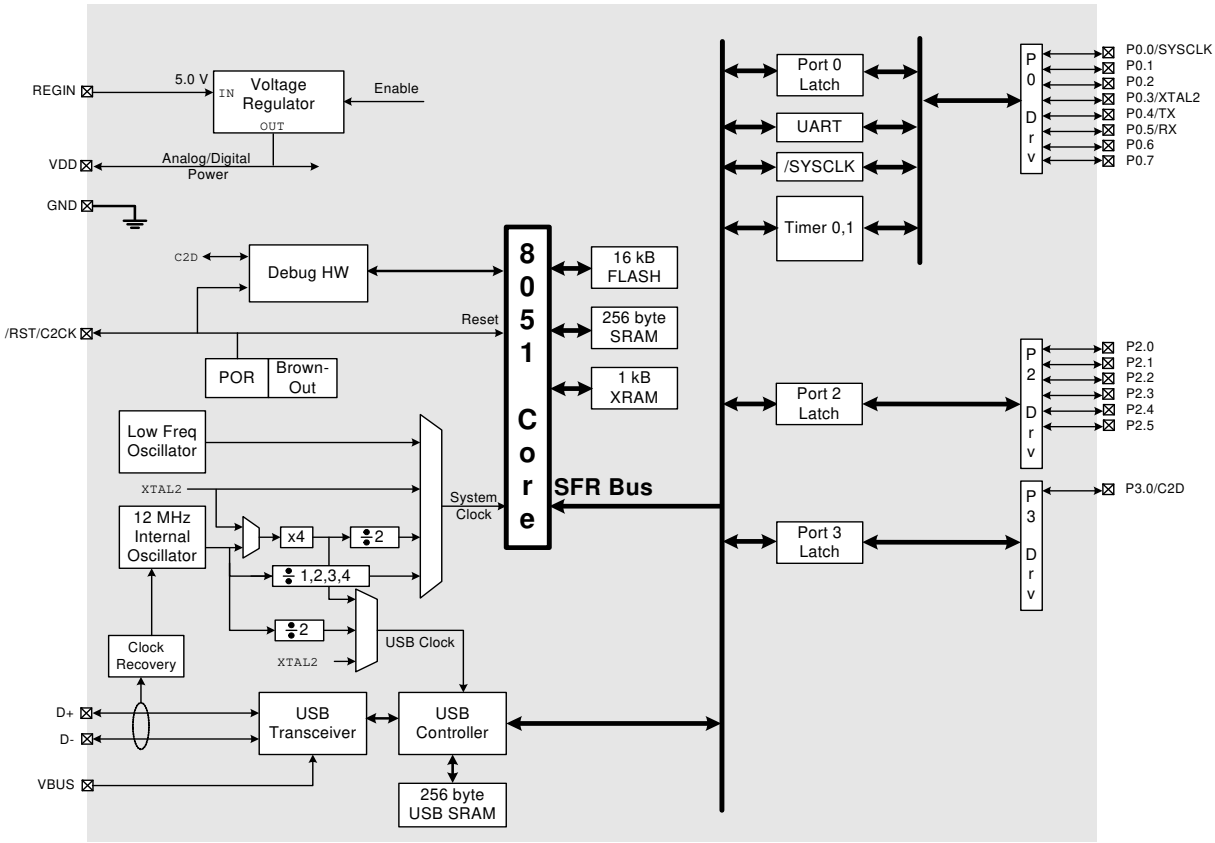

Figure 1.2. C8051F327 Block Diagram

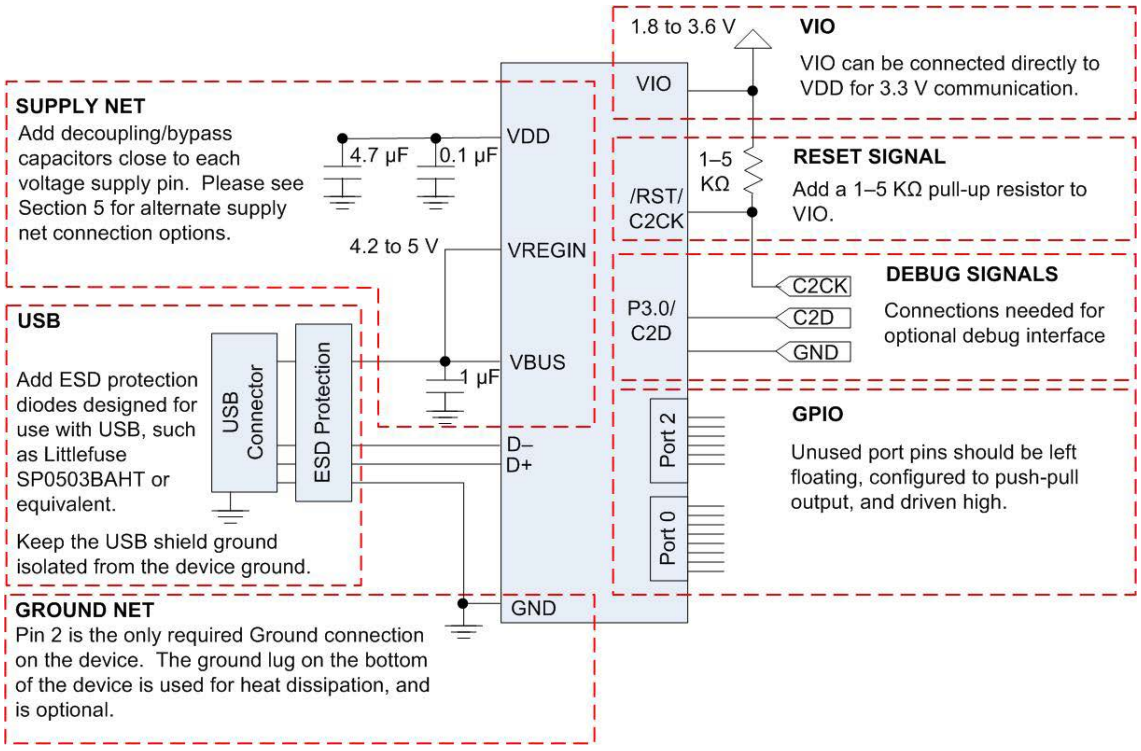

Figure 1.3. Typical Connections for the C8051F326

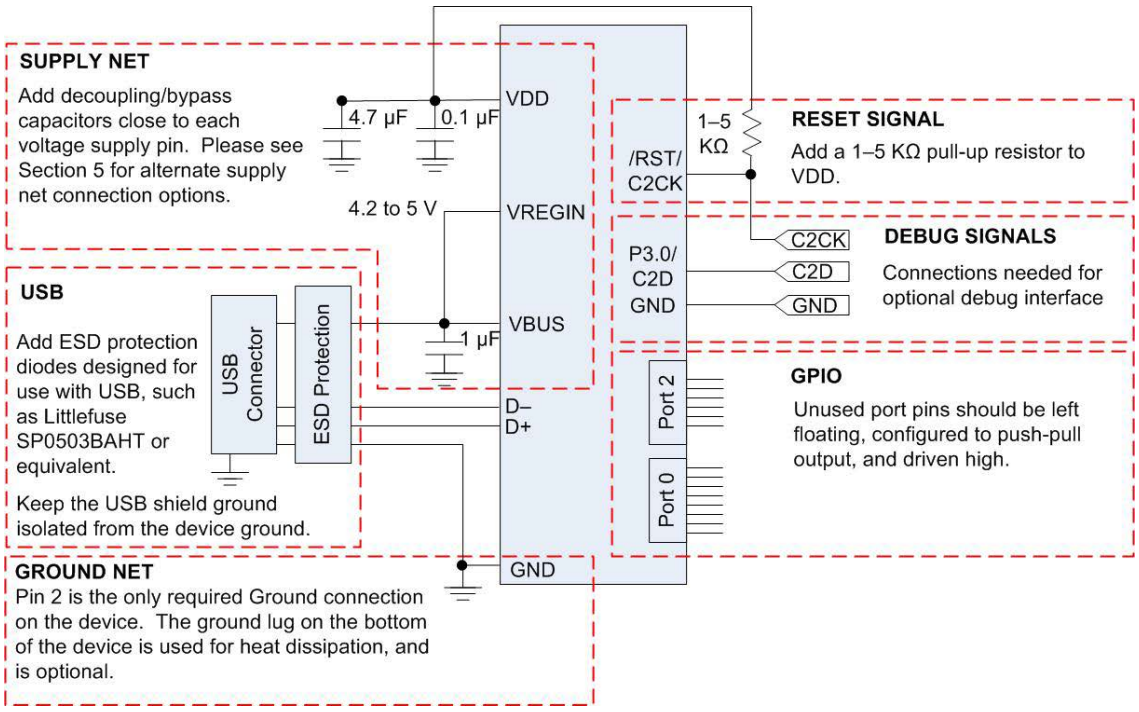

Figure 1.4. Typical Connections for the C8051F327

1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F326/7 family utilizes Silicon Laboratories' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052, including two 16-bit counter/timers, a full-duplex UART with extended baud rate configuration, 1536 bytes of on-chip RAM, 128 byte Special Function Register (SFR) address space, and 15 I/O pins.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. Figure 1.5 shows a comparison of peak throughputs for various 8-bit microcontroller cores with their maximum system clocks.

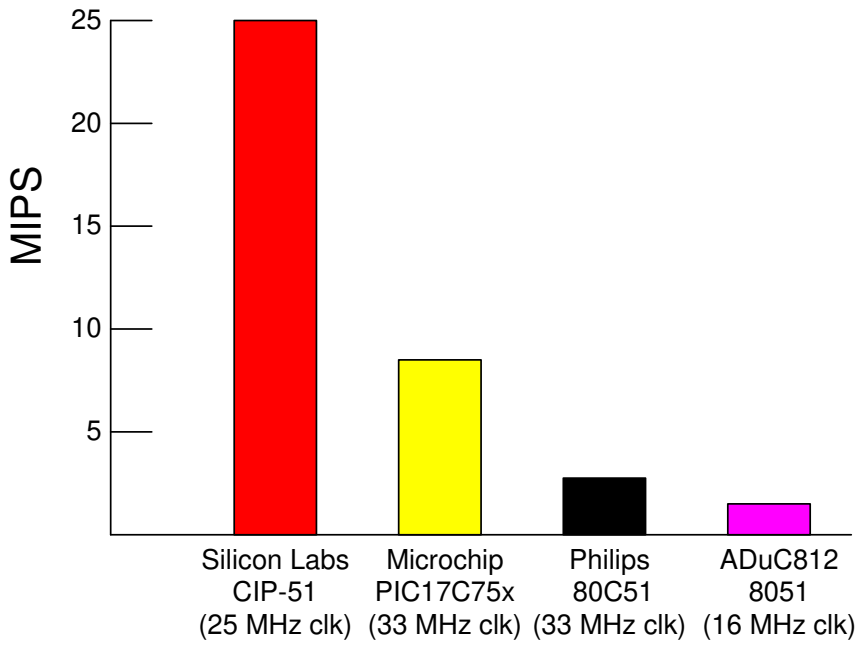

Figure 1.5. Comparison of Peak MCU Execution Speeds

1.1.3. Additional Features

The C8051F326/7 SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides 8 interrupt sources into the CIP-51. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The interrupt sources are very useful when building multi-tasking, real-time systems.

Seven reset sources are available: power-on reset circuitry (POR), an on-chip VDD monitor (forces reset when power supply voltage drops below V_{RST} as given in Table 7.1 on page 62), the USB controller (USB bus reset or a VBUS transition), a Missing Clock Detector, a forced software reset, an external reset pin, and an errant Flash read/write protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software.

The internal oscillator is factory calibrated to 12 MHz ±1.5%, and the internal oscillator period may be user programmed in ~0.25% increments. An additional low-frequency oscillator is also available which facilitates low power operation. A clock recovery mechanism allows the internal oscillator to be used with the 4x Clock Multiplier as the USB clock source in Full Speed mode; the internal oscillator can also be used as the USB clock source in Low Speed mode. An external CMOS clock may also be used with the 4x Clock Multiplier. The system clock may be configured to use the internal oscillator, external clock, low-frequency oscillator, or the Clock Multiplier output divided by 2. If desired, the system clock source may be switched on-the-fly between oscillator sources. The external clock and internal low-frequency oscillator can be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) clock source, while periodically switching to the high-frequency internal oscillator as needed.

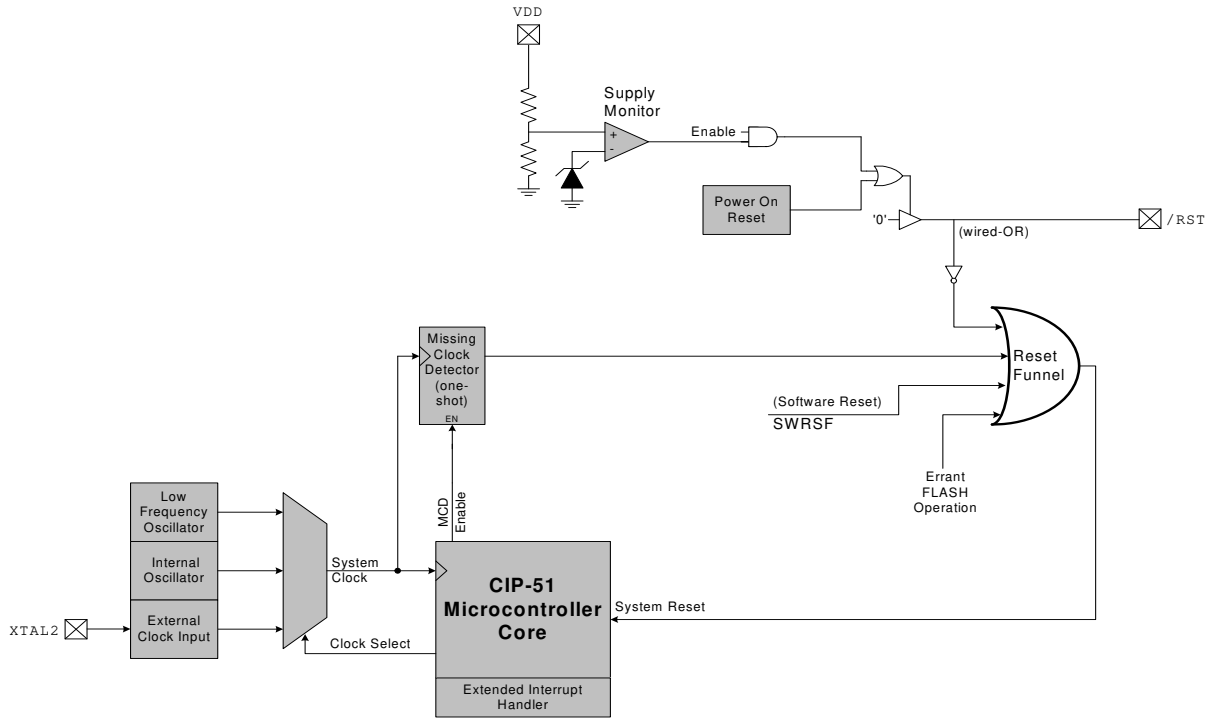

Figure 1.6. On-Chip Clock and Reset

1.2. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

Program memory consists of 16k bytes of Flash. This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. See Figure 1.7 for the MCU system memory map.

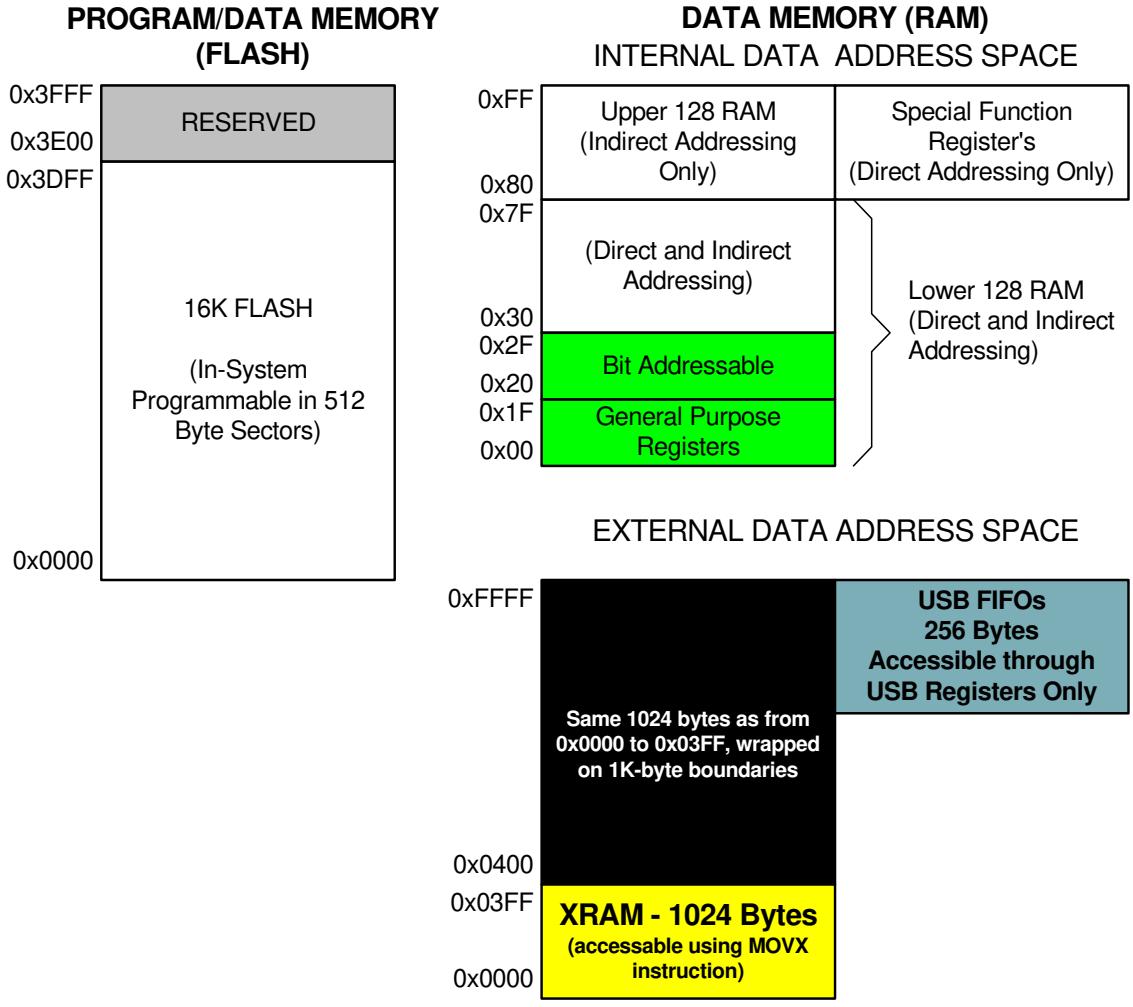

Figure 1.7. On-Board Memory Map

1.3. Universal Serial Bus Controller

The Universal Serial Bus Controller (USB0) is a USB 2.0 peripheral with integrated transceiver and endpoint FIFO RAM. The controller supports both full and low speed modes. A total of three endpoint pipes are available: a bi-directional control endpoint (Endpoint0) and a data endpoint (Endpoint1) with one IN pipe and one OUT pipe.

A 256 block of XRAM is used as dedicated USB FIFO space. This FIFO space is distributed between Endpoint0 and Endpoint1. Endpoint0 is 64 bytes, and Endpoint1 has a 64 byte IN pipe and a 128 byte OUT pipe.

USB0 can be operated as a Full or Low Speed function. The on-chip 4x Clock Multiplier and clock recovery circuitry allow both Full and Low Speed options to be implemented with the on-chip precision oscillator as the USB clock source. An external clock source can also be used with the 4x Clock Multiplier to generate the USB clock.

The USB Transceiver is USB 2.0 compliant, and includes on-chip matching and pullup resistors. The pullup resistors can be enabled/disabled in software, and will appear on the D+ or D– pin according to the software-selected speed setting (full or low speed).

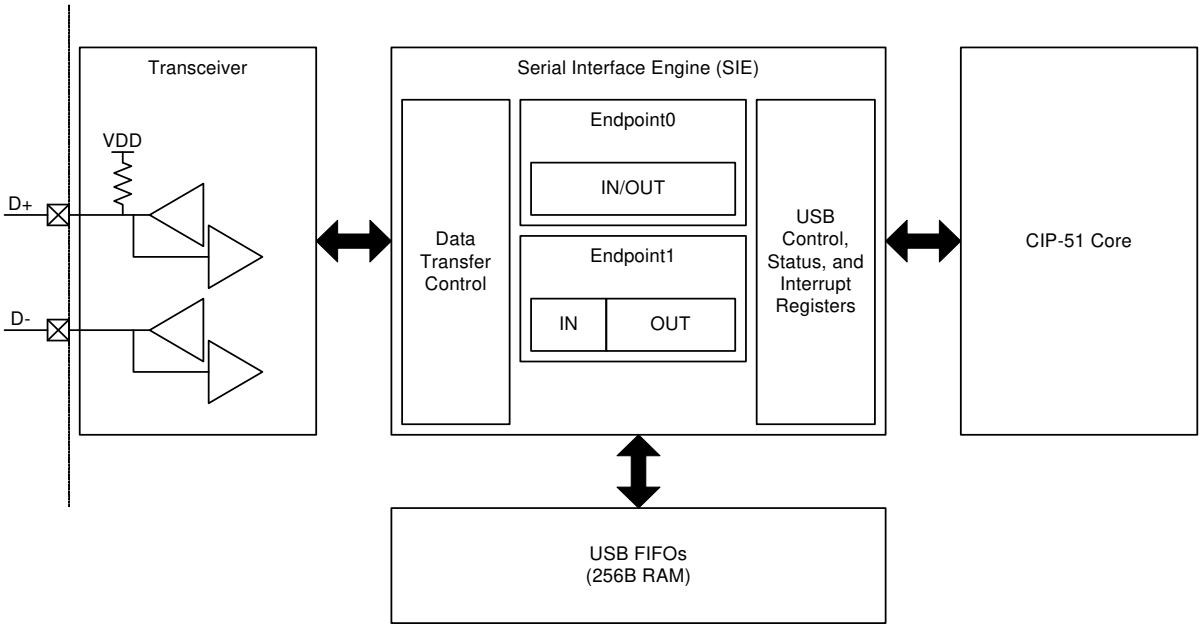

Figure 1.8. USB Controller Block Diagram

1.4. Voltage Regulator

C8051F326/7 devices include a voltage regulator (REG0). When enabled, the REG0 output appears on the VDD pin and can be used to power external devices. REG0 can be enabled/disabled by software.

1.5. On-Chip Debug Circuitry

C8051F326/7 devices include on-chip Silicon Laboratories 2-Wire (C2) debug circuitry that provides non-intrusive, full speed, in-circuit debugging of the production part *installed in the end application.*

The Silicon Laboratories' debugging system supports inspection and modification of memory and registers, breakpoints, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the USB) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F326DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F326/7 MCUs. The kit includes a Windows development environment, a serial adapter for connecting to the C2 port, and a target application board. All of the necessary communication cables and a wall-mount power supply are also supplied with the development kit. The Silicon Laboratories debug environment is a vastly superior configuration for developing and debugging embedded applications compared to standard MCU emulators, which use on-board "ICE Chips" and target cables and require the MCU in the application board to be socketed. The Silicon Laboratories debug environment enhances ease of use and preserves the performance of on-chip peripherals.

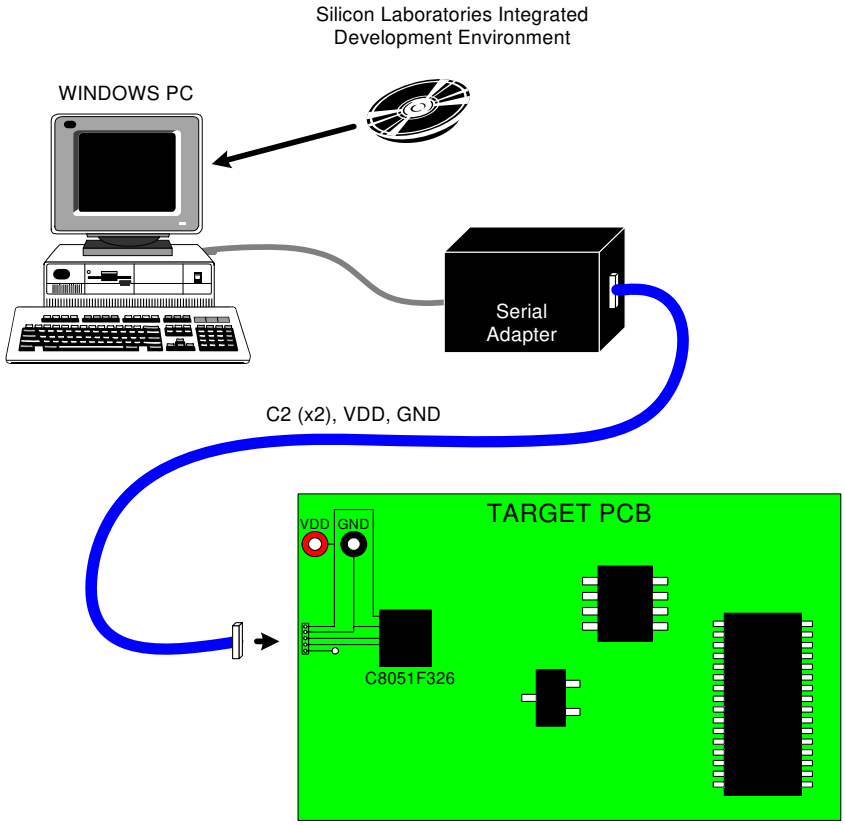

Figure 1.9. Development/In-System Debug Diagram

1.6. Programmable Digital I/O

C8051F326/7 devices include 15 I/O pins (one byte-wide Port, one 6-bit-wide and one 1-bit-wide Port). The C8051F326/7 Ports behave like typical 8051 Ports with a few enhancements. Each Port pin may be configured as a digital input or output pin. Pins selected as digital outputs may additionally be configured for push-pull or open-drain output. The “weak pullups” that are fixed on typical 8051 devices may be globally disabled, providing power savings capabilities.

1.7. Serial Ports

The C8051F326/7 Family includes a full-duplex UART with enhanced baud rate configuration. The serial interface is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.

2. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Ambient Temperature under Bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on any Port I/O Pin or $\overline{\text{RST}}$ with Respect to GND		–0.3	—	5.8	V
Voltage on VDD or VIO with Respect to GND		–0.3	—	4.2	V
Maximum Total Current through VDD, VIO, and GND		—	—	500	mA
Maximum Output Current Sunk by $\overline{\text{RST}}$ or any Port Pin		—	—	100	mA

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3. Global DC Electrical Characteristics

Table 3.1. Global DC Electrical Characteristics

–40 to +85 °C, 25 MHz System Clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
I/O Supply Voltage (VIO)[1,2]		1.8	3.3	3.6	V
Core Supply Voltage (VDD)[3]		2.7	3.3	3.6	V
Core Supply Current with CPU Active	VDD = 3.3 V, Clock = 24 MHz VDD = 3.3 V, Clock = 3 MHz VDD = 3.3 V, Clock = 32 kHz	— — —	11 1.9 20	— — —	mA mA µA
Core Supply Current with CPU Inactive (not accessing Flash)	VDD = 3.3 V, Clock = 24 MHz VDD = 3.3 V, Clock = 3 MHz VDD = 3.3 V, Clock = 32 kHz	— — —	4.4 0.83 13	— — —	mA mA µA
Digital Supply Current (suspend mode or shutdown mode)	Oscillator not running	—	< 0.1	—	µA
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
SYSCLK (System Clock)[4]		0	—	25	MHz
T_{SYSH} (SYSCLK High Time)		18	—	—	ns
T_{SYSL} (SYSCLK Low Time)		18	—	—	ns
Specified Operating Temperature Range		–40	—	+85	°C

Notes:
1. The I/O Supply Voltage (VIO) must be less than or equal to the Core Supply Voltage (VDD).
2. For C8051F327 devices, VIO is internally connected to VDD.
3. USB Requires 3.0 V Minimum Core Supply Voltage (VDD).
4. SYSCLK must be at least 32 kHz to enable debugging.

4. Pinout and Package Definitions

Table 4.1. Pin Definitions for the C8051F326/7

Name	Pin Numbers		Type	Description
	'F326	'F327		
VDD	6	6	Power In Power Out	2.7–3.6 V Core Supply Voltage Input. 3.3 V Voltage Regulator Output. See Section 5.
VIO	5	—	Power In	V I/O Supply Voltage Input. The voltage at this pin must be less than or equal to the Core Supply Voltage (V_{DD}) for the 'F326. On the 'F327, this pin is internally connected to V_{DD}.
GND	2	3		Ground.
$\overline{RST}$/ C2CK	9	9	D I/O D I/O	Device Reset. Open-drain output of internal POR or VDD monitor. An external source can initiate a system reset by driving this pin low for at least 15 µs. See Section 7. Clock signal for the C2 Debug Interface.
P3.0/ C2D	10	10	D I/O D I/O	Port 3.0. See Section 11 for a complete description. Bi-directional data signal for the C2 Debug Interface.
REGIN	7	7	Power In	5 V Regulator Input. This pin is the input to the on-chip voltage regulator.
VBUS	8	8	D In	VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network. A 5 V signal on this pin indicates a USB network connection.
D+	3	4	D I/O	USB D+.
D–	4	5	D I/O	USB D–.
P0.0	1	2	D I/O	Port 0.0. See Section 11 for a complete description.
P0.1	28	1	D I/O	Port 0.1. See Section 11 for a complete description.
P0.2	27	28	D I/O	Port 0.2. See Section 11 for a complete description.
P0.3/ XTAL2	26	27	D I/O D In	Port 0.3. See Section 11 for a complete description. External Clock Input. See Section 10 for a complete description.
P0.4	25	26	D I/O	Port 0.4. See Section 11 for a complete description.
P0.5	24	25	D I/O	Port 0.5. See Section 11 for a complete description.