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### Analog Peripherals

- **10-Bit ADC** ('F330/2/4 only)
  - Up to 200 ksp/s
  - Up to 16 external single-ended or differential inputs
  - VREF from internal VREF, external pin or V<sub>DD</sub>
  - Internal or external start of conversion source
  - Built-in temperature sensor
- **10-Bit Current Output DAC** ('F330 only)
- **Comparator**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source
  - Low current (0.4  $\mu$ A)

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Low cost, **complete** development kit

### Supply Voltage 2.7 to 3.6 V

- Typical operating current: 6.4 mA at 25 MHz;  
9  $\mu$ A at 32 kHz
- Typical stop mode current: 0.1  $\mu$ A

### Temperature Range: -40 to +85 °C

### High Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 768 bytes internal data RAM (256 + 512)
- 8 kB ('F330/1), 4 kB ('F332/3), or 2 kB ('F334/5) Flash; In-system programmable in 512-byte Sectors—512 bytes are reserved in the 8 kB devices

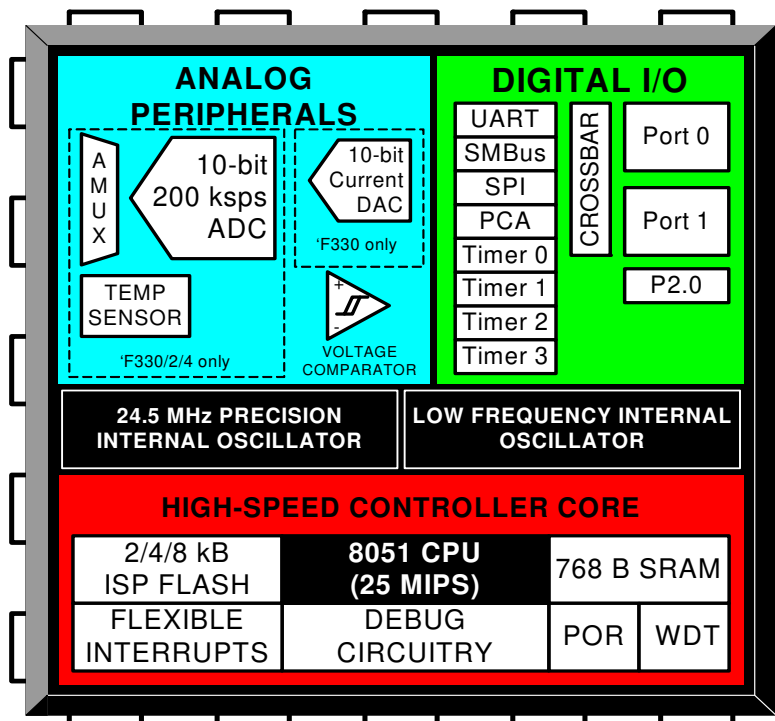
### Digital Peripherals

- 17 Port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART, SMBus™, and enhanced SPI™ serial ports
- Four general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with three capture/compare modules
- Real time clock mode using PCA or timer and external clock source

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz with  $\pm 2\%$  accuracy supports crystal-less UART operation
  - 80/40/20/10 kHz low frequency, low power
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly; useful in power saving modes

### 20-Pin QFN or 20-pin PDIP



# C8051F330/1/2/3/4/5

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## Table of Contents

<b>1. System Overview</b> .....	<b>17</b>
1.1. CIP-51™ Microcontroller Core.....	22
1.1.1. Fully 8051 Compatible.....	22
1.1.2. Improved Throughput.....	22
1.1.3. Additional Features .....	23
1.2. On-Chip Memory.....	24
1.3. On-Chip Debug Circuitry.....	25
1.4. Programmable Digital I/O and Crossbar .....	26
1.5. Serial Ports .....	26
1.6. Programmable Counter Array .....	27
1.7. 10-Bit Analog to Digital Converter.....	28
1.8. Comparators .....	29
1.9. 10-bit Current Output DAC.....	30
<b>2. Absolute Maximum Ratings .....</b>	<b>31</b>
<b>3. Global Electrical Characteristics .....</b>	<b>32</b>
<b>4. Pinout and Package Definitions.....</b>	<b>35</b>
<b>5. 10-Bit ADC (ADC0, C8051F330/2/4 only) .....</b>	<b>43</b>
5.1. Analog Multiplexer .....	43
5.2. Temperature Sensor .....	44
5.3. Modes of Operation .....	45
5.3.1. Starting a Conversion.....	46
5.3.2. Tracking Modes.....	47
5.3.3. Settling Time Requirements .....	48
5.4. Programmable Window Detector .....	53
5.4.1. Window Detector In Single-Ended Mode .....	55
5.4.2. Window Detector In Differential Mode.....	56
<b>6. 10-Bit Current Mode DAC (IDA0, C8051F330 only).....</b>	<b>59</b>
6.1. IDA0 Output Scheduling .....	59
6.1.1. Update Output On-Demand .....	59
6.1.2. Update Output Based on Timer Overflow .....	60
6.1.3. Update Output Based on CNVSTR Edge.....	60
6.2. IDAC Output Mapping.....	60
<b>7. Voltage Reference (C8051F330/2/4 only).....</b>	<b>63</b>
<b>8. Comparator0 .....</b>	<b>67</b>
<b>9. CIP-51 Microcontroller .....</b>	<b>73</b>
9.1. Instruction Set.....	74
9.1.1. Instruction and CPU Timing .....	74
9.1.2. MOVX Instruction and Program Memory .....	74
9.2. Memory Organization.....	78
9.2.1. Program Memory.....	79
9.2.2. Data Memory.....	80
9.2.3. General Purpose Registers .....	80
9.2.4. Bit Addressable Locations.....	80

# C8051F330/1/2/3/4/5

---

9.2.5. Stack .....	80
9.2.6. Special Function Registers.....	81
9.2.7. Register Descriptions .....	85
9.3. Interrupt Handler .....	87
9.3.1. MCU Interrupt Sources and Vectors .....	88
9.3.2. External Interrupts .....	89
9.3.3. Interrupt Priorities .....	89
9.3.4. Interrupt Latency .....	89
9.3.5. Interrupt Register Descriptions.....	91
9.4. Power Management Modes .....	96
9.4.1. Idle Mode.....	96
9.4.2. Stop Mode .....	97
<b>10. Reset Sources.....</b>	<b>99</b>
10.1. Power-On Reset .....	100
10.2. Power-Fail Reset/VDD Monitor .....	100
10.3. External Reset .....	101
10.4. Missing Clock Detector Reset .....	101
10.5. Comparator0 Reset .....	102
10.6. PCA Watchdog Timer Reset .....	102
10.7. Flash Error Reset .....	102
10.8. Software Reset.....	102
<b>11. Flash Memory .....</b>	<b>105</b>
11.1. Programming The Flash Memory .....	105
11.1.1. Flash Lock and Key Functions .....	105
11.1.2. Flash Erase Procedure .....	105
11.1.3. Flash Write Procedure .....	106
11.2. Non-volatile Data Storage .....	106
11.3. Security Options .....	107
11.4. Flash Write and Erase Guidelines .....	109
11.4.1. $V_{DD}$ Maintenance and the $V_{DD}$ monitor .....	109
11.4.2. PSWE Maintenance .....	109
11.4.3. System Clock .....	110
<b>12. External RAM .....</b>	<b>113</b>
<b>13. Oscillators .....</b>	<b>115</b>
13.1. Programmable Internal High-Frequency (H-F) Oscillator .....	115
13.2. Programmable Internal Low-Frequency (L-F) Oscillator .....	117
13.2.1. Calibrating the Internal L-F Oscillator.....	117
13.3. External Oscillator Drive Circuit.....	118
13.3.1. External Crystal Example.....	120
13.3.2. External RC Example.....	122
13.3.3. External Capacitor Example.....	122
13.4. System Clock Selection.....	123
<b>14. Port Input/Output.....</b>	<b>125</b>
14.1. Priority Crossbar Decoder .....	127
14.2. Port I/O Initialization .....	129

---



---

14.3.General Purpose Port I/O .....	131
<b>15.SMBus .....</b>	<b>137</b>
15.1.Supporting Documents .....	138
15.2.SMBus Configuration.....	138
15.3.SMBus Operation .....	138
15.3.1.Arbitration.....	139
15.3.2.Clock Low Extension.....	140
15.3.3.SCL Low Timeout.....	140
15.3.4.SCL High (SMBus Free) Timeout .....	140
15.4.Using the SMBus.....	140
15.4.1.SMBus Configuration Register.....	142
15.4.2.SMB0CN Control Register .....	145
15.4.3.Data Register .....	148
15.5.SMBus Transfer Modes.....	148
15.5.1.Master Transmitter Mode .....	148
15.5.2.Master Receiver Mode .....	150
15.5.3.Slave Receiver Mode .....	151
15.5.4.Slave Transmitter Mode .....	152
15.6.SMBus Status Decoding.....	152
<b>16.UART0.....</b>	<b>155</b>
16.1.Enhanced Baud Rate Generation.....	156
16.2.Operational Modes .....	157
16.2.1.8-Bit UART .....	157
16.2.2.9-Bit UART .....	158
16.3.Multiprocessor Communications .....	158
<b>17.Enhanced Serial Peripheral Interface (SPI0).....</b>	<b>165</b>
17.1.Signal Descriptions.....	166
17.1.1.Master Out, Slave In (MOSI).....	166
17.1.2.Master In, Slave Out (MISO).....	166
17.1.3.Serial Clock (SCK) .....	166
17.1.4.Slave Select (NSS) .....	166
17.2.SPI0 Master Mode Operation .....	167
17.3.SPI0 Slave Mode Operation .....	169
17.4.SPI0 Interrupt Sources .....	169
17.5.Serial Clock Timing.....	170
17.6.SPI Special Function Registers .....	171
<b>18.Timers.....</b>	<b>179</b>
18.1.Timer 0 and Timer 1 .....	179
18.1.1.Mode 0: 13-bit Counter/Timer .....	179
18.1.2.Mode 1: 16-bit Counter/Timer .....	180
18.1.3.Mode 2: 8-bit Counter/Timer with Auto-Reload.....	181
18.1.4.Mode 3: Two 8-bit Counter/Timers (Timer 0 Only).....	182
18.2.Timer 2 .....	187
18.2.1.16-bit Timer with Auto-Reload.....	187

# C8051F330/1/2/3/4/5

---

18.2.2.8-bit Timers with Auto-Reload.....	188
18.3.Timer 3 .....	191
18.3.1.16-bit Timer with Auto-Reload.....	191
18.3.2.8-bit Timers with Auto-Reload.....	192
<b>19. Programmable Counter Array .....</b>	<b>195</b>
19.1.PCA Counter/Timer .....	196
19.2.Capture/Compare Modules .....	197
19.2.1.Edge-triggered Capture Mode.....	198
19.2.2.Software Timer (Compare) Mode.....	199
19.2.3.High-Speed Output Mode .....	200
19.2.4.Frequency Output Mode .....	201
19.2.5.8-Bit Pulse Width Modulator Mode.....	202
19.2.6.16-Bit Pulse Width Modulator Mode.....	203
19.3.Watchdog Timer Mode .....	203
19.3.1.Watchdog Timer Operation .....	204
19.3.2.Watchdog Timer Usage .....	205
19.4.Register Descriptions for PCA.....	206
<b>20. C2 Interface .....</b>	<b>211</b>
20.1.C2 Interface Registers.....	211
20.2.C2 Pin Sharing .....	213
<b>Document Change List .....</b>	<b>214</b>
<b>Contact Information .....</b>	<b>216</b>

## List of Figures

### 1. System Overview

Figure 1.1. C8051F330 Block Diagram.....	19
Figure 1.2. C8051F331 Block Diagram.....	19
Figure 1.3. C8051F332 Block Diagram.....	20
Figure 1.4. C8051F333 Block Diagram.....	20
Figure 1.5. C8051F334 Block Diagram.....	21
Figure 1.6. C8051F335 Block Diagram.....	21
Figure 1.7. Comparison of Peak MCU Execution Speeds .....	22
Figure 1.8. On-Chip Clock and Reset.....	23
Figure 1.9. On-Board Memory Map .....	24
Figure 1.10. Development/In-System Debug Diagram.....	25
Figure 1.11. Digital Crossbar Diagram .....	26
Figure 1.12. PCA Block Diagram.....	27
Figure 1.13. PCA Block Diagram.....	27
Figure 1.14. 10-Bit ADC Block Diagram.....	28
Figure 1.15. Comparator0 Block Diagram.....	29
Figure 1.16. IDA0 Functional Block Diagram .....	30

### 2. Absolute Maximum Ratings

### 3. Global Electrical Characteristics

### 4. Pinout and Package Definitions

Figure 4.1. QFN-20 Pinout Diagram (Top View).....	37
Figure 4.2. PDIP-20 Pinout Diagram (Top View).....	40
Figure 4.3. PDIP-20 Package Drawing .....	41

### 5. 10-Bit ADC (ADC0, C8051F330/2/4 only)

Figure 5.1. ADC0 Functional Block Diagram .....	43
Figure 5.2. Typical Temperature Sensor Transfer Function .....	45
Figure 5.3. 10-Bit ADC Track and Conversion Example Timing.....	47
Figure 5.4. ADC0 Equivalent Input Circuits .....	48
Figure 5.5. ADC Window Compare Example: Right-Justified Single-Ended Data... 55	
Figure 5.6. ADC Window Compare Example: Left-Justified Single-Ended Data .....	55
Figure 5.7. ADC Window Compare Example: Right-Justified Differential Data .....	56
Figure 5.8. ADC Window Compare Example: Left-Justified Differential Data .....	56

### 6. 10-Bit Current Mode DAC (IDA0, C8051F330 only)

Figure 6.1. IDA0 Functional Block Diagram.....	59
Figure 6.2. IDA0 Data Word Mapping.....	60

### 7. Voltage Reference (C8051F330/2/4 only)

Figure 7.1. Voltage Reference Functional Block Diagram .....	63
--	----

### 8. Comparator0

Figure 8.1. Comparator0 Functional Block Diagram.....	67
Figure 8.2. Comparator Hysteresis Plot.....	68

### 9. CIP-51 Microcontroller

Figure 9.1. CIP-51 Block Diagram .....	73
Figure 9.2. Memory Map.....	79



# C8051F330/1/2/3/4/5

---

## 10. Reset Sources

Figure 10.1. Reset Sources.....	99
Figure 10.2. Power-On and VDD Monitor Reset Timing .....	100

## 11. Flash Memory

Figure 11.1. Flash Program Memory Map.....	107
--	-----

## 12. External RAM

## 13. Oscillators

Figure 13.1. Oscillator Diagram.....	115
Figure 13.2. External 32.768 kHz Quartz Crystal Oscillator Connection Diagram .	121

## 14. Port Input/Output

Figure 14.1. Port I/O Functional Block Diagram.....	125
Figure 14.2. Port I/O Cell Block Diagram .....	126
Figure 14.3. Crossbar Priority Decoder with No Pins Skipped .....	127
Figure 14.4. Crossbar Priority Decoder with Crystal Pins Skipped .....	128

## 15. SMBus

Figure 15.1. SMBus Block Diagram .....	137
Figure 15.2. Typical SMBus Configuration .....	138
Figure 15.3. SMBus Transaction .....	139
Figure 15.4. Typical SMBus SCL Generation.....	143
Figure 15.5. Typical Master Transmitter Sequence.....	149
Figure 15.6. Typical Master Receiver Sequence.....	150
Figure 15.7. Typical Slave Receiver Sequence.....	151
Figure 15.8. Typical Slave Transmitter Sequence.....	152

## 16. UART0

Figure 16.1. UART0 Block Diagram .....	155
Figure 16.2. UART0 Baud Rate Logic.....	156
Figure 16.3. UART Interconnect Diagram .....	157
Figure 16.4. 8-Bit UART Timing Diagram.....	157
Figure 16.5. 9-Bit UART Timing Diagram.....	158
Figure 16.6. UART Multi-Processor Mode Interconnect Diagram .....	159

## 17. Enhanced Serial Peripheral Interface (SPI0)

Figure 17.1. SPI Block Diagram .....	165
Figure 17.2. Multiple-Master Mode Connection Diagram .....	168
Figure 17.3. 3-Wire Single Master and 3-Wire Single Slave Mode Connection Diagram 168	
Figure 17.4. 4-Wire Single Master Mode and 4-Wire Slave Mode Connection Diagram 168	
Figure 17.5. Master Mode Data/Clock Timing .....	170
Figure 17.6. Slave Mode Data/Clock Timing (CKPHA = 0) .....	171
Figure 17.7. Slave Mode Data/Clock Timing (CKPHA = 1) .....	171
Figure 17.8. SPI Master Timing (CKPHA = 0) .....	175
Figure 17.9. SPI Master Timing (CKPHA = 1) .....	175
Figure 17.10. SPI Slave Timing (CKPHA = 0) .....	176
Figure 17.11. SPI Slave Timing (CKPHA = 1) .....	176

## 18. Timers

---

---

Figure 18.1. T0 Mode 0 Block Diagram.....	180
Figure 18.2. T0 Mode 2 Block Diagram.....	181
Figure 18.3. T0 Mode 3 Block Diagram.....	182
Figure 18.4. Timer 2 16-Bit Mode Block Diagram .....	187
Figure 18.5. Timer 2 8-Bit Mode Block Diagram .....	188
Figure 18.6. Timer 3 16-Bit Mode Block Diagram .....	191
Figure 18.7. Timer 3 8-Bit Mode Block Diagram .....	192
<b>19. Programmable Counter Array</b>	
Figure 19.1. PCA Block Diagram.....	195
Figure 19.2. PCA Counter/Timer Block Diagram.....	196
Figure 19.3. PCA Interrupt Block Diagram .....	197
Figure 19.4. PCA Capture Mode Diagram.....	198
Figure 19.5. PCA Software Timer Mode Diagram .....	199
Figure 19.6. PCA High-Speed Output Mode Diagram.....	200
Figure 19.7. PCA Frequency Output Mode .....	201
Figure 19.8. PCA 8-Bit PWM Mode Diagram .....	202
Figure 19.9. PCA 16-Bit PWM Mode.....	203
Figure 19.10. PCA Module 2 with Watchdog Timer Enabled .....	204
<b>20. C2 Interface</b>	
Figure 20.1. Typical C2 Pin Sharing.....	213

# C8051F330/1/2/3/4/5

---



---

## List of Tables

<b>1. System Overview</b>	
Table 1.1. Product Selection Guide .....	18
<b>2. Absolute Maximum Ratings</b>	
Table 2.1. Absolute Maximum Ratings .....	31
<b>3. Global Electrical Characteristics</b>	
Table 3.1. Global Electrical Characteristics .....	32
Table 3.2. Index to Electrical Characteristics Tables .....	34
<b>4. Pinout and Package Definitions</b>	
Table 4.1. Pin Definitions for the C8051F330/1/2/3/4/5 .....	35
Table 4.2. QFN-20 Package Dimensions .....	38
Table 4.3. QFN-20 PCB Land Pattern Dimensions .....	39
Table 4.4. PDIP-20 Package Dimensions .....	41
<b>5. 10-Bit ADC (ADC0, C8051F330/2/4 only)</b>	
Table 5.1. ADC0 Electrical Characteristics .....	57
<b>6. 10-Bit Current Mode DAC (IDA0, C8051F330 only)</b>	
Table 6.1. IDAC Electrical Characteristics .....	62
<b>7. Voltage Reference (C8051F330/2/4 only)</b>	
Table 7.1. Voltage Reference Electrical Characteristics .....	65
<b>8. Comparator0</b>	
Table 8.1. Comparator Electrical Characteristics .....	72
<b>9. CIP-51 Microcontroller</b>	
Table 9.1. CIP-51 Instruction Set Summary .....	75
Table 9.2. Special Function Register (SFR) Memory Map .....	81
Table 9.3. Special Function Registers .....	82
Table 9.4. Interrupt Summary .....	90
<b>10. Reset Sources</b>	
Table 10.1. Reset Electrical Characteristics .....	104
<b>11. Flash Memory</b>	
Table 11.1. Flash Electrical Characteristics .....	106
Table 11.2. Flash Security Summary .....	108
<b>12. External RAM</b>	
<b>13. Oscillators</b>	
Table 13.1. Internal Oscillator Electrical Characteristics .....	124
<b>14. Port Input/Output</b>	
Table 14.1. Port I/O DC Electrical Characteristics .....	136
<b>15. SMBus</b>	
Table 15.1. SMBus Clock Source Selection .....	142
Table 15.2. Minimum SDA Setup and Hold Times .....	143
Table 15.3. Sources for Hardware Changes to SMB0CN .....	147
Table 15.4. SMBus Status Decoding .....	153
<b>16. UART0</b>	
Table 16.1. Timer Settings for Standard Baud Rates Using The Internal 24.5 MHz Os-	

# C8051F330/1/2/3/4/5

---

cillator .....	162
Table 16.2. Timer Settings for Standard Baud Rates Using an External 25.0 MHz Oscillator .....	162
Table 16.3. Timer Settings for Standard Baud Rates Using an External 22.1184 MHz Oscillator.....	163
Table 16.4. Timer Settings for Standard Baud Rates Using an External 18.432 MHz Oscillator.....	163
Table 16.5. Timer Settings for Standard Baud Rates Using an External 11.0592 MHz Oscillator.....	164
Table 16.6. Timer Settings for Standard Baud Rates Using an External 3.6864 MHz Oscillator.....	164
<b>17. Enhanced Serial Peripheral Interface (SPI0)</b>	
Table 17.1. SPI Slave Timing Parameters .....	177
<b>18. Timers</b>	
<b>19. Programmable Counter Array</b>	
Table 19.1. PCA Timebase Input Options .....	196
Table 19.2. PCA0CPM Register Settings for PCA Capture/Compare Modules ....	197
Table 19.3. Watchdog Timer Timeout Intervals1.....	206

## List of Registers

SFR Definition 5.1. AMX0P: AMUX0 Positive Channel Select .....	49
SFR Definition 5.2. AMX0N: AMUX0 Negative Channel Select .....	50
SFR Definition 5.3. ADC0CF: ADC0 Configuration .....	51
SFR Definition 5.4. ADC0H: ADC0 Data Word MSB .....	51
SFR Definition 5.5. ADC0L: ADC0 Data Word LSB .....	51
SFR Definition 5.6. ADC0CN: ADC0 Control .....	52
SFR Definition 5.7. ADC0GTH: ADC0 Greater-Than Data High Byte .....	53
SFR Definition 5.8. ADC0GTL: ADC0 Greater-Than Data Low Byte .....	53
SFR Definition 5.9. ADC0LTH: ADC0 Less-Than Data High Byte .....	54
SFR Definition 5.10. ADC0LTL: ADC0 Less-Than Data Low Byte .....	54
SFR Definition 6.1. IDA0CN: IDA0 Control .....	61
SFR Definition 6.2. IDA0H: IDA0 Data Word MSB .....	61
SFR Definition 6.3. IDA0L: IDA0 Data Word LSB .....	62
SFR Definition 7.1. REF0CN: Reference Control .....	64
SFR Definition 8.1. CPT0CN: Comparator0 Control .....	69
SFR Definition 8.2. CPT0MX: Comparator0 MUX Selection .....	70
SFR Definition 8.3. CPT0MD: Comparator0 Mode Selection .....	71
SFR Definition 9.1. DPL: Data Pointer Low Byte .....	85
SFR Definition 9.2. DPH: Data Pointer High Byte .....	85
SFR Definition 9.3. SP: Stack Pointer .....	85
SFR Definition 9.4. PSW: Program Status Word .....	86
SFR Definition 9.5. ACC: Accumulator .....	87
SFR Definition 9.6. B: B Register .....	87
SFR Definition 9.7. IE: Interrupt Enable .....	91
SFR Definition 9.8. IP: Interrupt Priority .....	92
SFR Definition 9.9. EIE1: Extended Interrupt Enable 1 .....	93
SFR Definition 9.10. EIP1: Extended Interrupt Priority 1 .....	94
SFR Definition 9.11. IT01CF: INT0/INT1 Configuration .....	95
SFR Definition 9.12. PCON: Power Control .....	97
SFR Definition 10.1. VDM0CN: VDD Monitor Control .....	101
SFR Definition 10.2. RSTSRC: Reset Source .....	103
SFR Definition 11.1. PSCTL: Program Store R/W Control .....	110
SFR Definition 11.2. FLKEY: Flash Lock and Key .....	111
SFR Definition 11.3. FLSCL: Flash Scale .....	111
SFR Definition 12.1. EMI0CN: External Memory Interface Control .....	113
SFR Definition 13.1. OSCICL: Internal H-F Oscillator Calibration .....	116
SFR Definition 13.2. OSCICN: Internal H-F Oscillator Control .....	116
SFR Definition 13.3. OSCLCN: Internal L-F Oscillator Control .....	117
SFR Definition 13.4. OSCXCN: External Oscillator Control .....	119
SFR Definition 13.5. CLKSEL: Clock Select .....	123
SFR Definition 14.1. XBR0: Port I/O Crossbar Register 0 .....	130
SFR Definition 14.2. XBR1: Port I/O Crossbar Register 1 .....	131
SFR Definition 14.3. P0: Port0 .....	132



# C8051F330/1/2/3/4/5

---

SFR Definition 14.4. P0MDIN: Port0 Input Mode	132
SFR Definition 14.5. P0MDOUT: Port0 Output Mode	133
SFR Definition 14.6. P0SKIP: Port0 Skip	133
SFR Definition 14.7. P1: Port1	133
SFR Definition 14.8. P1MDIN: Port1 Input Mode	134
SFR Definition 14.9. P1MDOUT: Port1 Output Mode	134
SFR Definition 14.10. P1SKIP: Port1 Skip	134
SFR Definition 14.11. P2: Port2	135
SFR Definition 14.12. P2MDOUT: Port2 Output Mode	135
SFR Definition 15.1. SMB0CF: SMBus Clock/Configuration	144
SFR Definition 15.2. SMB0CN: SMBus Control	146
SFR Definition 15.3. SMB0DAT: SMBus Data	148
SFR Definition 16.1. SCON0: Serial Port 0 Control	160
SFR Definition 16.2. SBUF0: Serial (UART0) Port Data Buffer	161
SFR Definition 17.1. SPI0CFG: SPI0 Configuration	172
SFR Definition 17.2. SPI0CN: SPI0 Control	173
SFR Definition 17.3. SPI0CKR: SPI0 Clock Rate	174
SFR Definition 17.4. SPI0DAT: SPI0 Data	174
SFR Definition 18.1. TCON: Timer Control	183
SFR Definition 18.2. TMOD: Timer Mode	184
SFR Definition 18.3. CKCON: Clock Control	185
SFR Definition 18.4. TL0: Timer 0 Low Byte	186
SFR Definition 18.5. TL1: Timer 1 Low Byte	186
SFR Definition 18.6. TH0: Timer 0 High Byte	186
SFR Definition 18.7. TH1: Timer 1 High Byte	186
SFR Definition 18.8. TMR2CN: Timer 2 Control	189
SFR Definition 18.9. TMR2RLL: Timer 2 Reload Register Low Byte	190
SFR Definition 18.10. TMR2RLH: Timer 2 Reload Register High Byte	190
SFR Definition 18.11. TMR2L: Timer 2 Low Byte	190
SFR Definition 18.12. TMR2H: Timer 2 High Byte	190
SFR Definition 18.13. TMR3CN: Timer 3 Control	193
SFR Definition 18.14. TMR3RLL: Timer 3 Reload Register Low Byte	194
SFR Definition 18.15. TMR3RLH: Timer 3 Reload Register High Byte	194
SFR Definition 18.16. TMR3L: Timer 3 Low Byte	194
SFR Definition 18.17. TMR3H: Timer 3 High Byte	194
SFR Definition 19.1. PCA0CN: PCA Control	207
SFR Definition 19.2. PCA0MD: PCA Mode	208
SFR Definition 19.3. PCA0CPMn: PCA Capture/Compare Mode	209
SFR Definition 19.4. PCA0L: PCA Counter/Timer Low Byte	210
SFR Definition 19.5. PCA0H: PCA Counter/Timer High Byte	210
SFR Definition 19.6. PCA0CPLn: PCA Capture Module Low Byte	210
SFR Definition 19.7. PCA0CPHn: PCA Capture Module High Byte	210
C2 Register Definition 20.1. C2ADD: C2 Address	211
C2 Register Definition 20.2. DEVICEID: C2 Device ID	211
C2 Register Definition 20.3. REVID: C2 Revision ID	212

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# C8051F330/1/2/3/4/5

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C2 Register Definition 20.4. FPCTL: C2 Flash Programming Control .....	212
C2 Register Definition 20.5. FPDAT: C2 Flash Programming Data .....	212

# C8051F330/1/2/3/4/5

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## 1. System Overview

C8051F330/1/2/3/4/5 devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 10-bit 200 ksps 16-channel single-ended/differential ADC with analog multiplexer
- 10-bit Current Output DAC
- Precision programmable 25 MHz internal oscillator
- Up to 8 kB of on-chip Flash memory—512 bytes are reserved
- 768 bytes of on-chip RAM
- SMBus/I2C, Enhanced UART, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with three capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset,  $V_{DD}$  Monitor, and Temperature Sensor
- On-chip Voltage Comparator
- 17 Port I/O (5 V tolerant)

With on-chip Power-On Reset,  $V_{DD}$  monitor, Watchdog Timer, and clock oscillator, the C8051F330/1/2/3/4/5 devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 2.7 to 3.6 V operation over the industrial temperature range (–40 to +85 °C). The Port I/O and RST pins are tolerant of input signals up to 5 V. The C8051F330/1/2/3/4/5 are available in 20-pin QFN packages (also referred to as MLP or MLF packages) and the C8051F330 is available in a 20-pin PDIP package. Lead-free (RoHS compliant) packages are also available. See Table 1.1 for ordering part numbers. Block diagrams are included in Figure 1.1, Figure 1.2, Figure 1.3, Figure 1.4, Figure 1.5, and Figure 1.6.

# C8051F330/1/2/3/4/5

**Table 1.1. Product Selection Guide**

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)	RAM (bytes)	Calibrated Internal 24.5 MHz Oscillator	Internal 80 kHz Oscillator	SMBus/I <sup>2</sup> C	Enhanced SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 200kps ADC	10-bit Current Output DAC	Internal Voltage Reference	Temperature Sensor	Analog Comparator	Lead-free (RoHS Compliant)	Package
C8051F330-GM	25	8	768	✓	✓	✓	✓	✓	4	✓	17	✓	✓	✓	✓	✓	✓	QFN-20
C8051F330-GP	25	8	768	✓	✓	✓	✓	✓	4	✓	17	✓	✓	✓	✓	✓	✓	PDIP-20
C8051F331-GM	25	8	768	✓	✓	✓	✓	✓	4	✓	17	—	—	—	—	✓	✓	QFN-20
C8051F332-GM	25	4	768	✓	✓	✓	✓	✓	4	✓	17	✓	—	✓	✓	✓	✓	QFN-20
C8051F333-GM	25	4	768	✓	✓	✓	✓	✓	4	✓	17	—	—	—	—	✓	✓	QFN-20
C8051F334-GM	25	2	768	✓	✓	✓	✓	✓	4	✓	17	✓	—	✓	✓	✓	✓	QFN-20
C8051F335-GM	25	2	768	✓	✓	✓	✓	✓	4	✓	17	—	—	—	—	✓	✓	QFN-20

# C8051F330/1/2/3/4/5

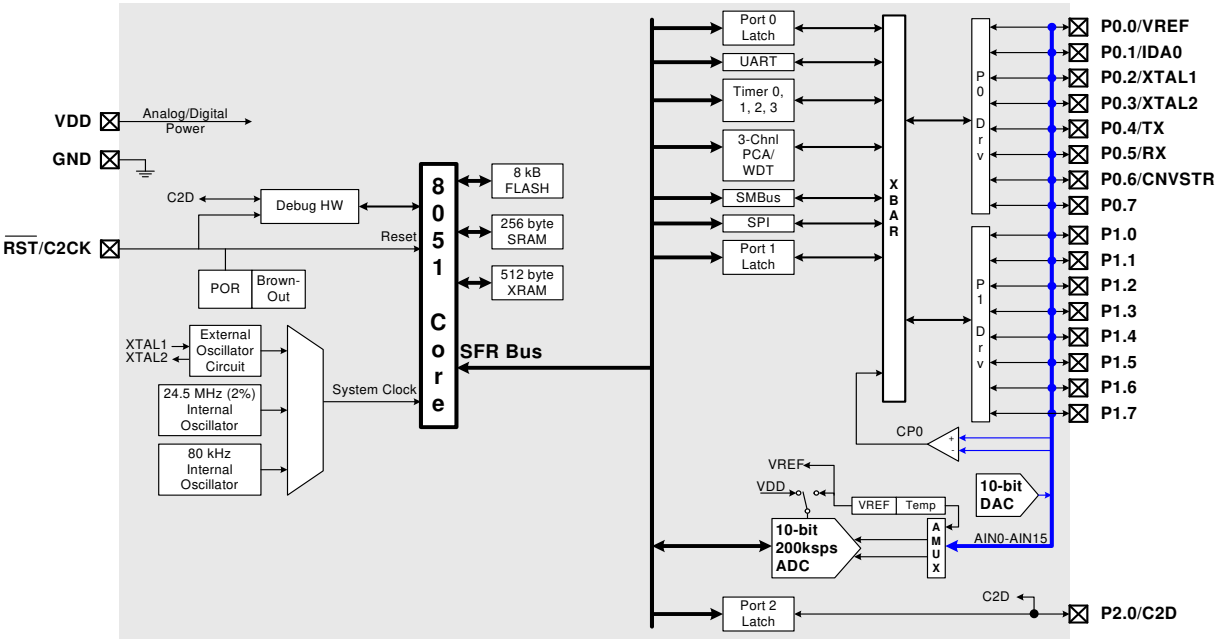


Figure 1.1. C8051F330 Block Diagram

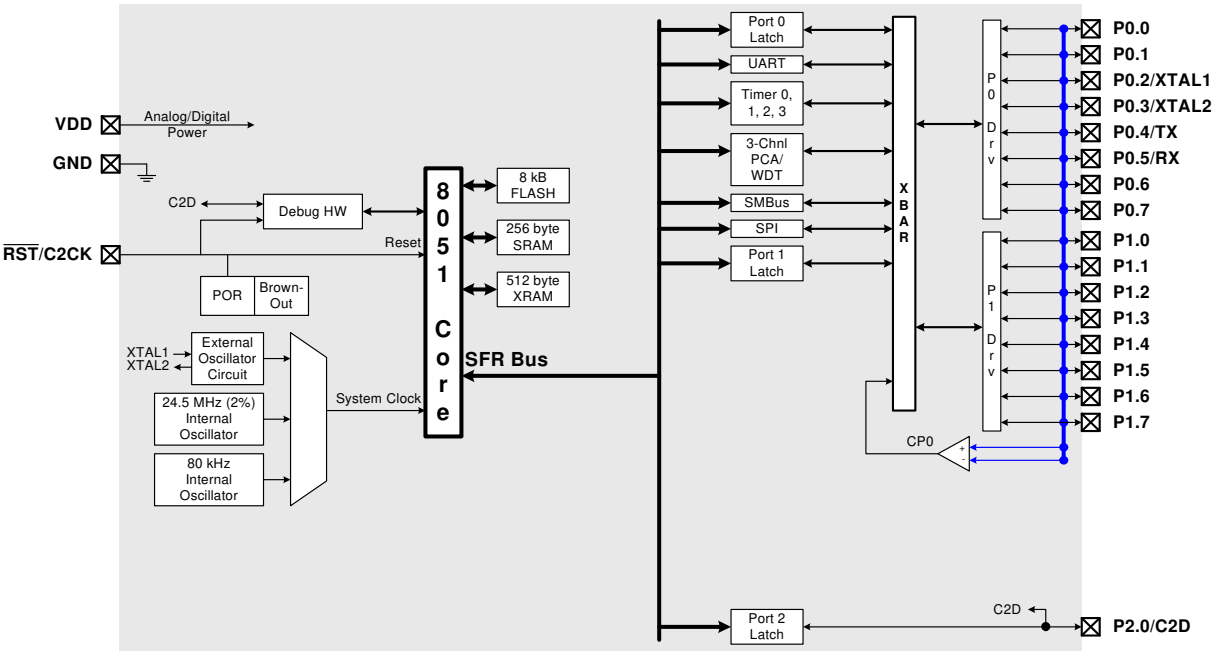


Figure 1.2. C8051F331 Block Diagram



# C8051F330/1/2/3/4/5

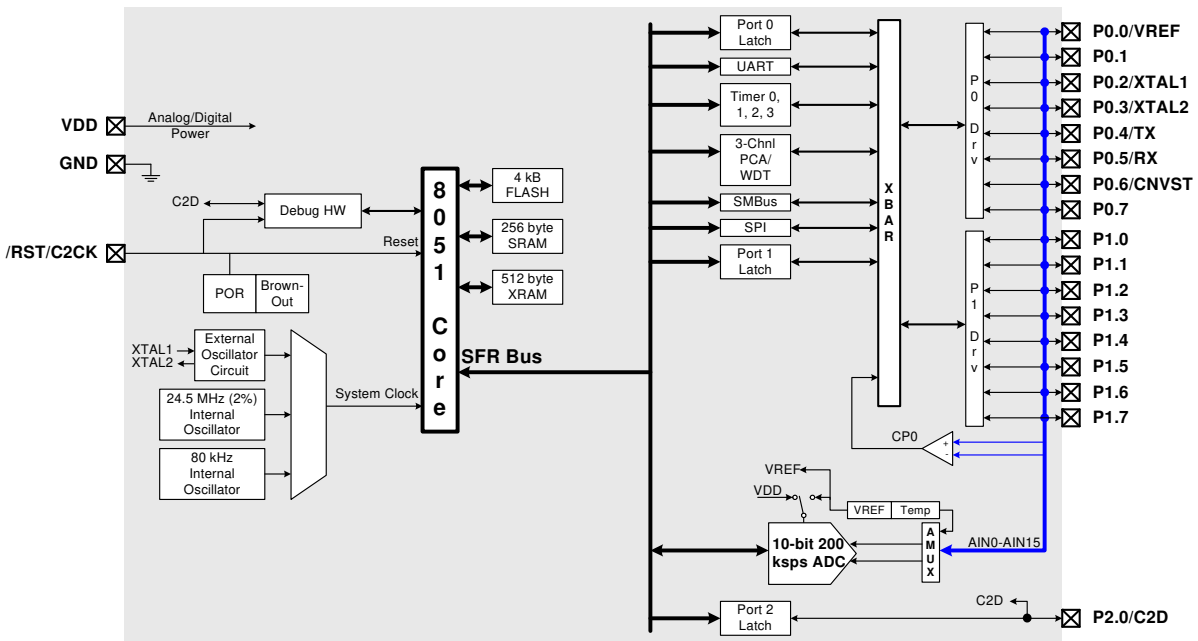


Figure 1.3. C8051F332 Block Diagram

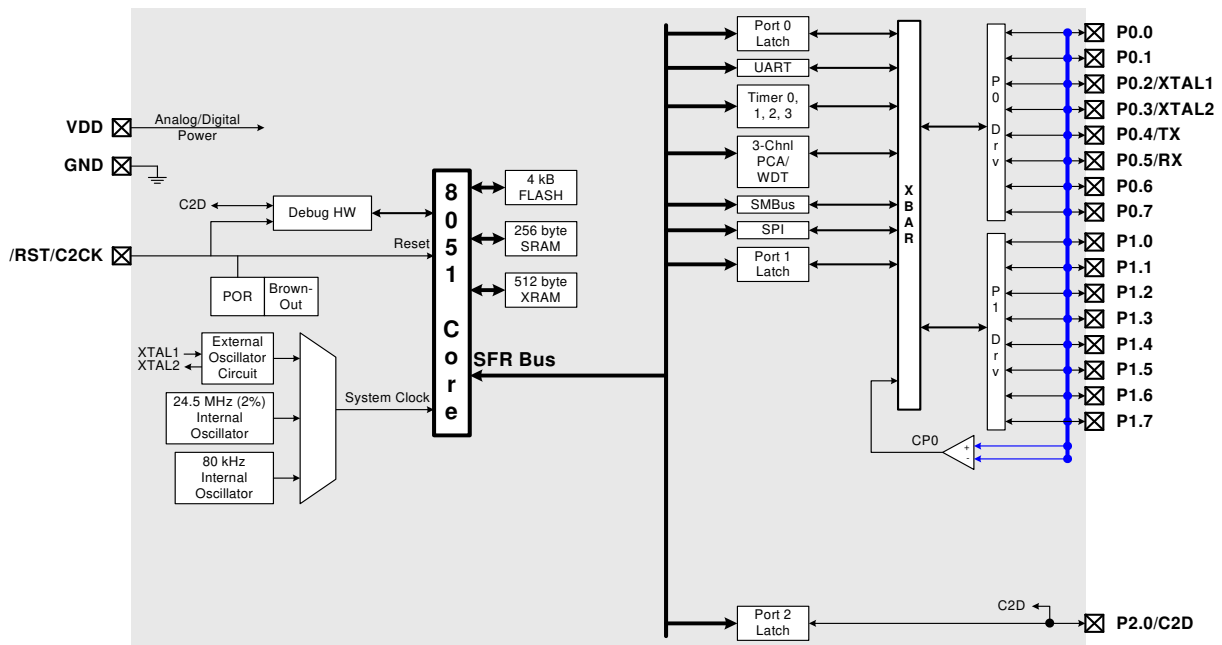


Figure 1.4. C8051F333 Block Diagram

# C8051F330/1/2/3/4/5

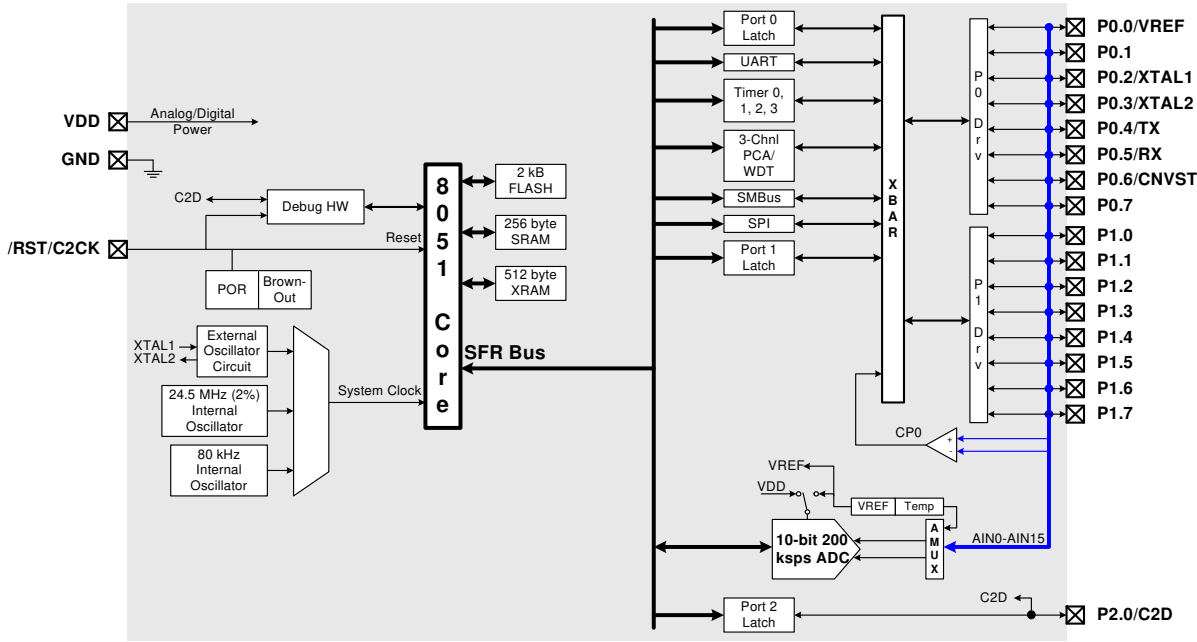


Figure 1.5. C8051F334 Block Diagram

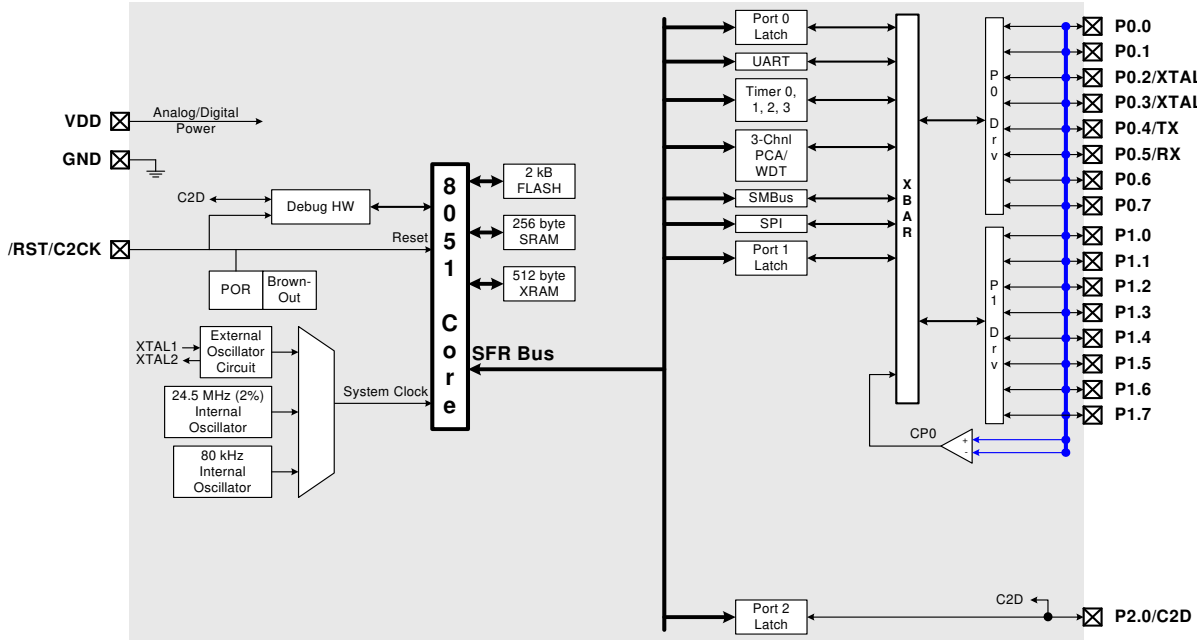


Figure 1.6. C8051F335 Block Diagram

# C8051F330/1/2/3/4/5

## 1.1. CIP-51™ Microcontroller Core

### 1.1.1. Fully 8051 Compatible

The C8051F330/1/2/3/4/5 family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052, including four 16-bit counter/timers, a full-duplex UART with extended baud rate configuration, an enhanced SPI port, 768 bytes of internal RAM, 128 byte Special Function Register (SFR) address space, and 17 I/O pins.

### 1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. Figure 1.7 shows a comparison of peak throughputs for various 8-bit microcontroller cores with their maximum system clocks.

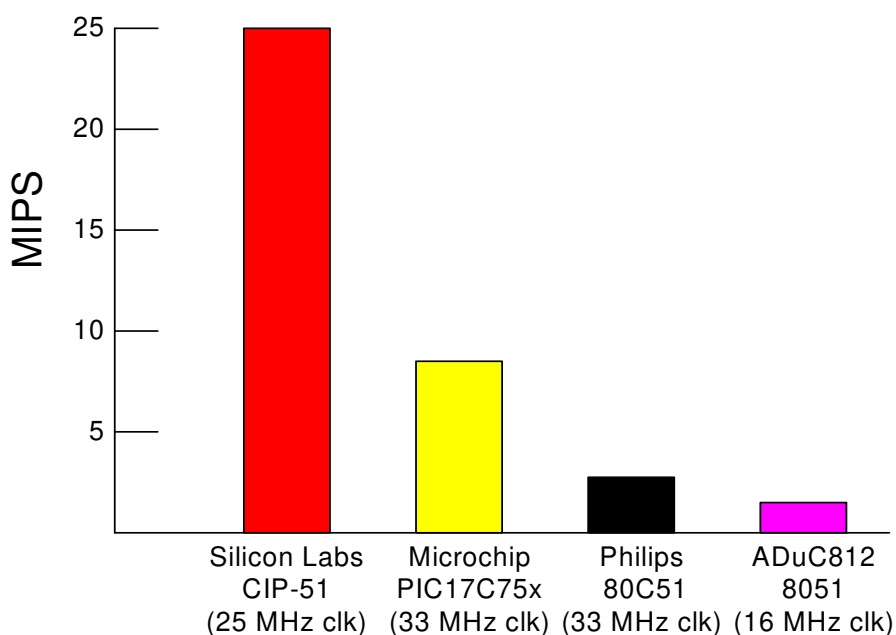


Figure 1.7. Comparison of Peak MCU Execution Speeds

## 1.1.3. Additional Features

The C8051F330/1/2/3/4/5 SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides 14 interrupt sources into the CIP-51 (as opposed to 7 for the standard 8051), allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip  $V_{DD}$  monitor (forces reset when power supply voltage drops below  $V_{RST}$  as given in Table 10.1 on page 104), a Watchdog Timer, a Missing Clock Detector, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an illegal Flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The internal oscillator factory calibrated to 24.5 MHz  $\pm 2\%$ . This internal oscillator period may be user programmed in  $\sim 0.5\%$  increments. An additional low-frequency oscillator is also available which facilitates low-power operation. An external oscillator drive circuit is included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. If desired, the system clock source may be switched on-the-fly between both internal and external oscillator circuits. An external oscillator can also be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) source, while periodically switching to the fast (up to 25 MHz) internal oscillator as needed.

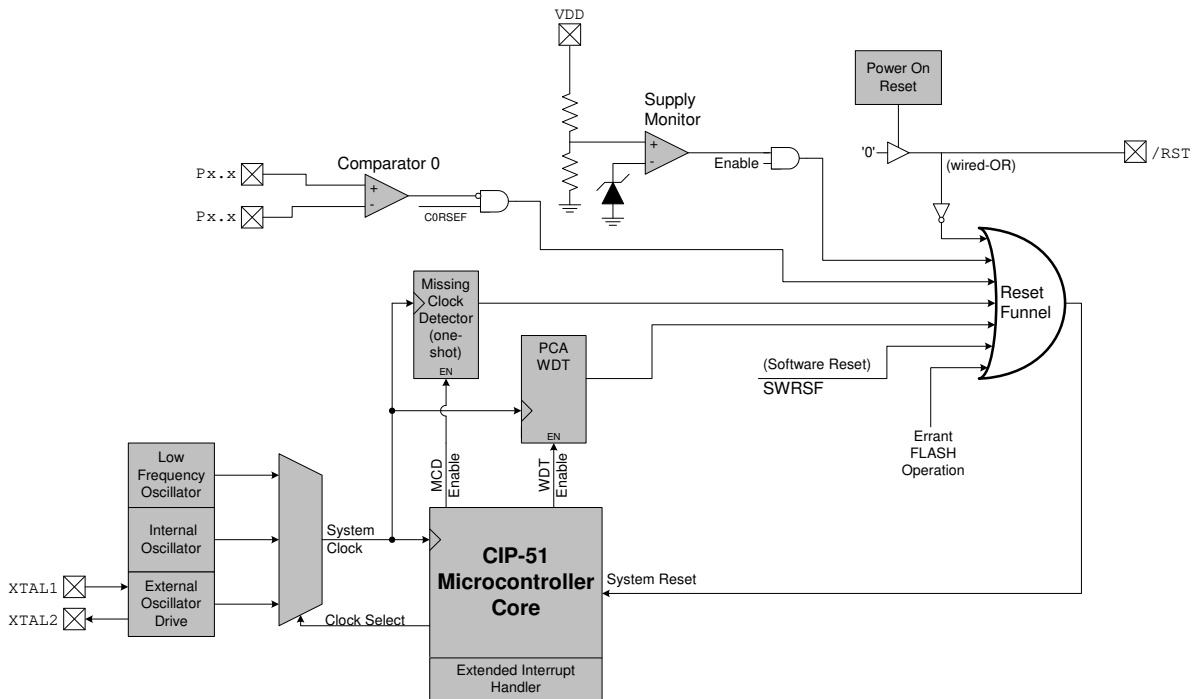


Figure 1.8. On-Chip Clock and Reset

# C8051F330/1/2/3/4/5

## 1.2. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

Program memory consists of 2/4/8 kB of Flash. This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. See Figure 1.9 for the MCU system memory map.

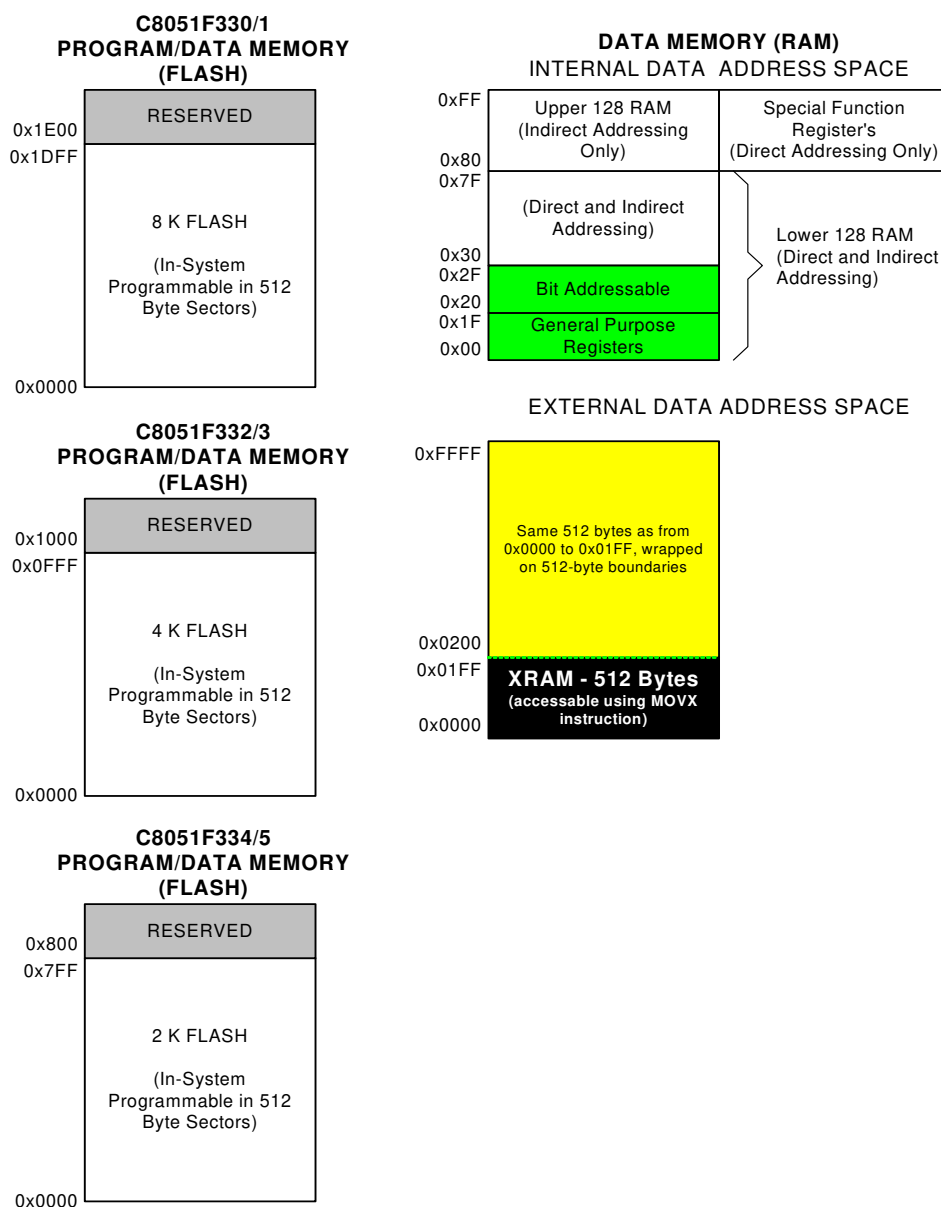


Figure 1.9. On-Board Memory Map

## 1.3. On-Chip Debug Circuitry

The C8051F330/1/2/3/4/5 devices include on-chip Silicon Labs 2-Wire (C2) debug circuitry that provides non-intrusive, full speed, in-circuit debugging of the production part *installed in the end application*.

Silicon Labs' debugging system supports inspection and modification of memory and registers, breakpoints, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the ADC and SMBus) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F330DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F330/1/2/3/4/5 MCUs. The kit includes software with a developer's studio and debugger, an integrated 8051 assembler, and a debug adapter. It also has a target application board with the associated MCU installed and prototyping area, plus the required cables, and wall-mount power supply. The Development Kit requires a PC running Windows98SE or later.

The Silicon Labs IDE interface is a vastly superior developing and debugging configuration, compared to standard MCU emulators that use on-board "ICE Chips" and require the MCU in the application board to be socketed. Silicon Labs' debug paradigm increases ease of use and preserves the performance of the precision analog peripherals.

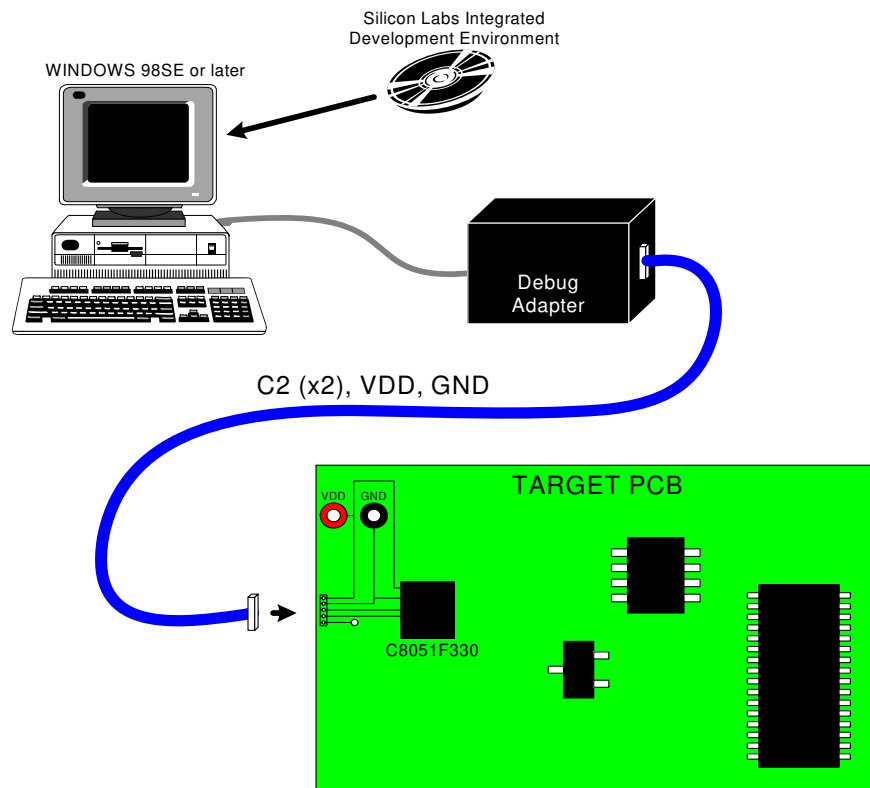


Figure 1.10. Development/In-System Debug Diagram