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Analog Peripherals

- **10-Bit ADC ('F330 and 'F330D only)**
 - Up to 200 ksp/s
 - Up to 16 external single-ended or differential inputs
 - VREF from internal VREF, external pin or V_{DD}
 - Internal or external start of conversion source
 - Built-in temperature sensor
- **10-Bit Current Output DAC ('F330 and 'F330D only)**
- **Comparator**
 - Programmable hysteresis and response time
 - Configurable as interrupt or reset source
 - Low current (0.4 μ A)

On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Low cost, **complete** development kit

Supply Voltage 2.7 to 3.6 V

- Typical operating current: 6.4 mA at 25 MHz;
9 μ A at 32 kHz
- Typical stop mode current: 0.1 μ A

Temperature Range: -40 to +85 °C

High Speed 8051 μ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

Memory

- 768 bytes internal data RAM (256 + 512)
- 8 kB Flash; In-system programmable in 512-byte Sectors—512 bytes are reserved

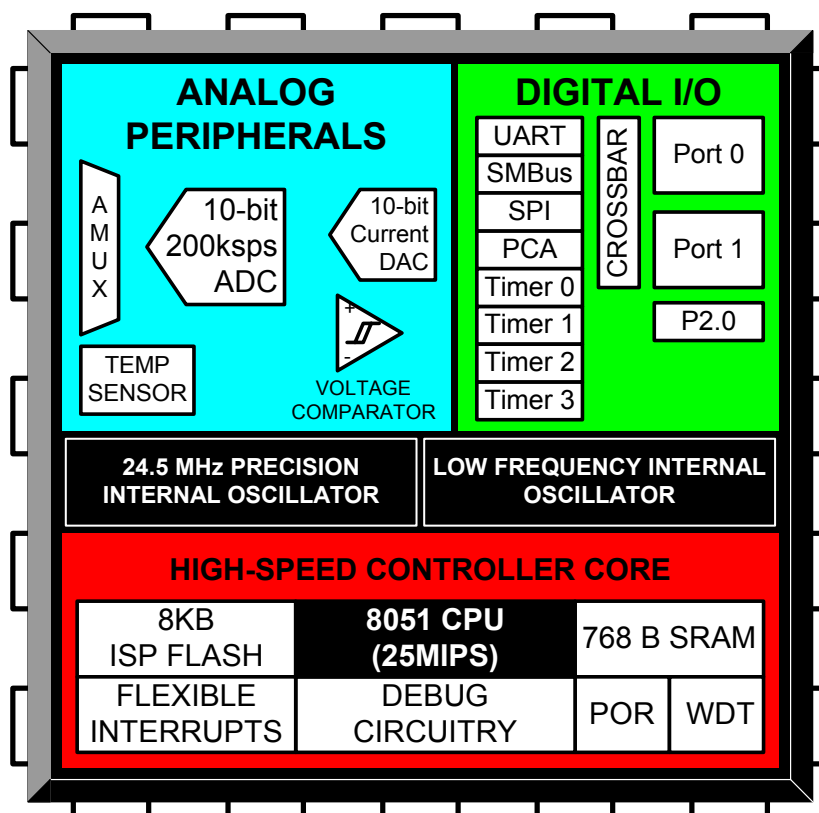
Digital Peripherals

- 17 Port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART, SMBus™, and enhanced SPI™ serial ports
- Four general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with three capture/compare modules
- Real time clock mode using PCA or timer and external clock source

Clock Sources

- Two internal oscillators:
 - 24.5 MHz with $\pm 2\%$ accuracy supports crystal-less UART operation
 - 80/40/20/10 kHz low frequency, low power
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly; useful in power saving modes

20-Pin MLP or 20-pin DIP



C8051F330/1, C8051F330D

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1. System Overview

C8051F330/1, C8051F330D devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 10-bit 200 kbps 16-channel single-ended/differential ADC with analog multiplexer
- 10-bit Current Output DAC
- Precision programmable 25 MHz internal oscillator
- 8k bytes of on-chip Flash memory—512 bytes are reserved
- 768 bytes of on-chip RAM
- SMBus/I2C, Enhanced UART, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with three capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, V_{DD} Monitor, and Temperature Sensor
- On-chip Voltage Comparator
- 17 Port I/O (5 V tolerant)

With on-chip Power-On Reset, V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051F330/1, C8051F330D devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 2.7 V-to-3.6 V operation over the industrial temperature range (–40 to +85 °C). The Port I/O and /RST pins are tolerant of input signals up to 5 V. The C8051F330/1 are available in a 20-pin MLP package and the C8051F330D is available in a 20-pin DIP package. Block diagrams are included in Figure 1.1 and Figure 1.2.

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Table 1.1. Product Selection Guide

	MIPS (Peak)	Flash Memory	RAM	Calibrated Internal 24.5 MHz Oscillator	Internal 80 kHz Oscillator	SMBus/I ² C	Enhanced SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 200ksps ADC	10-bit Current Output DAC	Internal Voltage Reference	Temperature Sensor	Analog Comparator	Package
C8051F330	25	8k	768	✓	✓	✓	✓	✓	4	✓	17	✓	✓	✓	✓	✓	MLP-20
C8051F330D	25	8k	768	✓	✓	✓	✓	✓	4	✓	17	✓	✓	✓	✓	✓	DIP-20
C8051F331	25	8k	768	✓	✓	✓	✓	✓	4	✓	17	-	-	-	-	✓	MLP-20

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1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F330/1, C8051F330D family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052, including four 16-bit counter/timers, a full-duplex UART with extended baud rate configuration, an enhanced SPI port, 768 bytes of internal RAM, 128 byte Special Function Register (SFR) address space, and 17 I/O pins.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. Figure 1.3 shows a comparison of peak throughputs for various 8-bit microcontroller cores with their maximum system clocks.

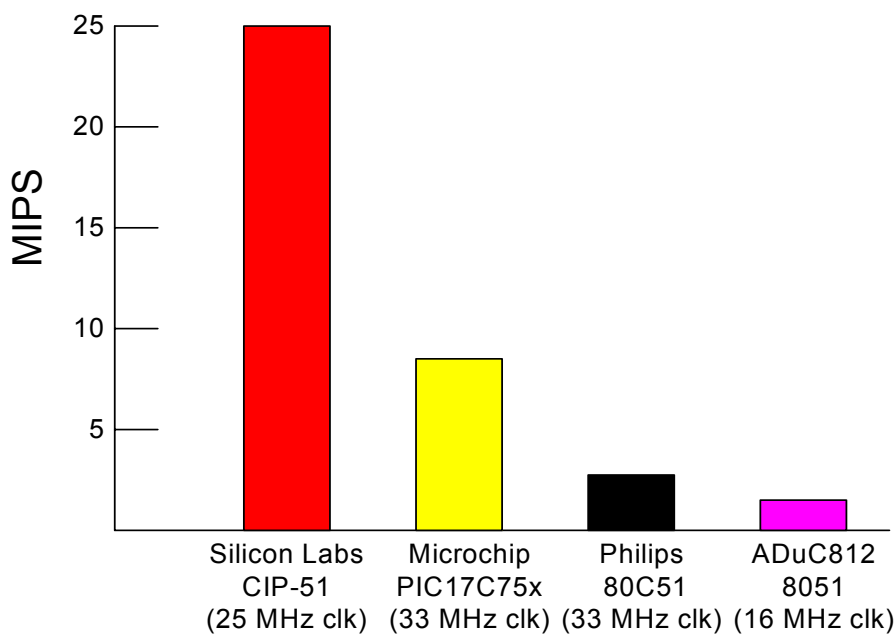


Figure 1.3. Comparison of Peak MCU Execution Speeds

1.1.3. Additional Features

The C8051F330/1, C8051F330D SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides 14 interrupt sources into the CIP-51 (as opposed to 7 for the standard 8051), allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} monitor (forces reset when power supply voltage drops below V_{RST} as given in Table 10.1 on page 94), a Watchdog Timer, a Missing Clock Detector, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an illegal Flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The internal oscillator factory calibrated to 24.5 MHz $\pm 2\%$. This internal oscillator period may be user programmed in $\sim 0.5\%$ increments. An additional low-frequency oscillator is also available which facilitates low-power operation. An external oscillator drive circuit is included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. If desired, the system clock source may be switched on-the-fly between both internal and external oscillator circuits. An external oscillator can also be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) source, while periodically switching to the fast (up to 25 MHz) internal oscillator as needed.

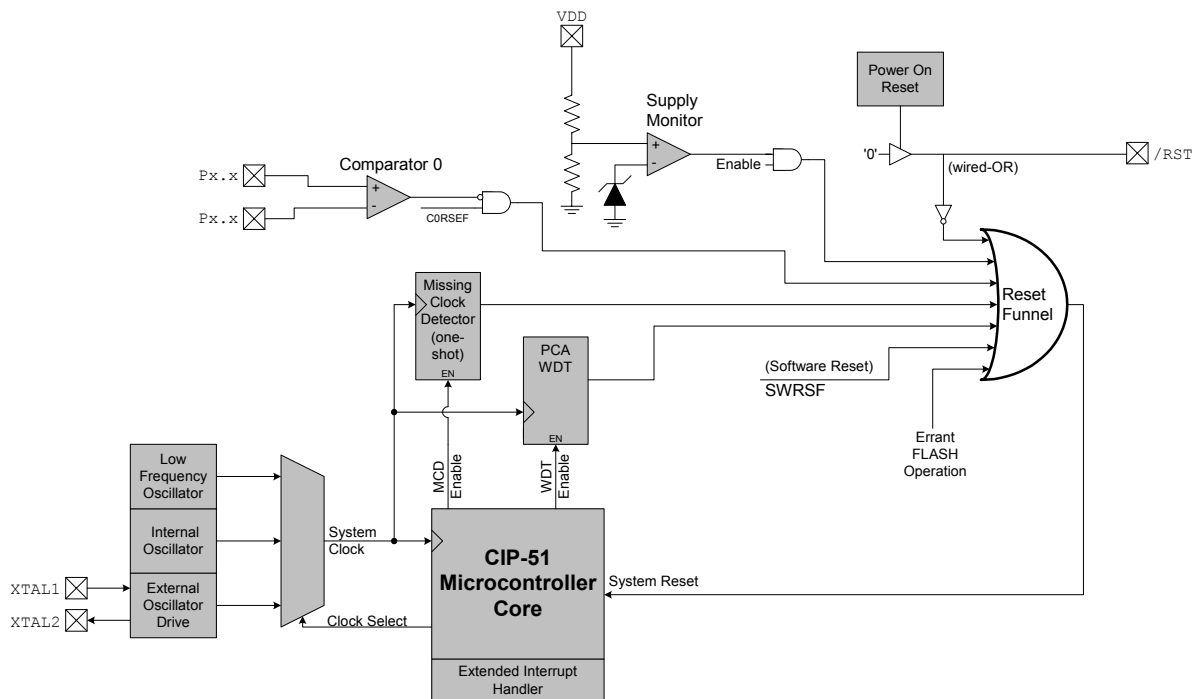


Figure 1.4. On-Chip Clock and Reset

C8051F330/1, C8051F330D

1.2. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

Program memory consists of 8k bytes of Flash. This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. See Figure 1.5 for the MCU system memory map.

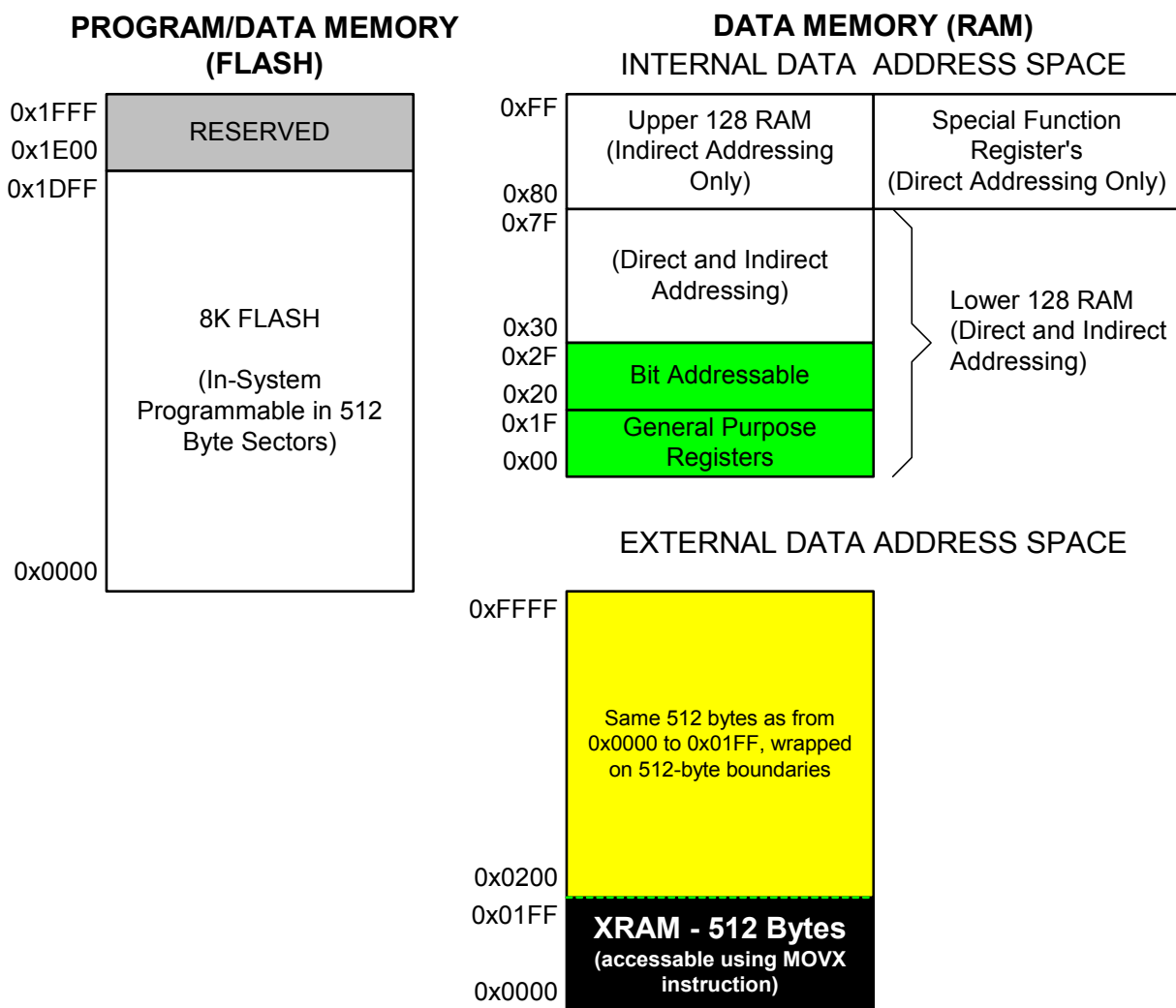


Figure 1.5. On-Board Memory Map

C8051F330/1, C8051F330D

1.3. On-Chip Debug Circuitry

The C8051F330/1, C8051F330D devices include on-chip Silicon Labs 2-Wire (C2) debug circuitry that provides non-intrusive, full speed, in-circuit debugging of the production part *installed in the end application*.

Silicon Labs' debugging system supports inspection and modification of memory and registers, breakpoints, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the ADC and SMBus) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F330DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F330/1, C8051F330D MCUs. The kit includes software with a developer's studio and debugger, an integrated 8051 assembler, and an RS-232 to C2 serial adapter. It also has a target application board with the associated MCU installed and prototyping area, plus the RS-232 and C2 cables, and wall-mount power supply. The Development Kit requires a Windows 95/98/NT/ME/2000 computer with one available RS-232 serial port. As shown in Figure 1.6, the PC is connected via RS-232 to the Serial Adapter. A six-inch ribbon cable connects the Serial Adapter to the user's application board, picking up the two C2 pins and V_{DD} and GND. The Serial Adapter takes its power from the application board. For applications where there is not sufficient power available from the target board, the provided power supply can be connected directly to the Serial Adapter.

The Silicon Labs IDE interface is a vastly superior developing and debugging configuration, compared to standard MCU emulators that use on-board "ICE Chips" and require the MCU in the application board to be socketed. Silicon Labs' debug paradigm increases ease of use and preserves the performance of the precision analog peripherals.

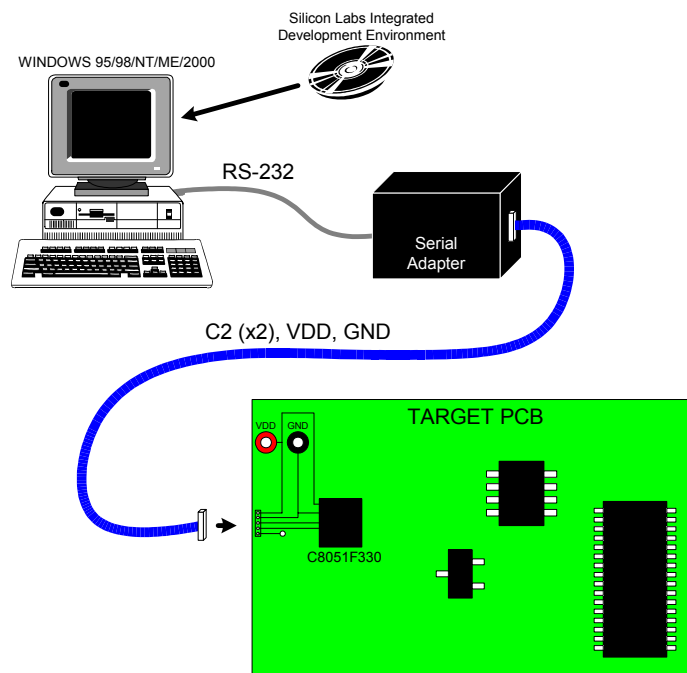


Figure 1.6. Development/In-System Debug Diagram

C8051F330/1, C8051F330D

1.4. Programmable Digital I/O and Crossbar

C8051F330/1, C8051F330D devices include 17 I/O pins (two byte-wide Ports and one 1-bit-wide Port). The C8051F330/1, C8051F330D Ports behave like typical 8051 Ports with a few enhancements. Each Port pin may be configured as an analog input or a digital I/O pin. Pins selected as digital I/Os may additionally be configured for push-pull or open-drain output. The “weak pull-ups” that are fixed on typical 8051 devices may be globally disabled, providing power savings capabilities.

The Digital Crossbar allows mapping of internal digital system resources to Port I/O pins (See Figure 1.7). On-chip counter/timers, serial buses, HW interrupts, comparator output, and other digital signals in the controller can be configured to appear on the Port I/O pins specified in the Crossbar Control registers. This allows the user to select the exact mix of general purpose Port I/O and digital resources needed for the particular application.

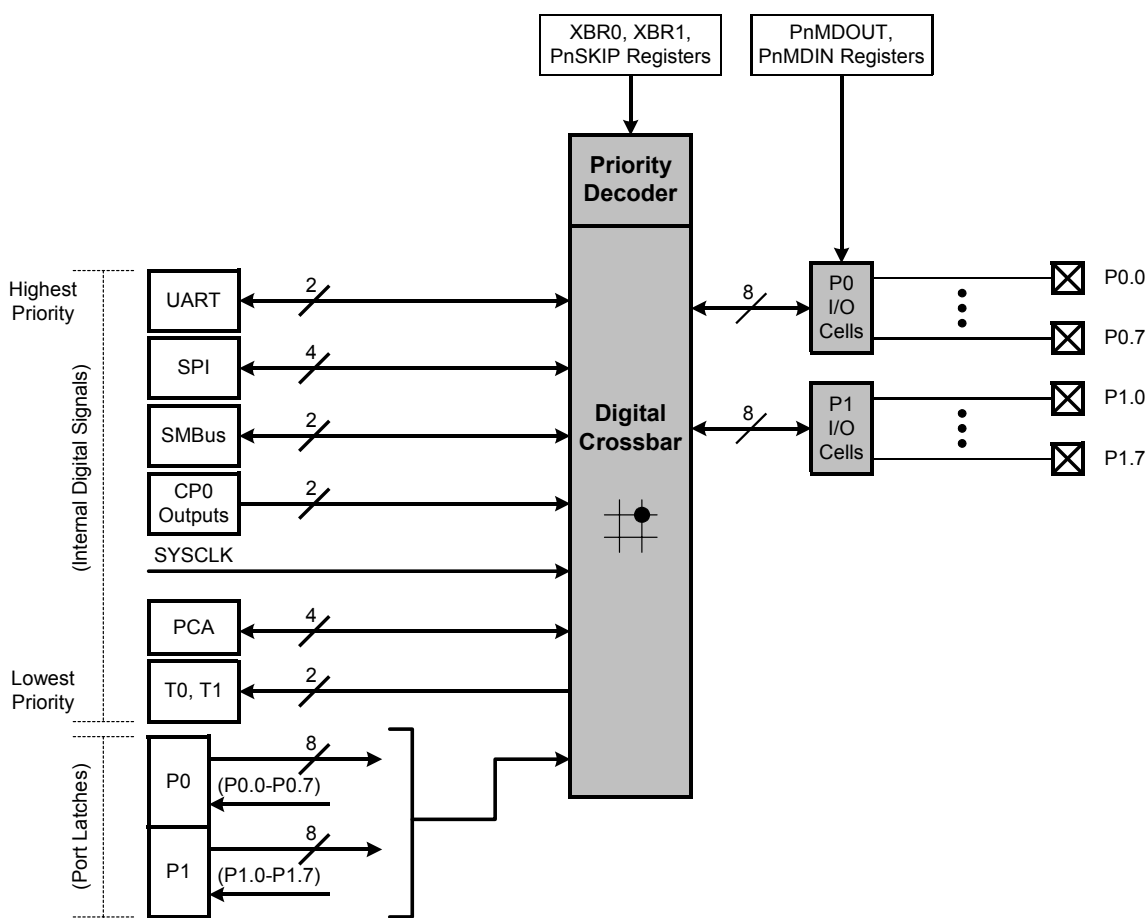


Figure 1.7. Digital Crossbar Diagram

1.5. Serial Ports

The C8051F330/1, C8051F330D Family includes an SMBus/I²C interface, a full-duplex UART with enhanced baud rate configuration, and an Enhanced SPI interface. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.

1.6. Programmable Counter Array

An on-chip Programmable Counter/Timer Array (PCA) is included in addition to the four 16-bit general purpose counter/timers. The PCA consists of a dedicated 16-bit counter/timer time base with three programmable capture/compare modules. The PCA clock is derived from one of six sources: the system clock divided by 12, the system clock divided by 4, Timer 0 overflows, an External Clock Input (ECI), the system clock, or the external oscillator clock source divided by 8. The external clock source selection is useful for real-time clock functionality, where the PCA is clocked by an external source while the internal oscillator drives the system clock.

Each capture/compare module can be configured to operate in one of six modes: Edge-Triggered Capture, Software Timer, High Speed Output, 8- or 16-bit Pulse Width Modulator, or Frequency Output. Additionally, Capture/Compare Module 2 offers watchdog timer (WDT) capabilities. Following a system reset, Module 2 is configured and enabled in WDT mode. The PCA Capture/Compare Module I/O and External Clock Input may be routed to Port I/O via the Digital Crossbar.

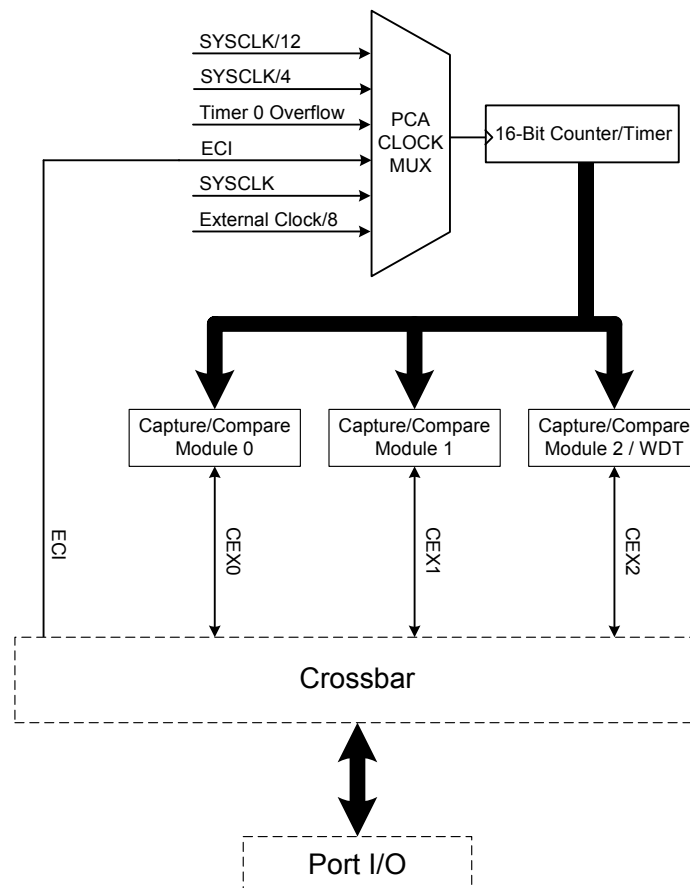


Figure 1.9. PCA Block Diagram

C8051F330/1, C8051F330D

1.7. 10-Bit Analog to Digital Converter

The C8051F330 and C8051F330D devices include an on-chip 10-bit SAR ADC with a 16-channel differential input multiplexer. With a maximum throughput of 200 ksps, the ADC offers true 10-bit linearity with an INL and DNL of ± 1 LSB. The ADC system includes a configurable analog multiplexer that selects both positive and negative ADC inputs. Ports0-1 are available as an ADC inputs; additionally, the on-chip Temperature Sensor output and the power supply voltage (V_{DD}) are available as ADC inputs. User firmware may shut down the ADC to save power.

Conversions can be started in six ways: a software command, an overflow of Timer 0, 1, 2, or 3, or an external convert start signal. This flexibility allows the start of conversion to be triggered by software events, a periodic signal (timer overflows), or external HW signals. Conversion completions are indicated by a status bit and an interrupt (if enabled). The resulting 10-bit data word is latched into the ADC data SFRs upon completion of a conversion.

Window compare registers for the ADC data can be configured to interrupt the controller when ADC data is either within or outside of a specified range. The ADC can monitor a key voltage continuously in background mode, but not interrupt the controller unless the converted data is within/outside the specified range.

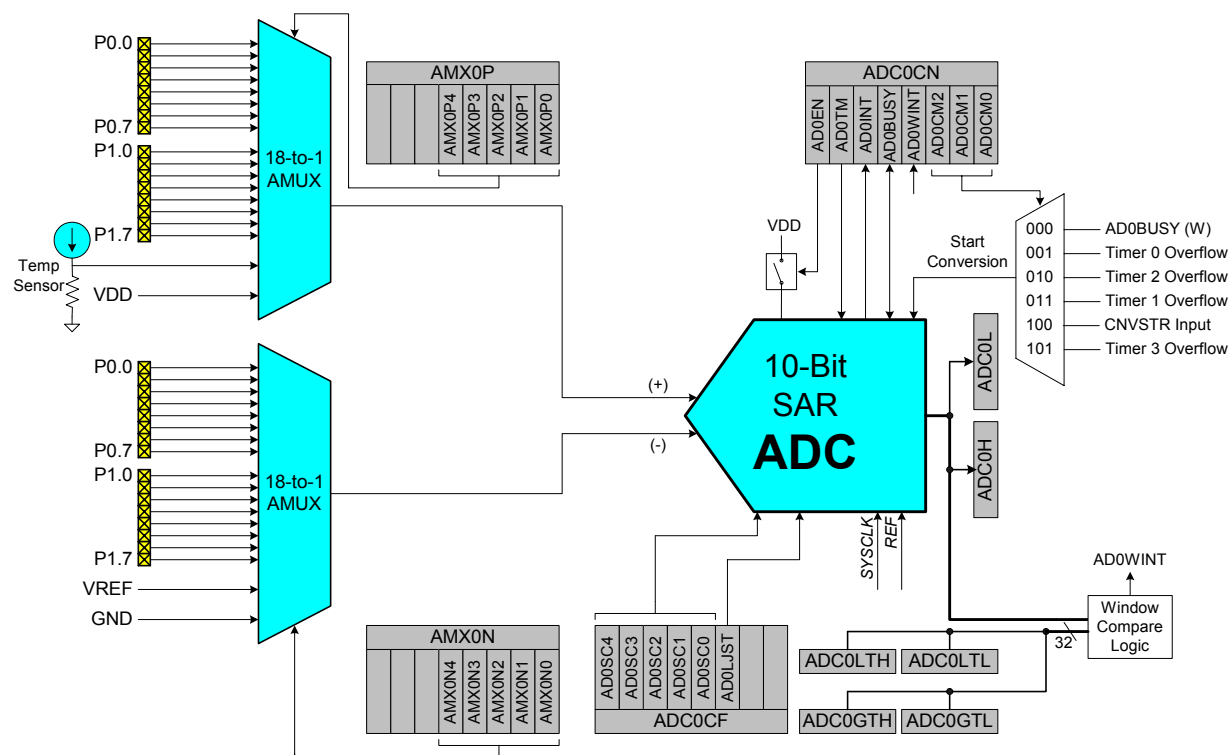


Figure 1.10. 10-Bit ADC Block Diagram

1.8. Comparators

C8051F330/1, C8051F330D devices include an on-chip voltage comparator that is enabled/disabled and configured via user software. Port I/O pins may be configured as comparator inputs via a selection mux. Two comparator outputs may be routed to a Port pin if desired: a latched output and/or an unlatched (asynchronous) output. Comparator response time is programmable, allowing the user to select between high-speed and low-power modes. Positive and negative hysteresis are also configurable.

Comparator interrupts may be generated on rising, falling, or both edges. When in IDLE mode, these interrupts may be used as a “wake-up” source. Comparator0 may also be configured as a reset source. Figure 1.10 shows the Comparator0 block diagram.

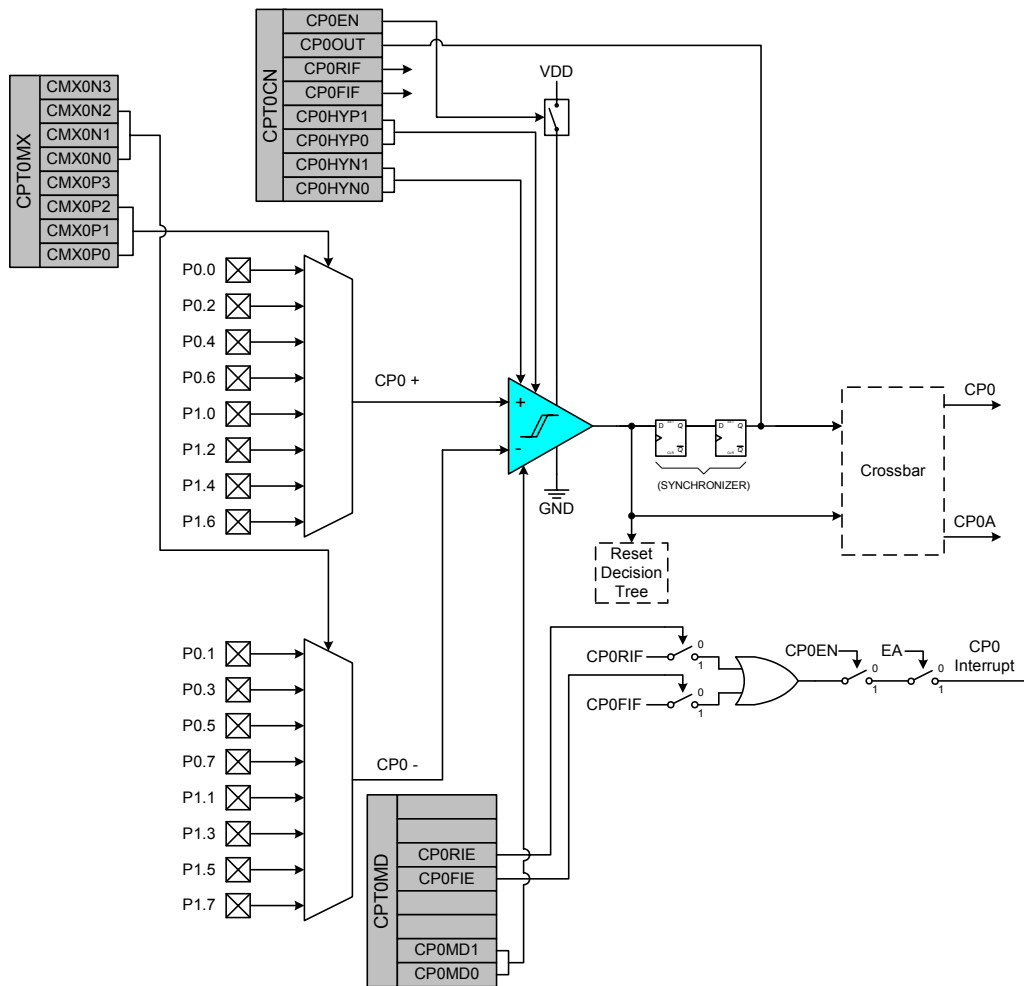


Figure 1.11. Comparator0 Block Diagram

C8051F330/1, C8051F330D

1.9. 10-bit Current Output DAC

The C8051F330 and C8051F330D device includes a 10-bit current-mode Digital-to-Analog Converter (IDA0). The maximum current output of the IDA0 can be adjusted for three different current settings; 0.5 mA, 1 mA, and 2 mA. IDA0 features a flexible output update mechanism which allows for seamless full-scale changes and supports jitter-free updates for waveform generation. Three update modes are provided, allowing IDA0 output updates on a write to IDA0H, on a Timer overflow, or on an external pin edge.

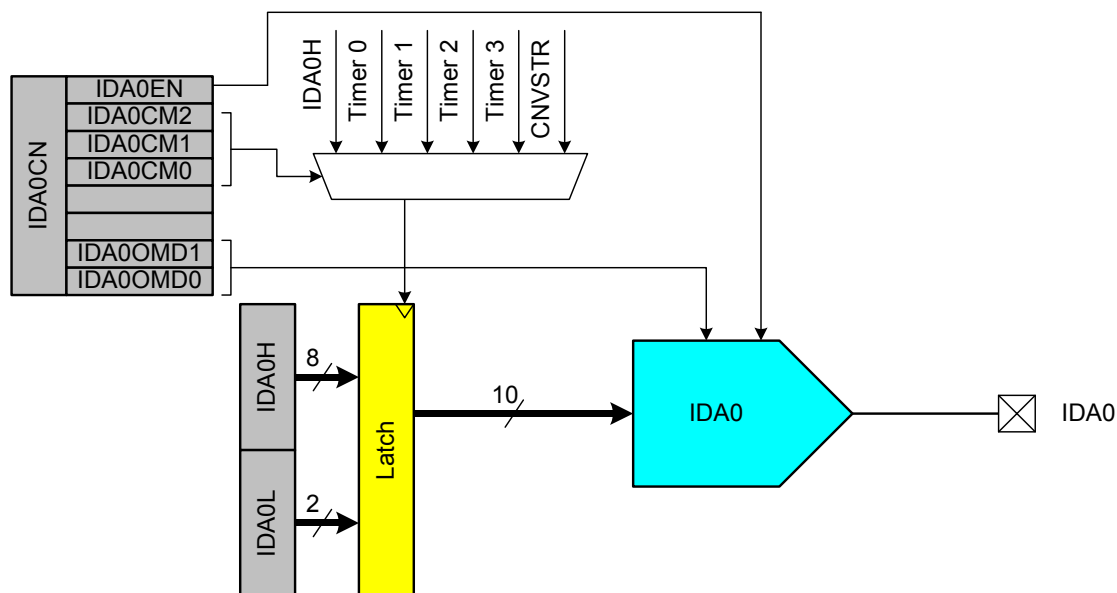


Figure 1.12. IDA0 Functional Block Diagram

2. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		-55	—	125	°C
Storage Temperature		-65	—	150	°C
Voltage on any Port I/O Pin or /RST with respect to GND		-0.3	—	5.8	V
Voltage on V_{DD} with respect to GND		-0.3	—	4.2	V
Maximum Total current through V_{DD} or GND		—	—	500	mA
Maximum output current sunk by /RST or any Port pin		—	—	100	mA
Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.					