Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

C8051F350/1/2/3

8 k ISP Flash MCU Family

Analog Peripherals
- **24 or 16-Bit ADC**
  - No missing codes
  - 0.0015% nonlinearity
  - Programmable conversion rates up to 1 ksps
  - 8-Input multiplexer
  - 1x to 128x PGA
  - Built-in temperature sensor
- **Two 8-Bit Current Output DACs**
- **Comparator**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source
  - Low current (0.4 µA)

On-chip Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (No emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-Chips, target pods, and sockets
- Low Cost, **Complete** Development Kit

Supply Voltage 2.7 to 3.6 V
- Typical operating current: 5.8 mA @ 25 MHz; 11 µA @ 32 kHz
- Typical stop mode current: 0.1 µA

Temperature Range: –40 to +85 °C

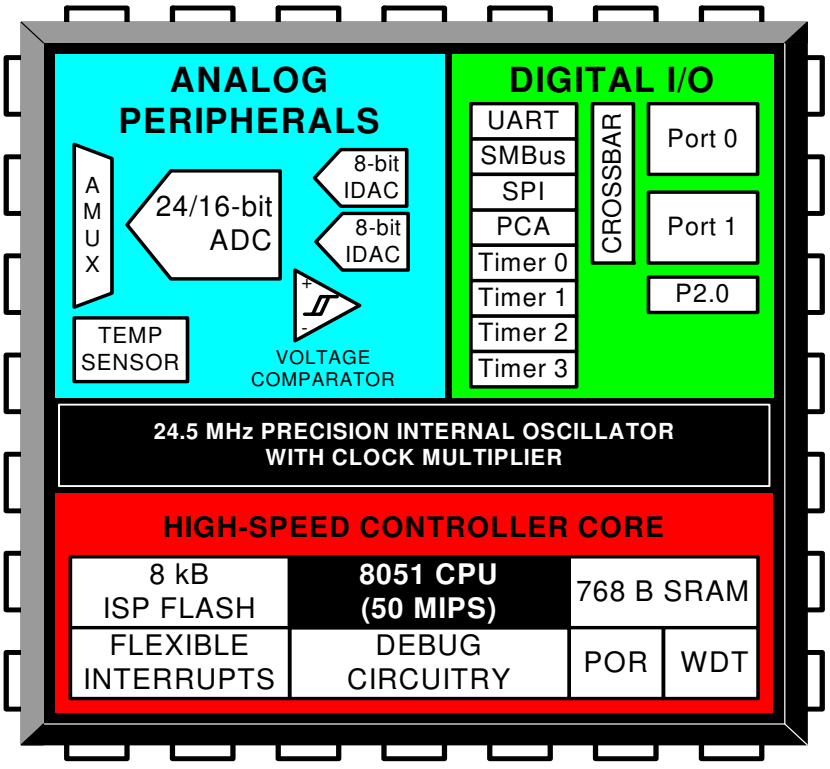
High Speed 8051 µC Core
- Pipelined Instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput
- Expanded interrupt handler

Memory
- 768 Bytes (256 + 512) On-Chip RAM
- 8 kB Flash; In-system programmable in 512-byte Sectors

Digital Peripherals
- 17 Port I/O; All 5 V tolerant with high sink current
- Enhanced UART, SMBus™, and SPI™ Serial Ports
- Four general purpose 16-bit counter/timers
- 16-bit programmable counter array (PCA) with three capture/compare modules
- Real time clock mode using PCA or timer and external clock source

Clock Sources
- Internal Oscillator: 24.5 MHz with ± 2% accuracy supports UART operation
- External Oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- Clock multiplier to achieve 50 MHz internal clock
- Can switch between clock sources on-the-fly

28-Pin QFN or 32-Pin LQFP Package
- 5 x 5 mm PCB footprint with 28-QFN



Copyright © 2007 by Silicon Laboratories

NOTES:

Table of Contents

1. System Overview 17
1.1. CIP-51™ Microcontroller 21
1.1.1. Fully 8051 Compatible Instruction Set 21
1.1.2. Improved Throughput 21
1.1.3. Additional Features 21
1.2. On-Chip Debug Circuitry 22
1.3. On-Chip Memory 23
1.4. 24 or 16-Bit Analog to Digital Converter (ADC0) 24
1.5. Two 8-bit Current-Mode DACs 25
1.6. Programmable Comparator 26
1.7. Serial Ports 26
1.8. Port Input/Output 27
1.9. Programmable Counter Array 28
2. Absolute Maximum Ratings 29
3. Global DC Electrical Characteristics 30
4. Pinout and Package Definitions 31
5. 24 or 16-Bit Analog to Digital Converter (ADC0) 41
5.1. Configuration 42
5.1.1. Voltage Reference Selection 42
5.1.2. Analog Inputs 42
5.1.3. Modulator Clock 43
5.1.4. Decimation Ratio 43
5.2. Calibrating the ADC 44
5.2.1. Internal Calibration 44
5.2.2. System Calibration 44
5.2.3. Calibration Coefficient Storage 44
5.3. Performing Conversions 46
5.3.1. Single Conversions 46
5.3.2. Continuous Conversions 46
5.3.3. ADC Output 46
5.3.4. Error Conditions 47
5.4. Offset DAC 47
5.5. Burnout Current Sources 47
5.6. Analog Multiplexer 59
6. 8-Bit Current Mode DACS (IDA0 and IDA1) 67
6.1. IDAC Output Scheduling 68
6.1.1. Update Output On-Demand 68
6.1.2. Update Output Based on Timer Overflow 68
6.1.3. Update Output Based on CNVSTR Edge 68
6.2. IDAC Output Mapping 68
6.3. IDAC External Pin Connections 71
7. Voltage Reference 73
8. Temperature Sensor 77

9. Comparator0 79
9.1. Comparator0 Inputs and Outputs 83
10. CIP-51 Microcontroller 87
10.1. Instruction Set 89
10.1.1. Instruction and CPU Timing 89
10.1.2. MOVX Instruction and Program Memory 89
10.2. Register Descriptions 93
10.3. Power Management Modes 96
10.3.1. Idle Mode 96
10.3.2. Stop Mode 96
11. Memory Organization and SFRs 99
11.1. Program Memory 99
11.2. Data Memory 100
11.3. General Purpose Registers 100
11.4. Bit Addressable Locations 100
11.5. Stack 100
11.6. Special Function Registers 101
12. Interrupt Handler 105
12.1. MCU Interrupt Sources and Vectors 105
12.2. Interrupt Priorities 105
12.3. Interrupt Latency 105
12.4. Interrupt Register Descriptions 107
12.5. External Interrupts 111
13. Prefetch Engine 113
14. Reset Sources 115
14.1. Power-On Reset 116
14.2. Power-Fail Reset / VDD Monitor 117
14.3. External Reset 118
14.4. Missing Clock Detector Reset 118
14.5. Comparator0 Reset 118
14.6. PCA Watchdog Timer Reset 118
14.7. Flash Error Reset 118
14.8. Software Reset 118
15. Flash Memory 121
15.1. Programming The Flash Memory 121
15.1.1. Flash Lock and Key Functions 121
15.1.2. Flash Erase Procedure 121
15.1.3. Flash Write Procedure 122
15.2. Non-volatile Data Storage 123
15.3. Security Options 123
16. External RAM 127
17. Oscillators 129
17.1. Programmable Internal Oscillator 129
17.2. External Oscillator Drive Circuit 131
17.2.1. Clocking Timers Directly Through the External Oscillator 131

17.2.2.External Crystal Example 131
17.2.3.External RC Example 133
17.2.4.External Capacitor Example 133
17.3.Clock Multiplier 135
17.4.System Clock Selection 136
18. Port Input/Output 137
18.1.Priority Crossbar Decoder 139
18.2.Port I/O Initialization 141
18.3.General Purpose Port I/O 144
19. SMBus 151
19.1.Supporting Documents 152
19.2.SMBus Configuration 152
19.3.SMBus Operation 152
19.3.1.Arbitration 153
19.3.2.Clock Low Extension 154
19.3.3.SCL Low Timeout 154
19.3.4.SCL High (SMBus Free) Timeout 154
19.4.Using the SMBus 155
19.4.1.SMBus Configuration Register 156
19.4.2.SMB0CN Control Register 159
19.4.3.Data Register 162
19.5.SMBus Transfer Modes 163
19.5.1.Master Transmitter Mode 163
19.5.2.Master Receiver Mode 164
19.5.3.Slave Receiver Mode 165
19.5.4.Slave Transmitter Mode 166
19.6.SMBus Status Decoding 167
20. UART0 171
20.1.Enhanced Baud Rate Generation 172
20.2.Operational Modes 173
20.2.1.8-Bit UART 173
20.2.2.9-Bit UART 174
20.3.Multiprocessor Communications 174
21. Serial Peripheral Interface (SPI0) 181
21.1.Signal Descriptions 182
21.1.1.Master Out, Slave In (MOSI) 182
21.1.2.Master In, Slave Out (MISO) 182
21.1.3.Serial Clock (SCK) 182
21.1.4.Slave Select (NSS) 182
21.2.SPI0 Master Mode Operation 183
21.3.SPI0 Slave Mode Operation 185
21.4.SPI0 Interrupt Sources 185
21.5.Serial Clock Timing 186
21.6.SPI Special Function Registers 186

22. Timers 195
22.1.Timer 0 and Timer 1 195
22.1.1.Mode 0: 13-bit Counter/Timer 195
22.1.2.Mode 1: 16-bit Counter/Timer 196
22.1.3.Mode 2: 8-bit Counter/Timer with Auto-Reload 197
22.1.4.Mode 3: Two 8-bit Counter/Timers (Timer 0 Only) 198
22.2.Timer 2 203
22.2.1.16-bit Timer with Auto-Reload 203
22.2.2.8-bit Timers with Auto-Reload 204
22.3.Timer 3 207
22.3.1.16-bit Timer with Auto-Reload 207
22.3.2.8-bit Timers with Auto-Reload 208
23. Programmable Counter Array 211
23.1.PCA Counter/Timer 212
23.2.Capture/Compare Modules 213
23.2.1.Edge-triggered Capture Mode 214
23.2.2.Software Timer (Compare) Mode 215
23.2.3.High Speed Output Mode 216
23.2.4.Frequency Output Mode 217
23.2.5.8-Bit Pulse Width Modulator Mode 218
23.2.6.16-Bit Pulse Width Modulator Mode 219
23.3.Watchdog Timer Mode 220
23.3.1.Watchdog Timer Operation 220
23.3.2.Watchdog Timer Usage 221
23.4.Register Descriptions for PCA 222
24. Revision Specific Behavior 227
24.1.Revision Identification 227
25. C2 Interface 229
25.1.C2 Interface Registers 229
25.2.C2 Pin Sharing 231
Document Change List 232
Contact Information 234

List of Figures

1. System Overview
Figure 1.1. C8051F350 Block Diagram 19
Figure 1.2. C8051F351 Block Diagram 19
Figure 1.3. C8051F352 Block Diagram 20
Figure 1.4. C8051F353 Block Diagram 20
Figure 1.5. Development/In-System Debug Diagram 22
Figure 1.6. Memory Map 23
Figure 1.7. ADC0 Block Diagram 24
Figure 1.8. IDAC Block Diagram 25
Figure 1.9. Comparator0 Block Diagram 26
Figure 1.10. Port I/O Functional Block Diagram 27
Figure 1.11. PCA Block Diagram 28
2. Absolute Maximum Ratings
3. Global DC Electrical Characteristics
4. Pinout and Package Definitions
Figure 4.1. LQFP-32 Pinout Diagram (Top View) 34
Figure 4.2. QFN-28 Pinout Diagram (Top View) 35
Figure 4.3. LQFP-32 Package Diagram 36
Figure 4.4. QFN-28 Package Drawing 37
Figure 4.5. Typical QFN-28 Landing Diagram 38
Figure 4.6. Typical QFN-28 Solder Paste Diagram 39
5. 24 or 16-Bit Analog to Digital Converter (ADC0)
Figure 5.1. ADC0 Block Diagram 41
Figure 5.2. ADC0 Buffer Control 43
Figure 5.3. ADC0 Offset Calibration Register Coding 45
Figure 5.4. ADC0 Gain Calibration Register Coding 45
Figure 5.5. ADC0 Multiplexer Connections 59
6. 8-Bit Current Mode DACS (IDA0 and IDA1)
Figure 6.1. IDAC Functional Block Diagram 67
Figure 6.2. IDAC Data Word Mapping 68
Figure 6.3. IDAC Pin Connections 71
7. Voltage Reference
Figure 7.1. Reference Circuitry Block Diagram 73
8. Temperature Sensor
Figure 8.1. Temperature Sensor Block Diagram 77
Figure 8.2. Single Channel Transfer Function 78
Figure 8.3. Differential Transfer Function 78
9. Comparator0
Figure 9.1. Comparator0 Functional Block Diagram 79
Figure 9.2. Comparator Hysteresis Plot 80
Figure 9.3. Comparator Pin Connections 83
10. CIP-51 Microcontroller
Figure 10.1. CIP-51 Block Diagram 87

11. Memory Organization and SFRs
Figure 11.1. Memory Map 99
12. Interrupt Handler
13. Prefetch Engine
14. Reset Sources
Figure 14.1. Reset Sources 115
Figure 14.2. Power-On and VDD Monitor Reset Timing 116
15. Flash Memory
Figure 15.1. Flash Memory Map 123
16. External RAM
17. Oscillators
Figure 17.1. Oscillator Diagram 129
Figure 17.2. 32.768 kHz External Crystal Example 132
18. Port Input/Output
Figure 18.1. Port I/O Functional Block Diagram 137
Figure 18.2. Port I/O Cell Block Diagram 138
Figure 18.3. Crossbar Priority Decoder with No Pins Skipped 139
Figure 18.4. Crossbar Priority Decoder with Crystal Pins Skipped 140
19. SMBus
Figure 19.1. SMBus Block Diagram 151
Figure 19.2. Typical SMBus Configuration 152
Figure 19.3. SMBus Transaction 153
Figure 19.4. Typical SMBus SCL Generation 157
Figure 19.5. Typical Master Transmitter Sequence 163
Figure 19.6. Typical Master Receiver Sequence 164
Figure 19.7. Typical Slave Receiver Sequence 165
Figure 19.8. Typical Slave Transmitter Sequence 166
20. UART0
Figure 20.1. UART0 Block Diagram 171
Figure 20.2. UART0 Baud Rate Logic 172
Figure 20.3. UART Interconnect Diagram 173
Figure 20.4. 8-Bit UART Timing Diagram 173
Figure 20.5. 9-Bit UART Timing Diagram 174
Figure 20.6. UART Multi-Processor Mode Interconnect Diagram 175
21. Serial Peripheral Interface (SPI0)
Figure 21.1. SPI Block Diagram 181
Figure 21.2. Multiple-Master Mode Connection Diagram 184
Figure 21.3. 3-Wire Single Master and Slave Mode Connection Diagram 184
Figure 21.4. 4-Wire Single Master and Slave Mode Connection Diagram 184
Figure 21.5. Data/Clock Timing Relationship 186
Figure 21.6. SPI Master Timing (CKPHA = 0) 191
Figure 21.7. SPI Master Timing (CKPHA = 1) 191
Figure 21.8. SPI Slave Timing (CKPHA = 0) 192
Figure 21.9. SPI Slave Timing (CKPHA = 1) 192

22. Timers
Figure 22.1. T0 Mode 0 Block Diagram 196
Figure 22.2. T0 Mode 2 Block Diagram 197
Figure 22.3. T0 Mode 3 Block Diagram 198
Figure 22.4. Timer 2 16-Bit Mode Block Diagram 203
Figure 22.5. Timer 2 8-Bit Mode Block Diagram 204
Figure 22.6. Timer 3 16-Bit Mode Block Diagram 207
Figure 22.7. Timer 3 8-Bit Mode Block Diagram 208
23. Programmable Counter Array
Figure 23.1. PCA Block Diagram 211
Figure 23.2. PCA Counter/Timer Block Diagram 212
Figure 23.3. PCA Interrupt Block Diagram 213
Figure 23.4. PCA Capture Mode Diagram 214
Figure 23.5. PCA Software Timer Mode Diagram 215
Figure 23.6. PCA High Speed Output Mode Diagram 216
Figure 23.7. PCA Frequency Output Mode 217
Figure 23.8. PCA 8-Bit PWM Mode Diagram 218
Figure 23.9. PCA 16-Bit PWM Mode 219
Figure 23.10. PCA Module 2 with Watchdog Timer Enabled 220
24. Revision Specific Behavior
Figure 24.1. Reading Package Marking 227
25. C2 Interface
Figure 25.1. Typical C2 Pin Sharing 231

NOTES:

List of Tables

1. System Overview
Table 1.1. Product Selection Guide 18
2. Absolute Maximum Ratings
3. Global DC Electrical Characteristics
4. Pinout and Package Definitions
Table 4.1. Pin Definitions for the C8051F350/1/2/3 31
Table 4.2. LQFP-32 Package Dimensions 36
Table 4.3. QFN-28 Package Dimensions 37
5. 24 or 16-Bit Analog to Digital Converter (ADC0)
Table 5.1. ADC0 Unipolar Output Word Coding (AD0POL = 0) 47
Table 5.2. ADC0 Bipolar Output Word Coding (AD0POL = 1) 47
Table 5.3. ADC0 SINC3 Filter Typical RMS Noise (µV) 62
Table 5.4. ADC0 SINC3 Filter Effective Resolution in Unipolar Mode (bits) 63
Table 5.5. ADC0 SINC3 Filter Flicker-Free (Noise-Free) Resolution in Unipolar Mode (bits) 63
Table 5.6. ADC0 Fast Filter Typical RMS Noise (µV) 64
Table 5.7. ADC0 Fast Filter Effective Resolution[1] in Unipolar Mode (bits) 64
Table 5.8. ADC0 Fast Filter Flicker-Free (Noise-Free) Resolution in Unipolar Mode (bits) 65
6. 8-Bit Current Mode DACS (IDA0 and IDA1)
7. Voltage Reference
8. Temperature Sensor
9. Comparator0
10. CIP-51 Microcontroller
Table 10.1. CIP-51 Instruction Set Summary 89
11. Memory Organization and SFRs
Table 11.1. Special Function Register (SFR) Memory Map 101
Table 11.2. Special Function Registers 102
12. Interrupt Handler
Table 12.1. Interrupt Summary 106
13. Prefetch Engine
14. Reset Sources
15. Flash Memory
16. External RAM
17. Oscillators
18. Port Input/Output
19. SMBus
Table 19.1. SMBus Clock Source Selection 156
Table 19.2. Minimum SDA Setup and Hold Times 157
Table 19.3. Sources for Hardware Changes to SMB0CN 161
Table 19.4. SMBus Status Decoding 167
20. UART0

Table 20.1. Timer Settings for Standard Baud Rates Using the Internal Oscillator 178
Table 20.2. Timer Settings for Standard Baud Rates Using an External 25.0 MHz Oscillator 178
Table 20.3. Timer Settings for Standard Baud Rates Using an External 22.1184 MHz Oscillator 179
Table 20.4. Timer Settings for Standard Baud Rates Using an External 18.432 MHz Oscillator 179
Table 20.5. Timer Settings for Standard Baud Rates Using an External 11.0592 MHz Oscillator 180
Table 20.6. Timer Settings for Standard Baud Rates Using an External 3.6864 MHz Oscillator 180
21. Serial Peripheral Interface (SPI0)
Table 21.1. SPI Slave Timing Parameters 193
22. Timers
23. Programmable Counter Array
Table 23.1. PCA Timebase Input Options 212
Table 23.2. PCA0CPM Register Settings for PCA Capture/Compare Modules 213
Table 23.3. Watchdog Timer Timeout Intervals..... 221
24. Revision Specific Behavior
25. C2 Interface

List of Registers

SFR Definition 5.1. ADC0CN: ADC0 Control 48
SFR Definition 5.2. ADC0CF: ADC0 Configuration 49
SFR Definition 5.3. ADC0MD: ADC0 Mode 50
SFR Definition 5.4. ADC0CLK: ADC0 Modulator Clock Divisor 51
SFR Definition 5.5. ADC0DECH: ADC0 Decimation Ratio Register High Byte 51
SFR Definition 5.6. ADC0DECL: ADC0 Decimation Ratio Register Low Byte 52
SFR Definition 5.7. ADC0DAC: ADC0 Offset DAC 52
SFR Definition 5.8. ADC0BUF: ADC0 Input Buffer Control 53
SFR Definition 5.9. ADC0STA: ADC0 Status 54
SFR Definition 5.10. ADC0COH: ADC0 Offset Calibration Register High Byte 55
SFR Definition 5.11. ADC0COM: ADC0 Offset Calibration Register Middle Byte 55
SFR Definition 5.12. ADC0COL: ADC0 Offset Calibration Register Low Byte 55
SFR Definition 5.13. ADC0CGH: ADC0 Gain Calibration Register High Byte 56
SFR Definition 5.14. ADC0CGM: ADC0 Gain Calibration Register Middle Byte 56
SFR Definition 5.15. ADC0CGL: ADC0 Gain Calibration Register Low Byte 56
SFR Definition 5.16. ADC0H: ADC0 Conversion Register (SINC3 Filter) High Byte . . 57
SFR Definition 5.17. ADC0M: ADC0 Conversion Register (SINC3 Filter) Middle Byte 57
SFR Definition 5.18. ADC0L: ADC0 Conversion Register (SINC3 Filter) Low Byte . . . 57
SFR Definition 5.19. ADC0FH: ADC0 Conversion Register (Fast Filter) High Byte . . . 58
SFR Definition 5.20. ADC0FM: ADC0 Conversion Register (Fast Filter) Middle Byte . 58
SFR Definition 5.21. ADC0FL: ADC0 Conversion Register (Fast Filter) Low Byte 58
SFR Definition 5.22. ADC0MUX: ADC0 Analog Multiplexer Control 60
SFR Definition 6.1. IDA0CN: IDA0 Control 69
SFR Definition 6.2. IDA0: IDA0 Data Word 69
SFR Definition 6.3. IDA1CN: IDA1 Control 70
SFR Definition 6.4. IDA1: IDA1 Data Word 70
SFR Definition 7.1. REF0CN: Reference Control 74
SFR Definition 9.1. CPT0CN: Comparator0 Control 81
SFR Definition 9.2. CPT0MD: Comparator0 Mode Selection 82
SFR Definition 9.3. CPT0MX: Comparator0 MUX Selection 84
SFR Definition 10.1. SP: Stack Pointer 93
SFR Definition 10.2. DPL: Data Pointer Low Byte 93
SFR Definition 10.3. DPH: Data Pointer High Byte 93
SFR Definition 10.4. PSW: Program Status Word 94
SFR Definition 10.5. ACC: Accumulator 95
SFR Definition 10.6. B: B Register 95
SFR Definition 10.7. PCON: Power Control 97
SFR Definition 12.1. IE: Interrupt Enable 107
SFR Definition 12.2. IP: Interrupt Priority 108
SFR Definition 12.3. EIE1: Extended Interrupt Enable 1 109
SFR Definition 12.4. EIP1: Extended Interrupt Priority 1 110
SFR Definition 12.5. IT01CF: INT0/INT1 Configuration 112
SFR Definition 13.1. PFE0CN: Prefetch Engine Control 113

SFR Definition 14.1. VDM0CN: VDD Monitor Control 117
SFR Definition 14.2. RSTSRC: Reset Source 119
SFR Definition 15.1. PSCTL: Program Store R/W Control 125
SFR Definition 15.2. FLKEY: Flash Lock and Key 125
SFR Definition 15.3. FLSCL: Flash Scale 126
SFR Definition 16.1. EMI0CN: External Memory Interface Control 127
SFR Definition 17.1. OSCICN: Internal Oscillator Control 130
SFR Definition 17.2. OSCICL: Internal Oscillator Calibration 130
SFR Definition 17.3. OSCXCN: External Oscillator Control 134
SFR Definition 17.4. CLKMUL: Clock Multiplier Control 135
SFR Definition 17.5. CLKSEL: Clock Select 136
SFR Definition 18.1. XBR0: Port I/O Crossbar Register 0 142
SFR Definition 18.2. XBR1: Port I/O Crossbar Register 1 143
SFR Definition 18.3. P0: Port0 145
SFR Definition 18.4. P0MDIN: Port0 Input Mode 145
SFR Definition 18.5. P0MDOUT: Port0 Output Mode 146
SFR Definition 18.6. P0SKIP: Port0 Skip 146
SFR Definition 18.7. P1: Port1 147
SFR Definition 18.8. P1MDIN: Port1 Input Mode 147
SFR Definition 18.9. P1MDOUT: Port1 Output Mode 148
SFR Definition 18.10. P1SKIP: Port1 Skip 148
SFR Definition 18.11. P2: Port2 149
SFR Definition 18.12. P2MDOUT: Port2 Output Mode 149
SFR Definition 19.1. SMB0CF: SMBus Clock/Configuration 158
SFR Definition 19.2. SMB0CN: SMBus Control 160
SFR Definition 19.3. SMB0DAT: SMBus Data 162
SFR Definition 20.1. SCON0: Serial Port 0 Control 176
SFR Definition 20.2. SBUF0: Serial (UART0) Port Data Buffer 177
SFR Definition 21.1. SPI0CFG: SPI0 Configuration 187
SFR Definition 21.2. SPI0CN: SPI0 Control 188
SFR Definition 21.3. SPI0CKR: SPI0 Clock Rate 189
SFR Definition 21.4. SPI0DAT: SPI0 Data 190
SFR Definition 22.1. TCON: Timer Contro 199
SFR Definition 22.2. TMOD: Timer Mode 200
SFR Definition 22.3. CKCON: Clock Control 201
SFR Definition 22.4. TL0: Timer 0 Low Byte 202
SFR Definition 22.5. TL1: Timer 1 Low Byte 202
SFR Definition 22.6. TH0: Timer 0 High Byte 202
SFR Definition 22.7. TH1: Timer 1 High Byte 202
SFR Definition 22.8. TMR2CN: Timer 2 Control 205
SFR Definition 22.9. TMR2RLL: Timer 2 Reload Register Low Byte 206
SFR Definition 22.10. TMR2RLH: Timer 2 Reload Register High Byte 206
SFR Definition 22.11. TMR2L: Timer 2 Low Byte 206
SFR Definition 22.12. TMR2H Timer 2 High Byte 206
SFR Definition 22.13. TMR3CN: Timer 3 Control 209

SFR Definition 22.14. TMR3RLL: Timer 3 Reload Register Low Byte 210
SFR Definition 22.15. TMR3RLH: Timer 3 Reload Register High Byte 210
SFR Definition 22.16. TMR3L: Timer 3 Low Byte 210
SFR Definition 22.17. TMR3H Timer 3 High Byte 210
SFR Definition 23.1. PCA0CN: PCA Control 222
SFR Definition 23.2. PCA0MD: PCA Mode 223
SFR Definition 23.3. PCA0CPMn: PCA Capture/Compare Mode 224
SFR Definition 23.4. PCA0L: PCA Counter/Timer Low Byte 225
SFR Definition 23.5. PCA0H: PCA Counter/Timer High Byte 225
SFR Definition 23.6. PCA0CPLn: PCA Capture Module Low Byte 226
SFR Definition 23.7. PCA0CPHn: PCA Capture Module High Byte 226
C2 Register Definition 25.1. C2ADD: C2 Address 229
C2 Register Definition 25.2. DEVICEID: C2 Device ID 229
C2 Register Definition 25.3. REVID: C2 Revision ID 230
C2 Register Definition 25.4. FPCTL: C2 Flash Programming Control 230
C2 Register Definition 25.5. FPDAT: C2 Flash Programming Data 230

NOTES:

1. System Overview

C8051F350/1/2/3 devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 50 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- 24 or 16-bit single-ended/differential ADC with analog multiplexer
- Two 8-bit Current Output DACs
- Precision programmable 24.5 MHz internal oscillator
- 8 kB of on-chip Flash memory
- 768 bytes of on-chip RAM
- SMBus/I2C, Enhanced UART, and SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable counter/timer array (PCA) with three capture/compare modules and watchdog timer function
- On-chip power-on reset, V_{DD} monitor, and temperature sensor
- On-chip voltage comparator
- 17 Port I/O (5 V tolerant)

With on-chip power-on reset, V_{DD} monitor, watchdog timer, and clock oscillator, the C8051F350/1/2/3 devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 2.7 to 3.6 V operation over the industrial temperature range (–45 to +85 °C). The Port I/O and /RST pins are tolerant of input signals up to 5 V. The C8051F350/1/2/3 are available in 28-pin QFN (also referred to as MLP or MLF) or 32-pin LQFP packaging, as shown in Figure 1.1 through Figure 1.4.

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory	RAM	Calibrated Internal 24.5 MHz Oscillator	Clock Multiplier	SMBus/I2C	SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	24-bit ADC	16-bit ADC	Two 8-bit Current Output DACs	Internal Voltage Reference	Temperature Sensor	Analog Comparator	Lead-free (RoHS Compliant)	Package
C8051F350-GQ	50	8 kB	768	✓	✓	✓	✓	✓	4	✓	17	✓	—	✓	✓	✓	✓	✓	LQFP-32
C8051F351-GM	50	8 kB	768	✓	✓	✓	✓	✓	4	✓	17	✓	—	✓	✓	✓	✓	✓	QFN-28
C8051F352-GQ	50	8 kB	768	✓	✓	✓	✓	✓	4	✓	17	—	✓	✓	✓	✓	✓	✓	LQFP-32
C8051F353-GM	50	8 kB	768	✓	✓	✓	✓	✓	4	✓	17	—	✓	✓	✓	✓	✓	✓	QFN-28

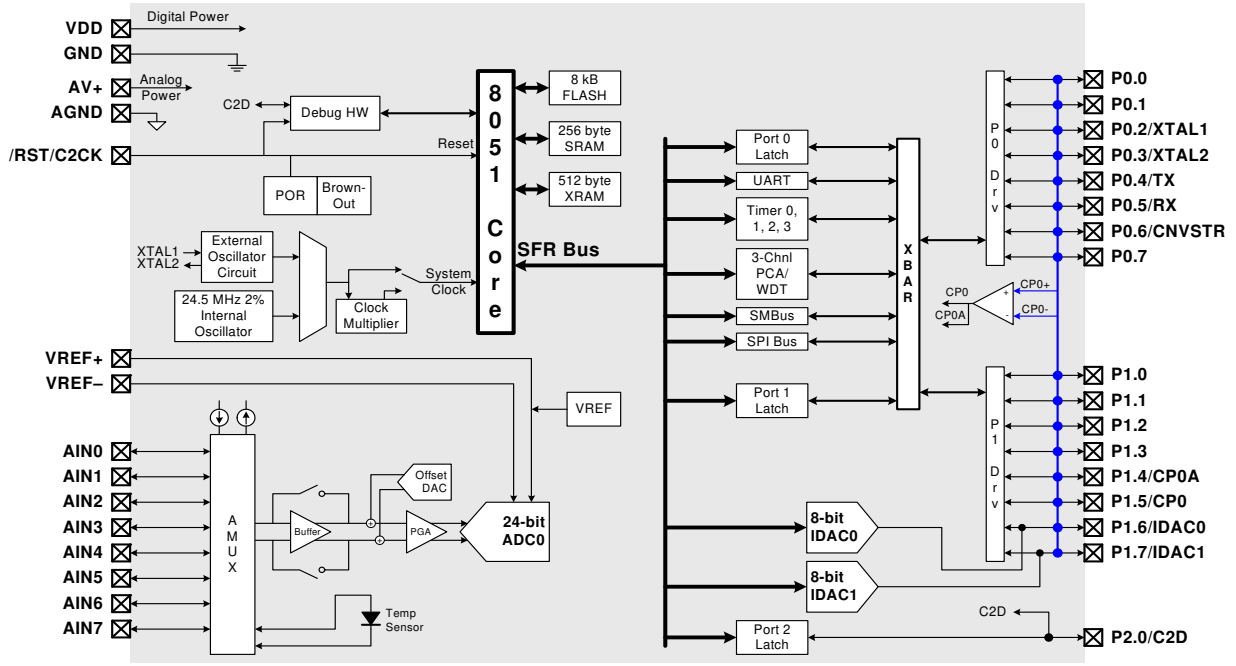


Figure 1.1. C8051F350 Block Diagram

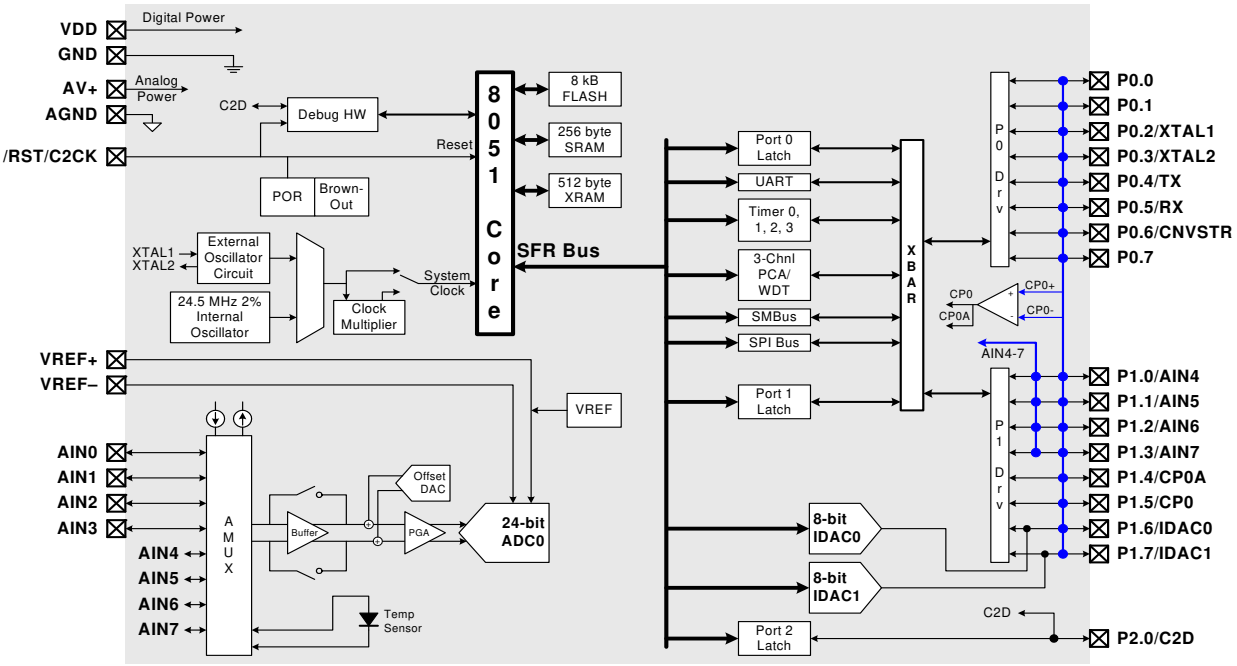


Figure 1.2. C8051F351 Block Diagram

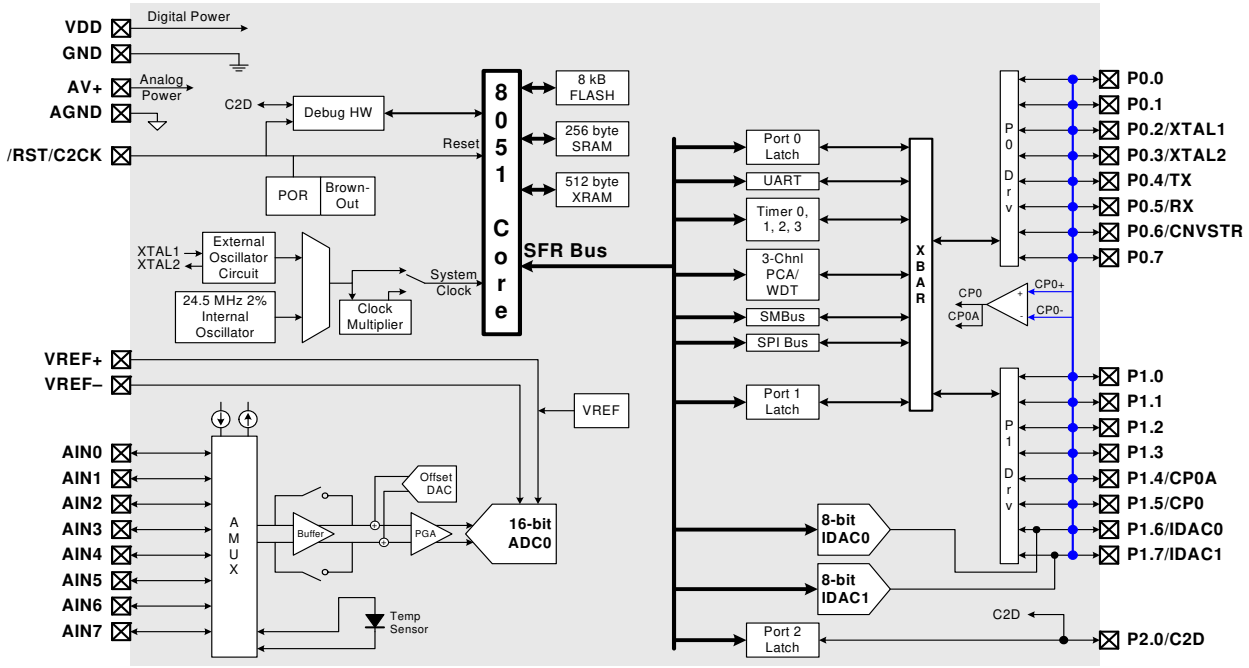


Figure 1.3. C8051F352 Block Diagram

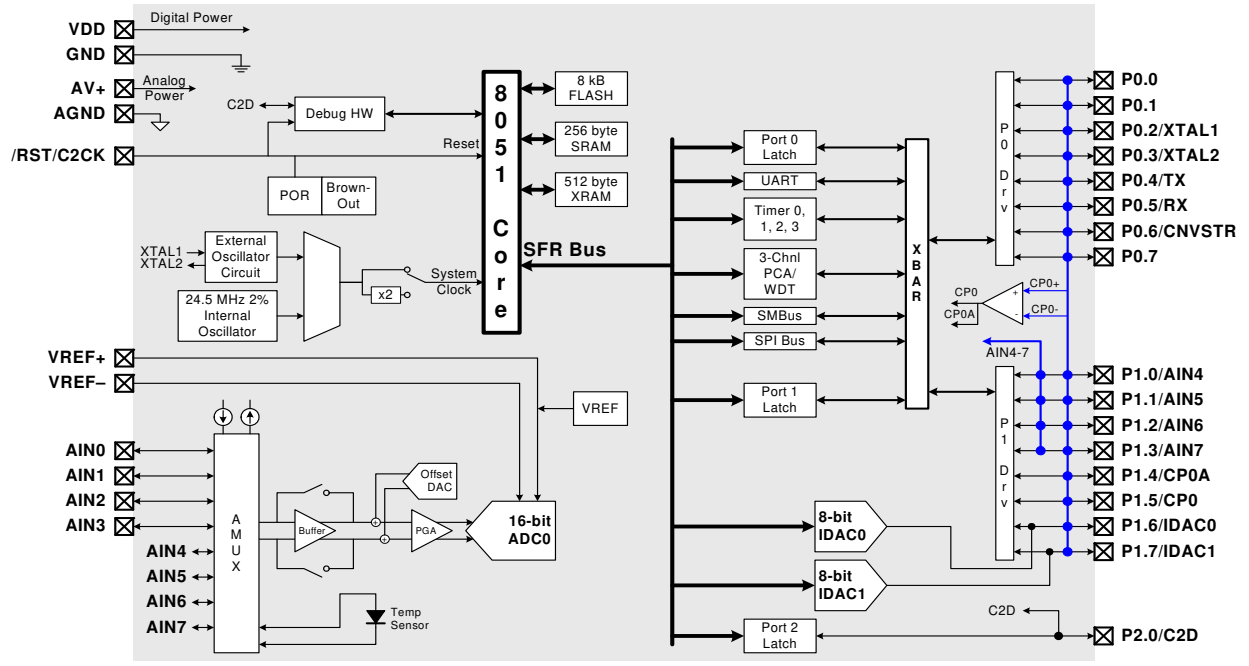


Figure 1.4. C8051F353 Block Diagram

1.1. CIP-51™ Microcontroller

1.1.1. Fully 8051 Compatible Instruction Set

The C8051F35x devices use Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set. Standard 803x/805x assemblers and compilers can be used to develop software. The C8051F35x family has a superset of all the peripherals included with a standard 8052.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute, and usually have a maximum system clock of 12 to 24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with no instructions taking more than eight system clock cycles.

With the CIP-51's system clock running at 50 MHz, it has a peak throughput of 50 MIPS. The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

1.1.3. Additional Features

The C8051F350/1/2/3 SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

An extended interrupt handler allows the numerous analog and digital peripherals to operate independently of the controller core and interrupt the controller only when necessary. By requiring less intervention from the microcontroller core, an interrupt-driven system is more efficient and allows for easier implementation of multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} monitor, a Watchdog Timer, a Missing Clock Detector, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an illegal Flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The internal oscillator is factory calibrated to 24.5 MHz ±2%. An external oscillator drive circuit is also included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. A clock multiplier allows for operation at up to 50 MHz. An external oscillator can also be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) source, while periodically switching to the fast internal oscillator as needed.

1.2. On-Chip Debug Circuitry

The C8051F350/1/2/3 devices include on-chip Silicon Labs 2-Wire (C2) debug circuitry that provides non-intrusive, full speed, in-circuit debugging of the production part *installed in the end application.*

Silicon Labs' debugging system supports inspection and modification of memory and registers, breakpoints, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the ADC and SMBus) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F350DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F35x MCUs. The kit includes software with a developer's studio and debugger, a C2 debug adapter, a target application board with the associated MCU installed, and the required cables and wall-mount power supply. The development kit requires a computer with Windows 98 SE or later installed.

The Silicon Labs IDE interface is a vastly superior developing and debugging configuration, compared to standard MCU emulators that use on-board "ICE Chips" and require the MCU in the application board to be socketed. Silicon Labs' debug paradigm increases ease of use and preserves the performance of the precision analog peripherals.

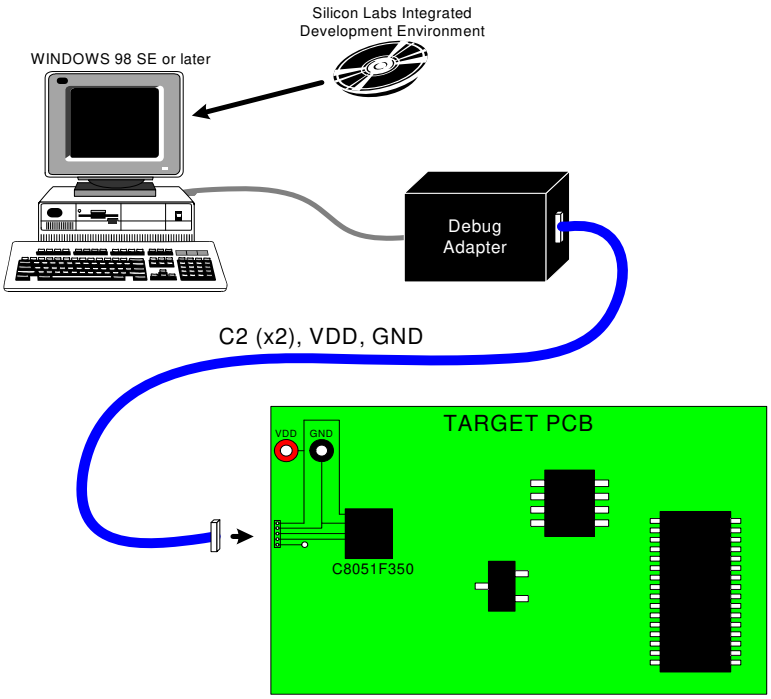


Figure 1.5. Development/In-System Debug Diagram

1.3. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

Program memory consists of 8 kB bytes of Flash. This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage.

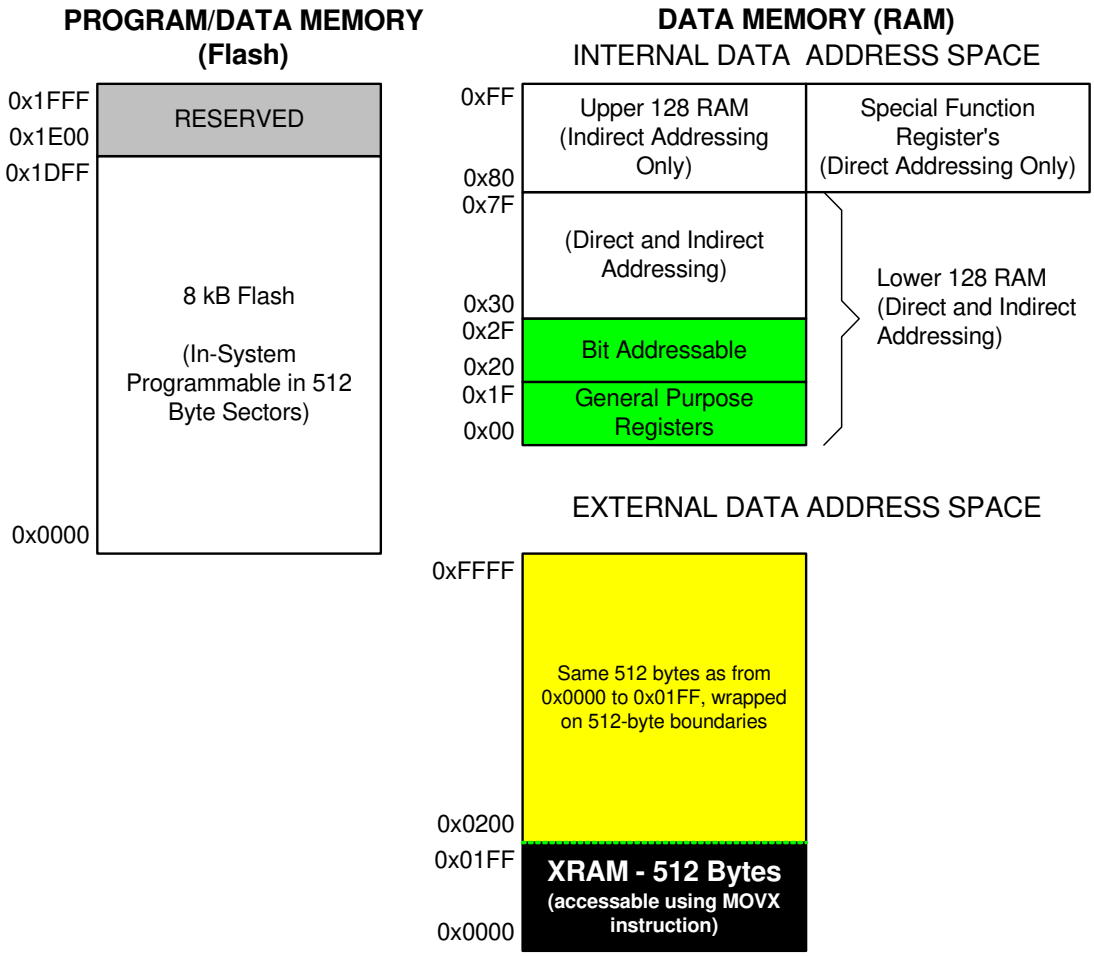


Figure 1.6. Memory Map

1.4. 24 or 16-Bit Analog to Digital Converter (ADC0)

The C8051F350/1/2/3 include a fully-differential, 24-bit (C8051F350/1) or 16-bit (C8051F352/3) Sigma-Delta Analog to Digital Converter (ADC) with on-chip calibration capabiliites. Two separate decimation filters can be programmed for throughputs of up to 1 kHz. An internal 2.5 V reference is available, or a differential external reference can be used for ratiometric measurements. A Programmable Gain Amplifier (PGA) is included, with eight gain settings up to 128x. An analog front-end multiplexer connects the differential inputs to eight external pins, the internal temperature sensor, or AGND. The on-chip input buffers can be used to provide a high input impedance for direct connection to sensitive transducers. An 8-bit offset DAC allows for correction of large input offset voltages.

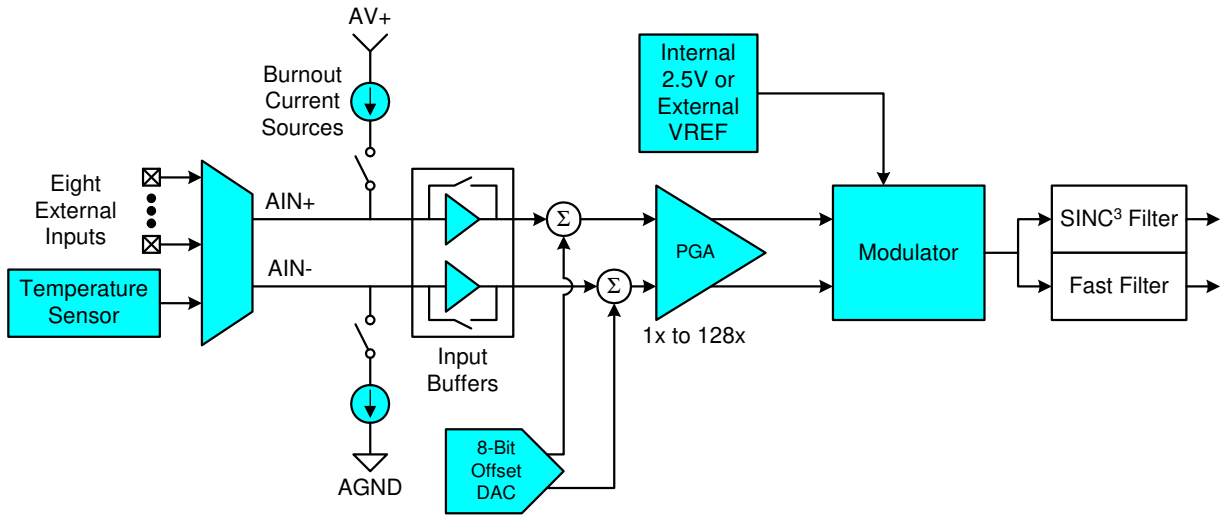


Figure 1.7. ADC0 Block Diagram

1.5. Two 8-bit Current-Mode DACs

The C8051F350/1/2/3 devices include two 8-bit current-mode Digital-to-Analog Converters (IDACs). The maximum current output of the IDACs can be adjusted for four different current settings; 0.25 mA, 0.5 mA, 1 mA, and 2 mA. A flexible output update mechanism allows for seamless full-scale changes, and supports jitter-free updates for waveform generation. IDAC updates can be performed on-demand, scheduled on a Timer overflow, or synchronized with an external signal. Figure 1.8 shows a block diagram of the IDAC circuitry.

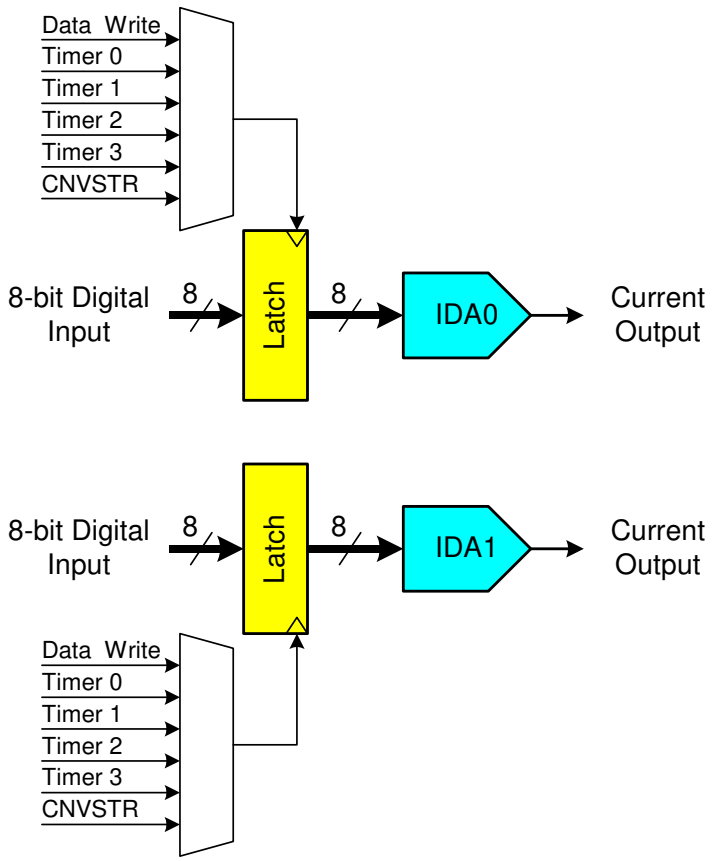


Figure 1.8. IDAC Block Diagram