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C8051F360/1/2/3/4/5/6/7/8/9

Mixed Signal ISP Flash MCU Family

Analog Peripherals
- **10-Bit ADC ('F360/1/2/6/7/8/9 only)**
  - Up to 200 ksps
  - Up to 21 external single-ended or differential inputs
  - VREF from internal VREF, external pin or V_{DD}
  - Internal or external start of conversion source
  - Built-in temperature sensor
- **10-Bit Current Output DAC ('F360/1/2/6/7/8/9 only)**
- **Two Comparators**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source
  - Low current (0.4 µA)
- **Brown-out detector and POR Circuitry**

On-Chip Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Low cost, **complete** development kit

Supply Voltage
- Range: 2.7–3.6 V (50 MIPS) 3.0–3.6 V (100 MIPS)
- Power saving suspend and shutdown modes

High Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 100 MIPS or 50 MIPS throughput with on-chip PLL
- Expanded interrupt handler
- 2-cycle 16 x 16 MAC engine

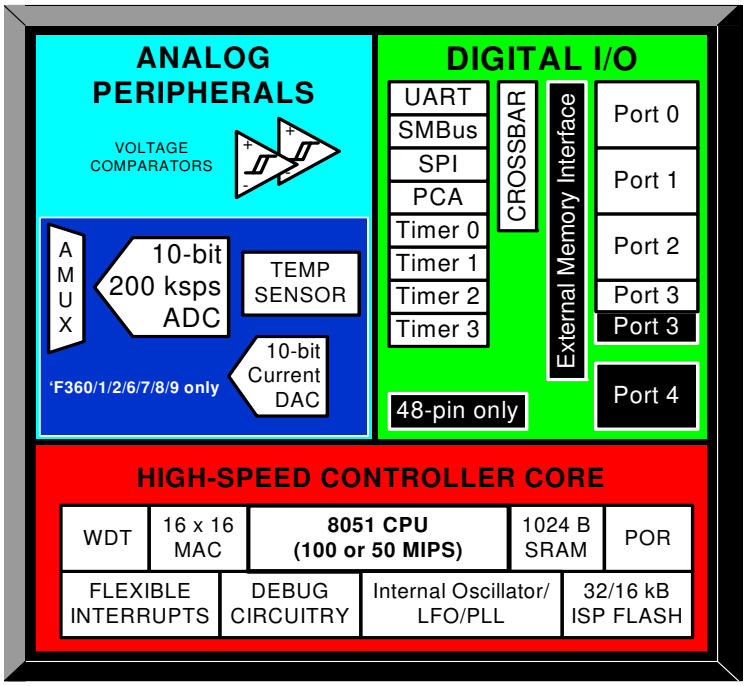
Memory
- 1280 bytes internal data RAM (256 + 1024)
- 32 kB ('F360/1/2/3/4/5/6/7) or 16 kB ('F368/9) Flash; In-system programmable in 1024-byte Sectors—1024 bytes are reserved in the 32 kB devices

Digital Peripherals
- up to 39 Port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART, SMBus™, and enhanced SPI™ serial ports
- Four general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with six capture/compare modules
- Real time clock mode using PCA or timer and external clock source
- External Memory Interface (EMIF)

Clock Sources
- Two internal oscillators:
  - 24.5 MHz with ±2% accuracy supports crystal-less UART operation
  - 80/40/20/10 kHz low frequency, low power
- Flexible PLL technology
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly; useful in power saving modes

Packages
- 48-pin TQFP (C8051F360/3)
- 32-pin LQFP (C8051F361/4/6/8)
- 28-pin QFN (C8051F362/5/7/9)

Temperature Range: –40 to +85 °C



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1. System Overview

C8051F36x devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 100 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 10-bit 200 ksps 16-channel single-ended/differential ADC with analog multiplexer
- 10-bit Current Output DAC
- 2-cycle 16 by 16 Multiply and Accumulate Engine
- Precision programmable 25 MHz internal oscillator
- Up to 32 kB of on-chip Flash memory—1024 bytes are reserved
- 1024 bytes of on-chip RAM
- External Data Memory Interface with 64 kB address space
- SMBus/I2C, Enhanced UART, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with six capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, V_{DD} Monitor, and Temperature Sensor
- Two on-chip Voltage Comparators
- up to 39 Port I/O (5 V tolerant)

With on-chip Power-On Reset, V_{DD} Monitor, Watchdog Timer, and clock oscillator, the C8051F36x devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 3.0 to 3.6 V (100 MIPS) operation or 2.7 to 3.6 V (50 MIPS) operation over the industrial temperature range (–40 to +85 °C). The Port I/O and $\overline{\text{RST}}$ pins are tolerant of input signals up to 5 V. The C8051F36x devices are available in 48-pin TQFP packages, and C8051F36x devices are available in 32-pin LQFP and 28-pin QFN packages (also referred to as MLP or MLF packages). All package types are lead-free (RoHS compliant). See Table 1.1 for ordering part numbers. Block diagrams are included in Figure 1.1, Figure 1.2, and Figure 1.3.

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)	RAM (bytes)	2-cycle 16 by 16 MAC	Calibrated Internal 24.5 MHz Oscillator	Internal 80 kHz Oscillator	External Memory Interface	SMBus/I^2C	Enhanced SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 200ksps ADC	10-bit Current Output DAC	Internal Voltage Reference	Temperature Sensor	Analog Comparators	Lead-free (RoHS Compliant)	Package
C8051F360-C-GQ	100	32	1024	✓	✓	✓	✓	✓	✓	✓	4	✓	39	✓	✓	✓	✓	2	✓	TQFP-48
C8051F361-C-GQ[1]	100	32	1024	✓	✓	✓	—	✓	✓	✓	4	✓	29	✓	✓	✓	✓	2	✓	LQFP-32
C8051F362-C-GM[2]	100	32	1024	✓	✓	✓	—	✓	✓	✓	4	✓	25	✓	✓	✓	✓	2	✓	QFN-28
C8051F363-C-GQ	100	32	1024	✓	✓	✓	✓	✓	✓	✓	4	✓	39	—	—	—	—	2	✓	TQFP-48
C8051F364-C-GQ[1]	100	32	1024	✓	✓	✓	—	✓	✓	✓	4	✓	29	—	—	—	—	2	✓	LQFP-32
C8051F365-C-GM[2]	100	32	1024	✓	✓	✓	—	✓	✓	✓	4	✓	25	—	—	—	—	2	✓	QFN-28
C8051F366-C-GQ[1]	50	32	1024	✓	✓	✓	—	✓	✓	✓	4	✓	29	✓	✓	✓	✓	2	✓	LQFP-32
C8051F367-C-GM[2]	50	32	1024	✓	✓	✓	—	✓	✓	✓	4	✓	25	✓	✓	✓	✓	2	✓	QFN-28
C8051F368-C-GQ[1]	50	16	1024	✓	✓	✓	—	✓	✓	✓	4	✓	29	✓	✓	✓	✓	2	✓	LQFP-32
C8051F369-C-GM[2]	50	16	1024	✓	✓	✓	—	✓	✓	✓	4	✓	25	✓	✓	✓	✓	2	✓	QFN-28

Notes:
1. Pin compatible with the C8051F310-GQ.
2. Pin compatible with the C8051F311-GM.

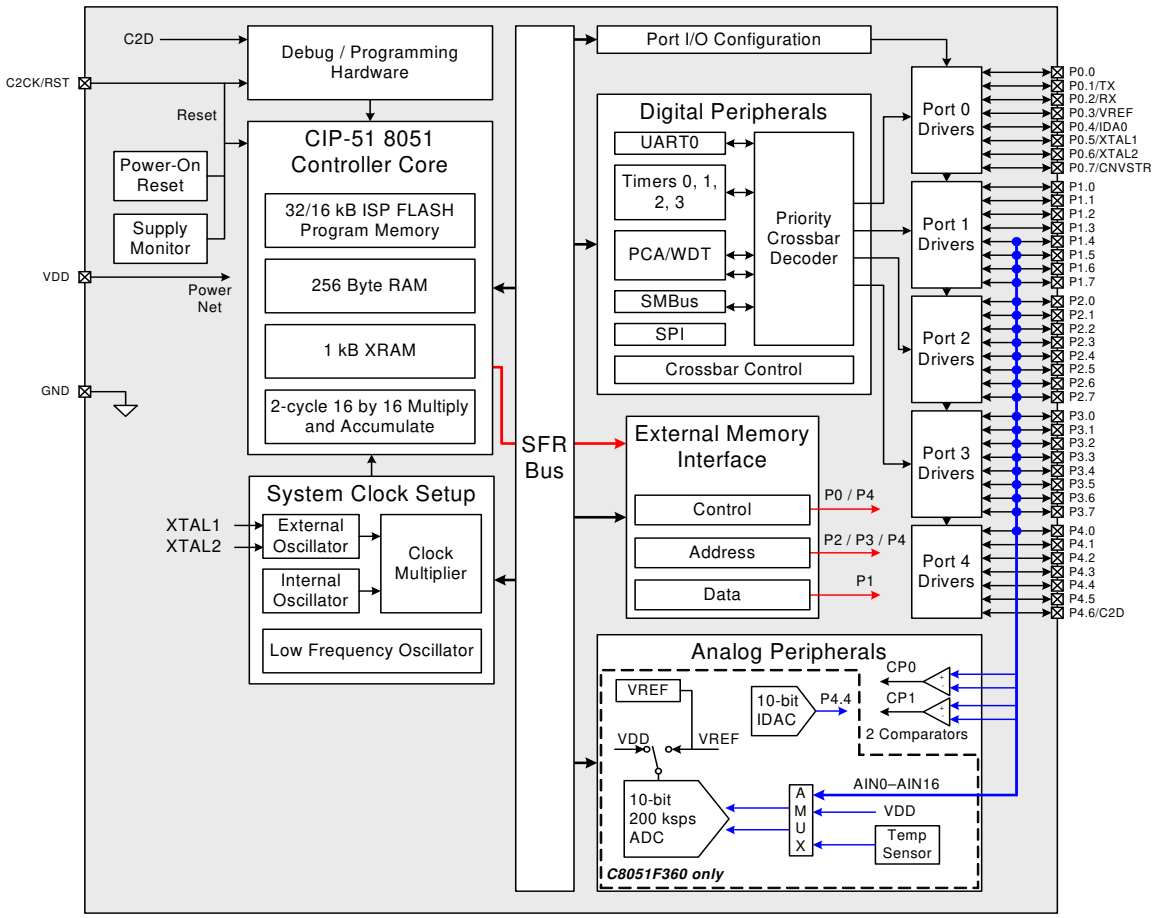

Figure 1.1. C8051F360/3 Block Diagram

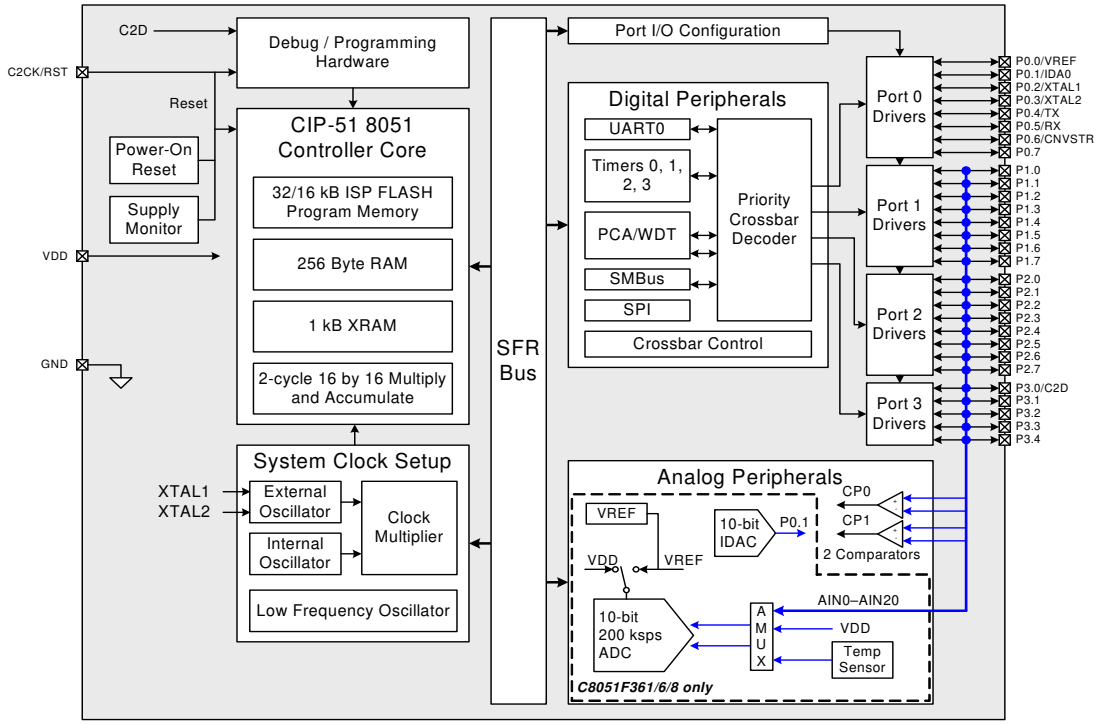

Figure 1.2. C8051F361/4/6/8 Block Diagram

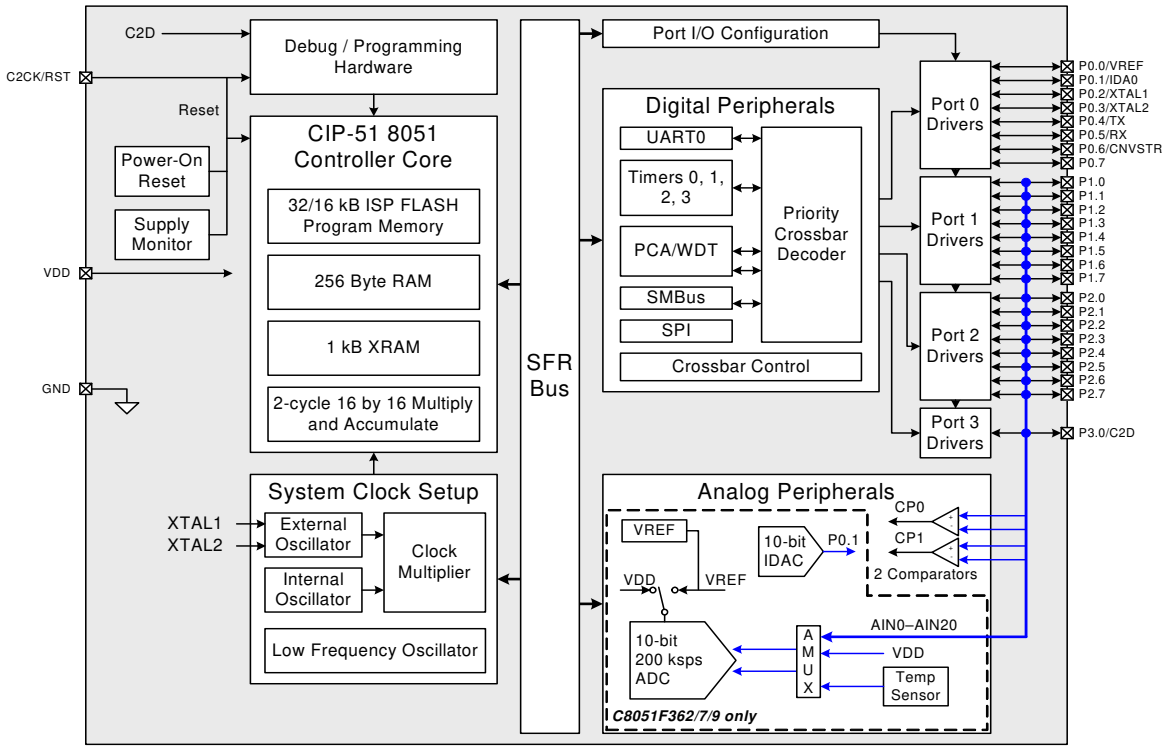

Figure 1.3. C8051F362/5/7/9 Block Diagram

1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F36x family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052, including four 16-bit counter/timers, a full-duplex UART with extended baud rate configuration, an enhanced SPI port, 1024 bytes of internal RAM, 128 byte Special Function Register (SFR) address space, and up to 39 I/O pins.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 100 MHz, it has a peak throughput of 100 MIPS. Figure 1.4 shows a comparison of peak throughputs for various 8-bit microcontroller cores with their maximum system clocks.

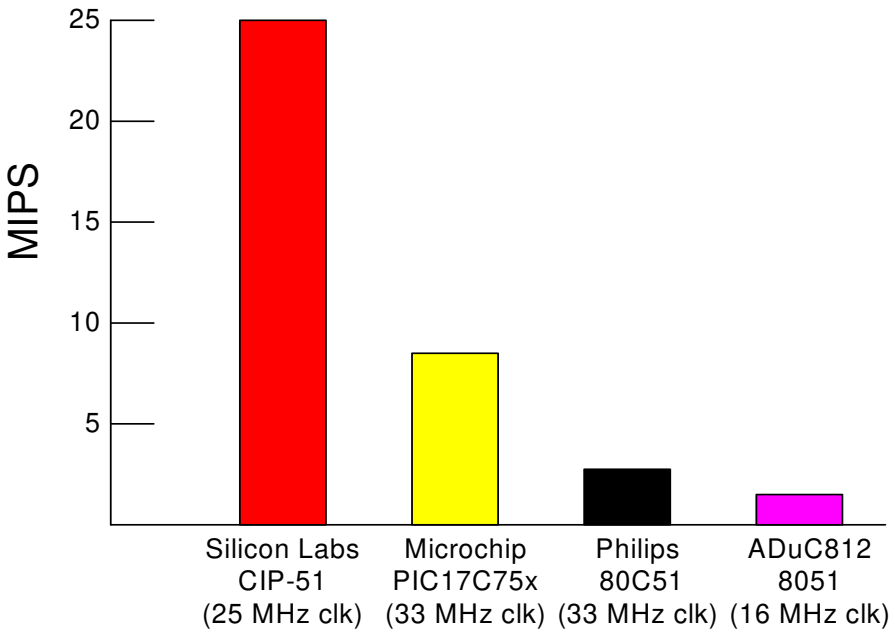

Figure 1.4. Comparison of Peak MCU Execution Speeds

1.1.3. Additional Features

The C8051F36x SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides 16 interrupt sources into the CIP-51 (as opposed to 7 for the standard 8051), allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} Monitor (forces reset when power supply voltage drops below V_{RST} as given in Table 12.1 on page 134), a Watchdog Timer, a Missing Clock Detector, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an illegal Flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The internal oscillator factory calibrated to 24.5 MHz ±2%. This internal oscillator period may be user programmed in ~0.5% increments. An additional low-frequency oscillator is also available which facilitates low-power operation. An external oscillator drive circuit is included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. If desired, the system clock source may be switched on-the-fly between both internal and external oscillator circuits. An external oscillator can also be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) source, while periodically switching to the fast (up to 25 MHz) internal oscillator as needed. Additionally, an on-chip PLL is provided to achieve higher system clock speeds for increased throughput.

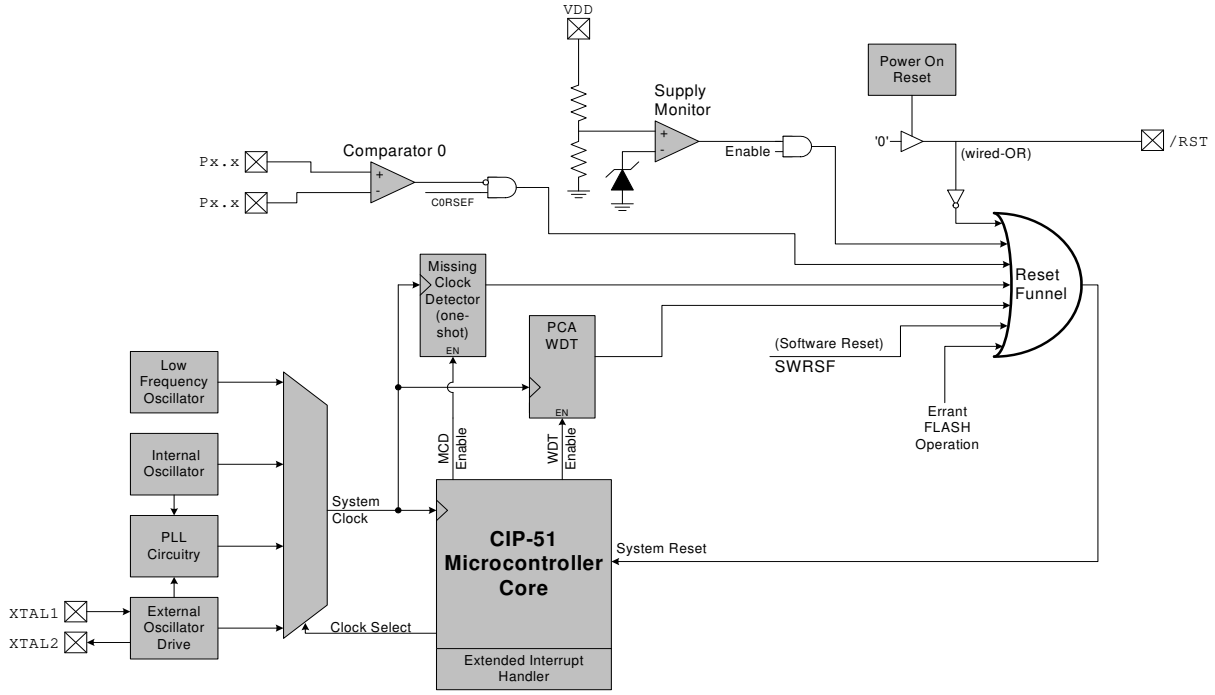

Figure 1.5. On-Chip Clock and Reset

1.2. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

Program memory consists of 32/16 kB of Flash. This memory may be reprogrammed in-system in 1024 byte sectors, and requires no special off-chip programming voltage. See Figure 1.6 for the MCU system memory map.

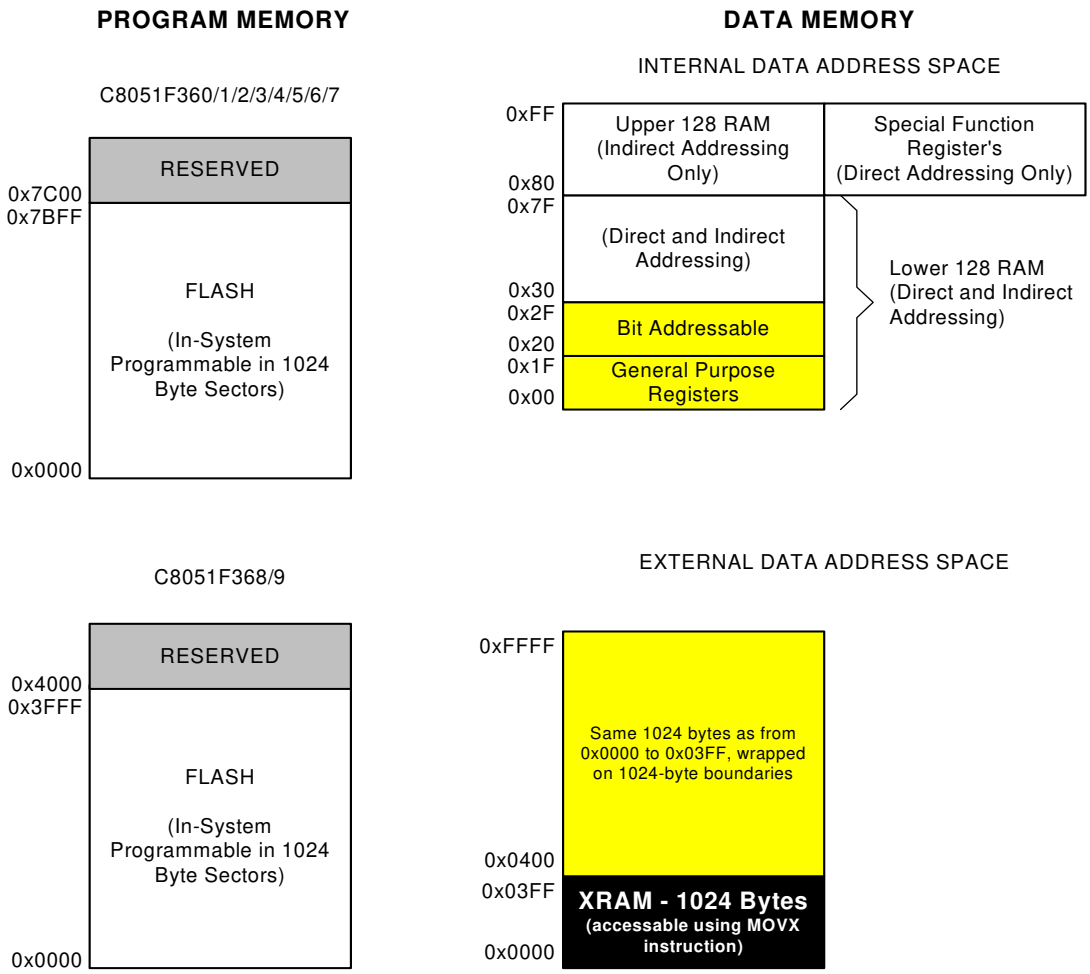

Figure 1.6. On-Board Memory Map

1.3. On-Chip Debug Circuitry

The C8051F36x devices include on-chip Silicon Labs 2-Wire (C2) debug circuitry that provides non-intrusive, full speed, in-circuit debugging of the production part *installed in the end application.*

Silicon Labs' debugging system supports inspection and modification of memory and registers, breakpoints, and single stepping. No additional target RAM, program memory, timers, or communications chan-

nels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the ADC and SMBus) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F360DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F36x MCUs. The kit includes software with a developer's studio and debugger, an integrated 8051 assembler, and a debug adapter. It also has a target application board with the associated MCU installed and prototyping area, plus the required cables, and wall-mount power supply. The Development Kit requires a PC running Windows98SE or later.

The Silicon Labs IDE interface is a vastly superior developing and debugging configuration, compared to standard MCU emulators that use on-board "ICE Chips" and require the MCU in the application board to be socketed. Silicon Labs' debug paradigm increases ease of use and preserves the performance of the precision analog peripherals.

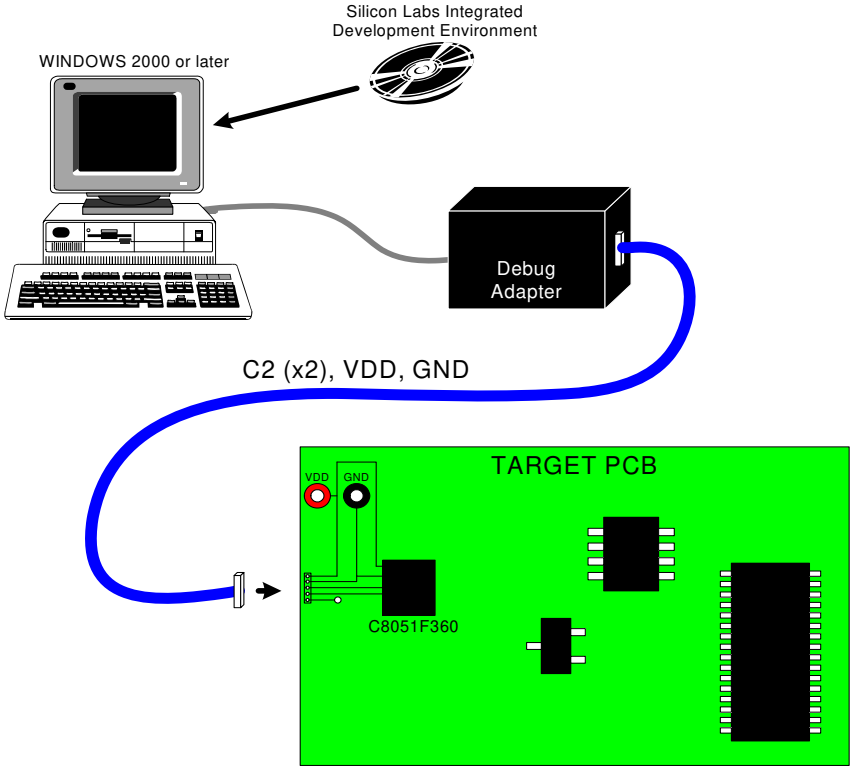

Figure 1.7. Development/In-System Debug Diagram

1.4. Programmable Digital I/O and Crossbar

C8051F36x devices include up to 39 I/O pins (four byte-wide Ports and one 7-bit-wide Port). The C8051F36x Ports behave like typical 8051 Ports with a few enhancements. Each Port pin may be configured as an analog input or a digital I/O pin. Pins selected as digital I/Os may additionally be configured for push-pull or open-drain output. The “weak pullups” that are fixed on typical 8051 devices may be globally disabled, providing power savings capabilities.