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C8051F388/9/A/B

Flash MCU Family

Analog Peripherals
- **10-Bit ADC**
  - Up to 500 ksps
  - Built-in analog multiplexer with single-ended and differential mode
  - VREF from external pin, internal reference, or V_{DD}
  - Built-in temperature sensor
  - External conversion start input option
- **Two comparators**
- **Internal voltage reference**
- **Brown-out detector and POR Circuitry**

On-Chip Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (No emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Voltage Supply Input: 2.7 to 5.25 V
- Voltages from 2.7 to 5.25 V supported using On-Chip Voltage Regulators

High Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 48 MIPS operation
- Expanded interrupt handler

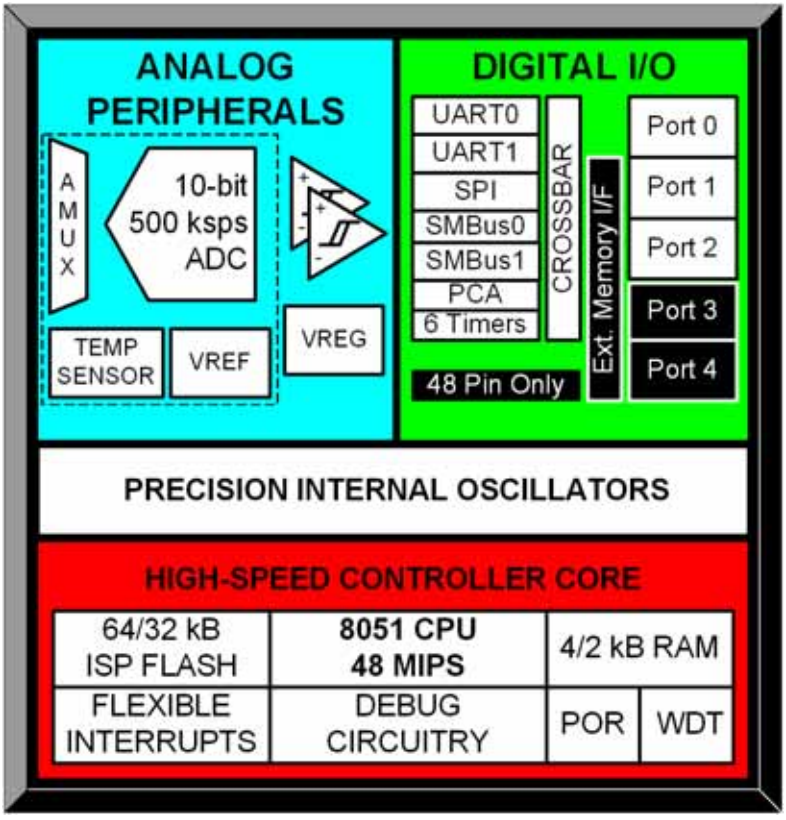
Memory
- 4352 or 2304 Bytes RAM
- 64 or 32 kB Flash; In-system programmable in 512-byte sectors

Digital Peripherals
- 40/25 Port I/O; All 5 V tolerant with high sink current
- Hardware enhanced SPI™, two I^2C/SMBus™, and two enhanced UART serial ports
- Six general purpose 16-bit counter/timers
- 16-bit programmable counter array (PCA) with five capture/compare modules
- External Memory Interface (EMIF)

Clock Sources
- Internal Oscillator: ±1.5% accuracy. Supports all UART modes
- External Oscillator: Crystal, RC, C, or clock (1 or 2 Pin modes)
- Low Frequency (80 kHz) Internal Oscillator
- Can switch between clock sources on-the-fly

Packages
- 48-pin TQFP (C8051F388/A)
- 32-pin LQFP (C8051F389/B)
- 5x5 mm 32-pin QFN (C8051F389/B)

Temperature Range: –40 to +85 °C



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1. System Overview

C8051F388/9/A/B devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 48 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- Supply Voltage Regulator
- True 10-bit 500 ksps differential / single-ended ADC with analog multiplexer
- On-chip Voltage Reference and Temperature Sensor
- On-chip Voltage Comparators (2)
- Precision internal calibrated 48 MHz internal oscillator
- Internal low-frequency oscillator for additional power savings
- Up to 64 kB of on-chip Flash memory
- Up to 4352 Bytes of on-chip RAM (256 + 4 kB)
- External Memory Interface (EMIF) available on 48-pin versions.
- 2 I^2C/SMBus, 2 UARTs, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with five capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, V_{DD} Monitor, and Missing Clock Detector
- Up to 40 Port I/O (5 V tolerant)

With on-chip Power-On Reset, V_{DD} monitor, Voltage Regulator, Watchdog Timer, and clock oscillator, C8051F388/9/A/B devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 2.7–5.25 V operation over the industrial temperature range (–40 to +85 °C). For voltages above 3.6 V, the on-chip Voltage Regulator must be used. The Port I/O and $\overline{RST}$ pins are tolerant of input signals up to 5 V. C8051F388/9/A/B devices are available in 48-pin TQFP, 32-pin LQFP, or 32-pin QFN packages. See Table 1.1, “Product Selection Guide,” on page 16 for feature and package choices.

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (Bytes)	RAM	Calibrated Internal Oscillator	Low Frequency Oscillator	Supply Voltage Regulator	SMBus/I2C	Enhanced SPI	UARTs	Timers (16-bit)	Programmable Counter Array	Digital Port I/O	External Memory Interface (EMIF)	10-bit 500ksps ADC	Temperature Sensor	Voltage Reference	Analog Comparators	Package
C8051F388-B-GQ	48	64k	4352	✓	✓	✓	2	✓	2	6	✓	40	✓	✓	✓	✓	2	TQFP48
C8051F389-B-GQ	48	64k	4352	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	LQFP32
C8051F389-B-GM	48	64k	4352	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	QFN32
C8051F38A-B-GQ	48	32k	2304	✓	✓	✓	2	✓	2	6	✓	40	✓	✓	✓	✓	2	TQFP48
C8051F38B-B-GQ	48	32k	2304	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	LQFP32
C8051F38B-B-GM	48	32k	2304	✓	✓	✓	2	✓	2	6	✓	25	—	✓	✓	✓	2	QFN32

Note: Starting with silicon revision B, the ordering part numbers have been updated to include the silicon revision and use this format: "C8051F388-B-GQ".

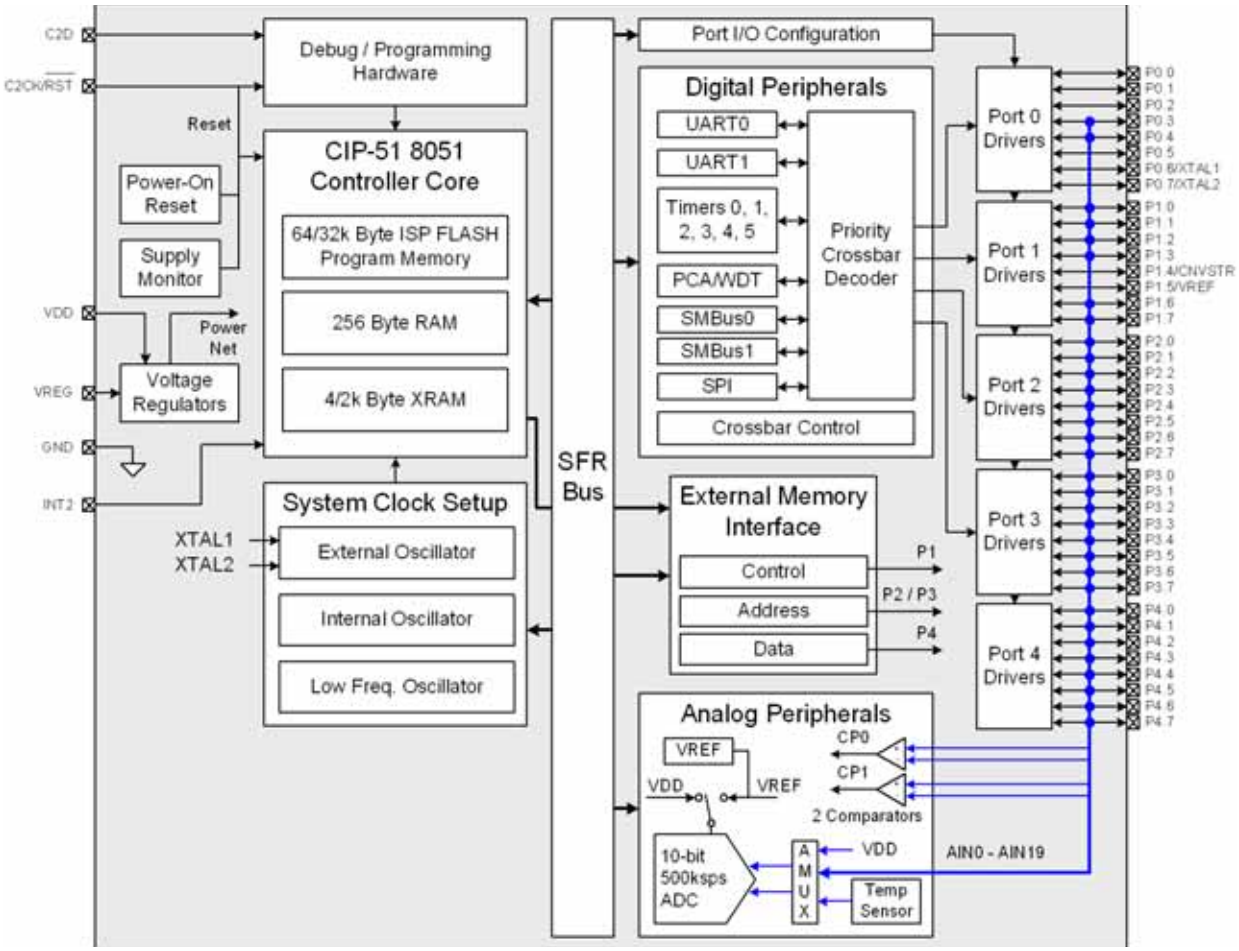

Figure 1.1. C8051F388/A Block Diagram

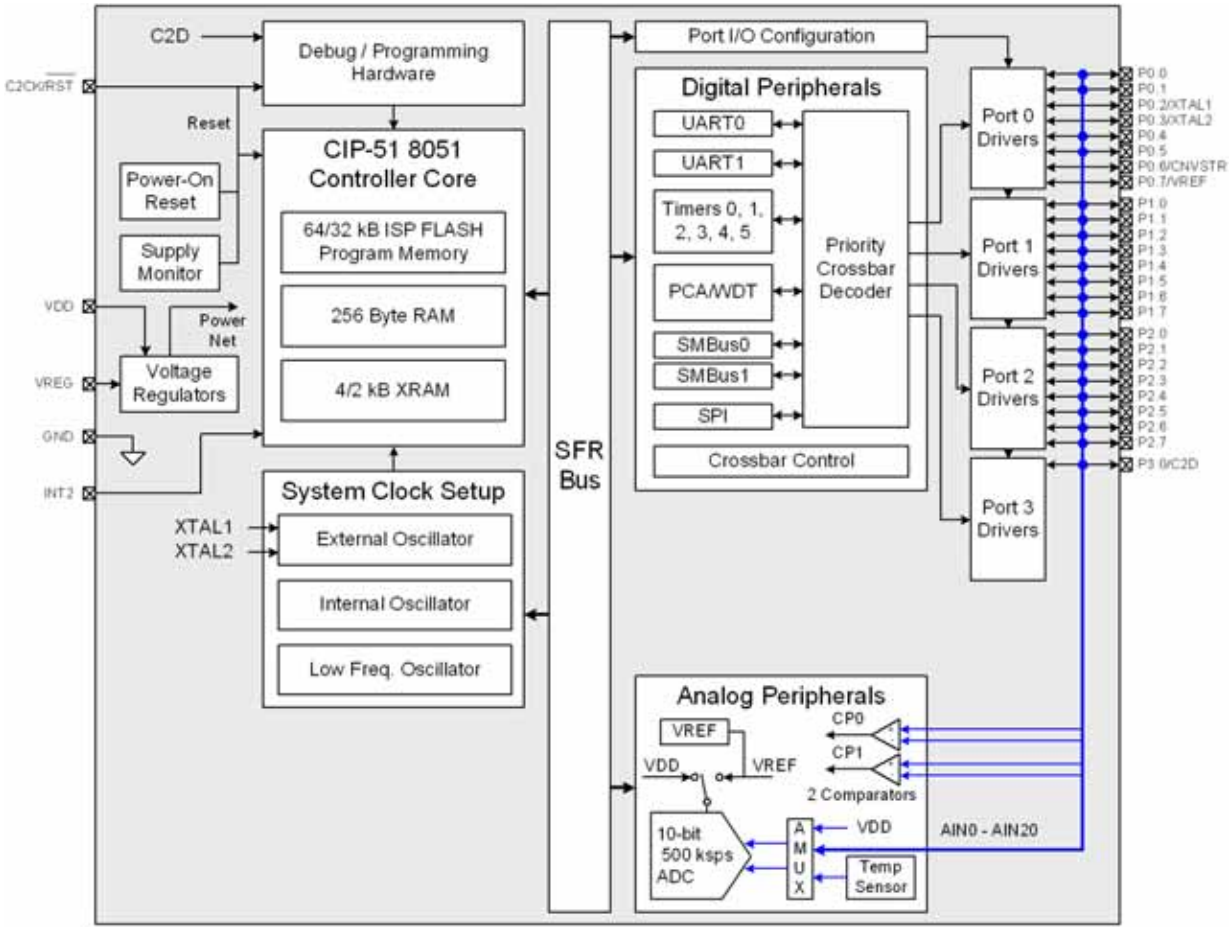

Figure 1.2. C8051F389/B Block Diagram

2. C8051F34x Compatibility

The C8051F388/9/A/B family is designed to be a pin and code compatible replacement for the C8051F34x device family. The C8051F388/9/A/B device should function as a drop-in replacement for the C8051F34x devices in most applications that do not use USB. Table 2.1 lists recommended replacement part numbers for C8051F34x devices. See “2.1. Hardware Incompatibilities” to determine if any changes are necessary when upgrading an existing C8051F34x design to the C8051F388/9/A/B.

Table 2.1. C8051F388/9/A/B Replacement Part Numbers

C8051F34x Part Number	C8051F38x Part Number
C8051F340-GQ	C8051F388-B-GQ
C8051F341-GQ	C8051F38A-B-GQ
C8051F342-GQ	C8051F389-B-GQ
C8051F342-GM	C8051F389-B-GM
C8051F343-GQ	C8051F38B-B-GQ
C8051F343-GM	C8051F38B-B-GM
C8051F344-GQ	C8051F388-B-GQ
C8051F345-GQ	C8051F38A-B-GQ
C8051F346-GQ	C8051F389-B-GQ
C8051F346-GM	C8051F389-B-GM
C8051F347-GQ	C8051F38B-B-GQ
C8051F347-GM	C8051F38B-B-GM
C8051F348-GQ	C8051F38A-B-GQ
C8051F349-GQ	C8051F38B-B-GQ
C8051F349-GM	C8051F38B-B-GM
C8051F34A-GQ	C8051F389-B-GQ
C8051F34A-GM	C8051F389-B-GM
C8051F34B-GQ	C8051F38B-B-GQ
C8051F34B-GM	C8051F38B-B-GM
C8051F34C-GQ	C8051F388-B-GQ
C8051F34D-GQ	C8051F389-B-GQ

2.1. Hardware Incompatibilities

While the C8051F388/9/A/B family includes a number of new features not found on the C8051F34x family, there are some differences that should be considered for any design port.

- **Clock Multiplier**: The C8051F388/9/A/B does not include the 4x clock multiplier from the C8051F34x device families. This change only impacts systems which use the clock multiplier in conjunction with an external oscillator source.
- **USB**: The C8051F388/9/A/B devices do not include the USB module.
- **External Oscillator C and RC Modes**: The C and RC modes of the oscillator have a divide-by-2 stage on the C8051F388/9/A/B to aid in noise immunity. This was not present on the C8051F34x device family, and any clock generated with C or RC mode will change accordingly.
- **Fab Technology**: The C8051F388/9/A/B is manufactured using a different technology process than the C8051F34x. As a result, many of the electrical performance parameters will have subtle differences. These differences should not affect most systems but it is nonetheless important to review the electrical parameters for any blocks that are used in the design, and ensure they are compatible with the existing hardware.

3. Pinout and Package Definitions

Table 3.1. Pin Definitions for the C8051F388/9/A/B

Name	Pin Numbers		Type	Description
	48-pin	32-pin		
V_{DD}	10	6	Power In Power Out	2.7–3.6 V Power Supply Voltage Input. 3.3 V Voltage Regulator Output.
GND	7	3		Ground.
$\overline{RST}$/ C2CK	13	9	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 15 µs. Clock signal for the C2 Debug Interface.
C2D	14	—	D I/O	Bi-directional data signal for the C2 Debug Interface.
P3.0 / C2D	—	10	D I/O D I/O	Port 3.0. See Section 20 for a complete description of Port 3. Bi-directional data signal for the C2 Debug Interface.
REGIN	11	7	Power In	5 V Regulator Input. This pin is the input to the on-chip voltage regulator.
INT2	12	8	D In	INT2 interrupt input.
NC	8	4		This pin is a no-connect and can be left floating.
NC	9	5		This pin is a no-connect and can be left floating.
P0.0	6	2	D I/O or A In	Port 0.0. See Section 20 for a complete description of Port 0.
P0.1	5	1	D I/O or A In	Port 0.1.
P0.2	4	32	D I/O or A In	Port 0.2.
P0.3	3	31	D I/O or A In	Port 0.3.
P0.4	2	30	D I/O or A In	Port 0.4.
P0.5	1	29	D I/O or A In	Port 0.5.
P0.6	48	28	D I/O or A In	Port 0.6.
P0.7	47	27	D I/O or A In	Port 0.7.

Table 3.1. Pin Definitions for the C8051F388/9/A/B (Continued)

Name	Pin Numbers		Type	Description
	48-pin	32-pin		
P1.0	46	26	D I/O or A In	Port 1.0. See Section 20 for a complete description of Port 1.
P1.1	45	25	D I/O or A In	Port 1.1.
P1.2	44	24	D I/O or A In	Port 1.2.
P1.3	43	23	D I/O or A In	Port 1.3.
P1.4	42	22	D I/O or A In	Port 1.4.
P1.5	41	21	D I/O or A In	Port 1.5.
P1.6	40	20	D I/O or A In	Port 1.6.
P1.7	39	19	D I/O or A In	Port 1.7.
P2.0	38	18	D I/O or A In	Port 2.0. See Section 20 for a complete description of Port 2.
P2.1	37	17	D I/O or A In	Port 2.1.
P2.2	36	16	D I/O or A In	Port 2.2.
P2.3	35	15	D I/O or A In	Port 2.3.
P2.4	34	14	D I/O or A In	Port 2.4.
P2.5	33	13	D I/O or A In	Port 2.5.
P2.6	32	12	D I/O or A In	Port 2.6.
P2.7	31	11	D I/O or A In	Port 2.7.
P3.0	30	—	D I/O or A In	Port 3.0. See Section 20 for a complete description of Port 3.
P3.1	29	—	D I/O or A In	Port 3.1.

Table 3.1. Pin Definitions for the C8051F388/9/A/B (Continued)

Name	Pin Numbers		Type	Description
	48-pin	32-pin		
P3.2	28	—	D I/O or A In	Port 3.2.
P3.3	27	—	D I/O or A In	Port 3.3.
P3.4	26	—	D I/O or A In	Port 3.4.
P3.5	25	—	D I/O or A In	Port 3.5.
P3.6	24	—	D I/O or A In	Port 3.6.
P3.7	23	—	D I/O or A In	Port 3.7.
P4.0	22	—	D I/O or A In	Port 4.0. See Section 20 for a complete description of Port 4.
P4.1	21	—	D I/O or A In	Port 4.1.
P4.2	20	—	D I/O or A In	Port 4.2.
P4.3	19	—	D I/O or A In	Port 4.3.
P4.4	18	—	D I/O or A In	Port 4.4.
P4.5	17	—	D I/O or A In	Port 4.5.
P4.6	16	—	D I/O or A In	Port 4.6.
P4.7	15	—	D I/O or A In	Port 4.7.

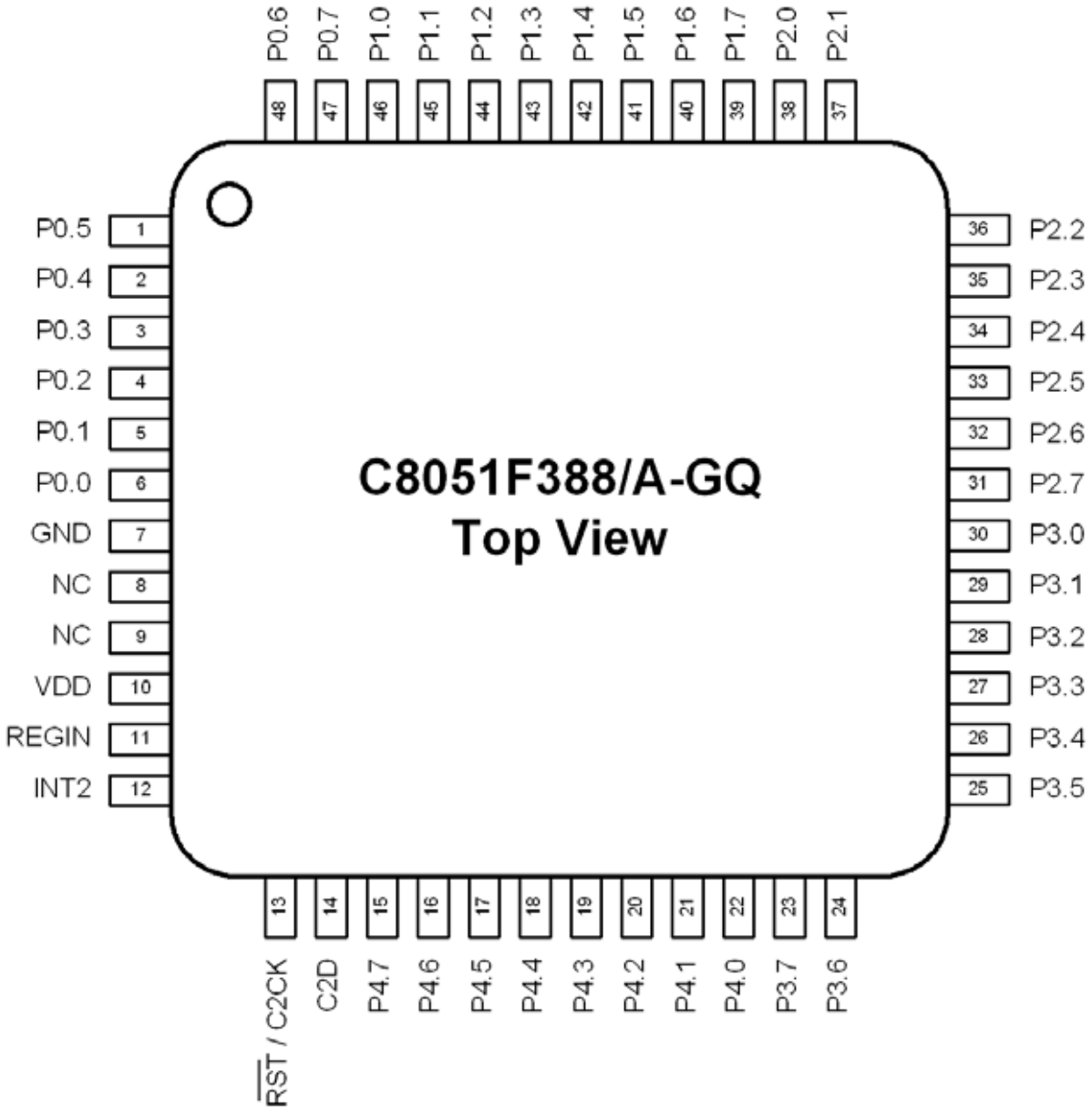

Figure 3.1. TQFP-48 (C8051F388/A) Pinout Diagram (Top View)

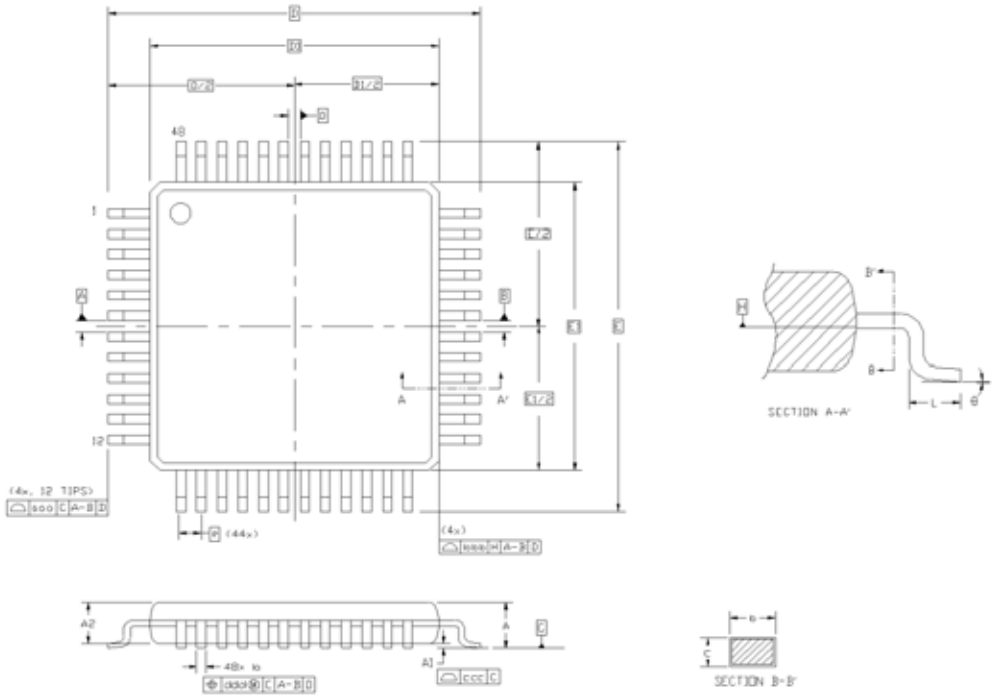

Figure 3.2. TQFP-48 Package Diagram

Table 3.2. TQFP-48 Package Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	—	—	1.20	E		9.00 BSC	
A1	0.05	—	0.15	E1		7.00 BSC	
A2	0.95	1.00	1.05	L	0.45	0.60	0.75
b	0.17	0.22	0.27	aaa		0.20	
c	0.09	—	0.20	bbb		0.20	
D		9.00 BSC		ccc		0.08	
D1		7.00 BSC		ddd		0.08	
e		0.50 BSC		q	0°	3.5°	7°

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation ABC.
4. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.