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C8051F39x/37x

50 MIPS 16 kB Flash, 512B EEPROM Mixed-Signal MCU

Analog Peripherals ('F390/2/4/6/8 and 'F370/4)

- **10-Bit ADC**
  - Programmable throughput up to 500 ksps
  - Up to 16 external inputs, programmable as single-ended or differential
  - Reference from on-chip voltage reference, V_{DD} or external VREF pin
  - Internal or external start of conversion sources
- **Two 10-Bit Current Output DACs**
  - Supports output through resets for continuous operation
- **Comparator**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source
- **Precision Temperature Sensor**
  - Accurate to ±2 °C across temperature range with no user calibration

On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers

Low Power

- 160 µA/MHz Active mode with 49 MHz internal precision oscillator
- 200 nA Stop mode current

Temperature Range

- –40 to +85 °C ('F37x)
- –40 to +105 °C ('F39x)

Package

- 24-Pin QFN ('F390/1/4/5 and 'F37x)
- 20-Pin QFN ('F392/3/6/7/8/9)

High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz clock
- Expanded interrupt handler

Memory

- Up to 1 kB internal data RAM (256 + 768)
- Up to 16 kB Flash; In-system programmable in 512-byte Sectors
- 512 bytes of byte-programmable EEPROM; 1 million write/erase cycles ('F37x)

Digital Peripherals

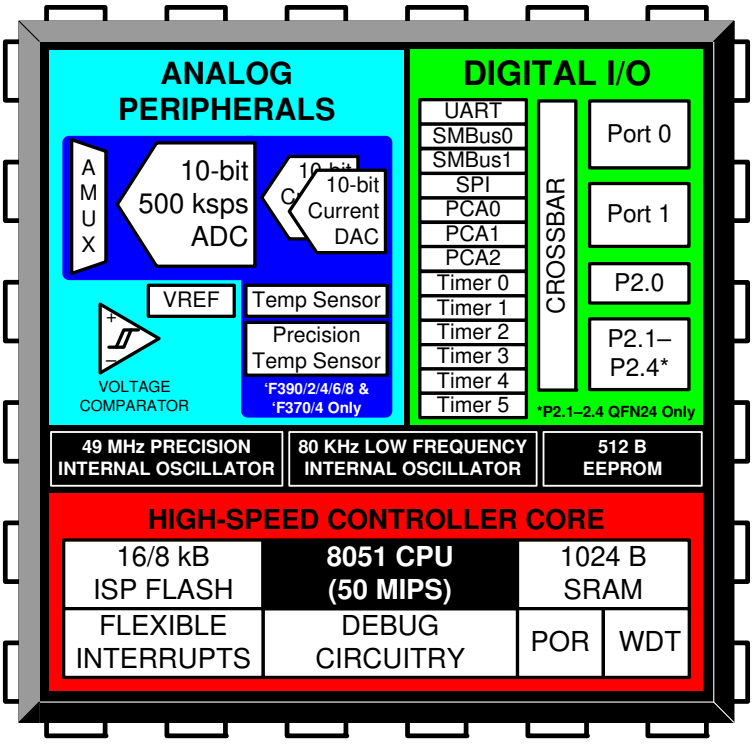
- 21 or 17 Port I/O
- UART, 2 SMBus (I^2C compatible), and SPI serial ports
- Six general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with three capture/compare modules and PWM functionality

Clock Sources

- 49 MHz ±2% precision internal oscillator
  - Supports crystal-less UART operation
  - Low-power suspend mode with fast wake time
- 80 kHz low-frequency, low-power oscillator
- External oscillator: Crystal, RC, C, or CMOS clock
- Can switch between clock sources on-the-fly; useful in power saving modes

Supply Voltage 1.8 to 3.6 V

- Built-in voltage supply monitor



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1. System Overview

C8051F39x/37x devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Section "2. Ordering Information" on page 20 for specific product feature selection and part ordering numbers.

- High-speed pipelined 8051-compatible microcontroller core (up to 50 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 10-bit 500 ksps 20 or 16-channel single-ended/differential ADC with analog multiplexer
- Two 10-bit Current Output DACs
- Precision temperature sensor with ±2 °C absolute accuracy
- Precision programmable 49 MHz internal oscillator
- Low-power, low-frequency oscillator
- 16 kB of on-chip Flash memory
- 1024 bytes of on-chip RAM
- Co-packaged with 512 bytes of EEPROM memory, accessible via I^2C (C8051F37x)
- Two SMBus/I^2C, UART, and SPI serial interfaces implemented in hardware
- Six general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with three capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, V_{DD} Monitor, and Temperature Sensor
- On-chip Voltage Comparator
- 21 or 17 Port I/O
- Low-power suspend mode with fast wake-up time

With on-chip Power-On Reset, V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051F39x/37x devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

The C8051F37x devices are specified for 1.8 to 3.6 V operation over the industrial temperature range (–40 to +85 °C), while the C8051F39x devices operate over an extended temperature range (-40 to +105 °C). The C8051F392/3/6/7/8/9 are available in a 20-pin QFN package and the C8051F390/1/4/5 and C8051F37x are available in a 24-pin QFN package. Both package options are lead-free and RoHS compliant. See Section "2. Ordering Information" on page 20 for ordering information. Block diagrams are included in Figure 1.1, Figure 1.2 and Figure 1.3.

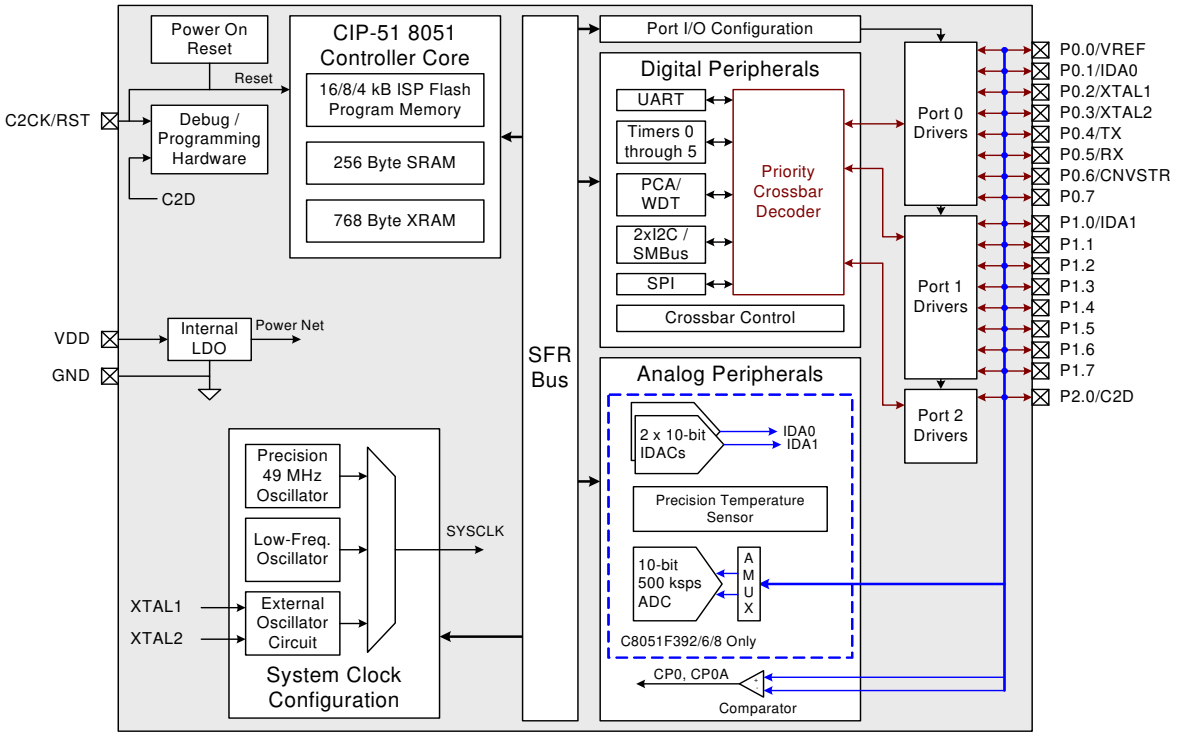

Figure 1.1. C8051F392/3/6/7/8/9 Block Diagram

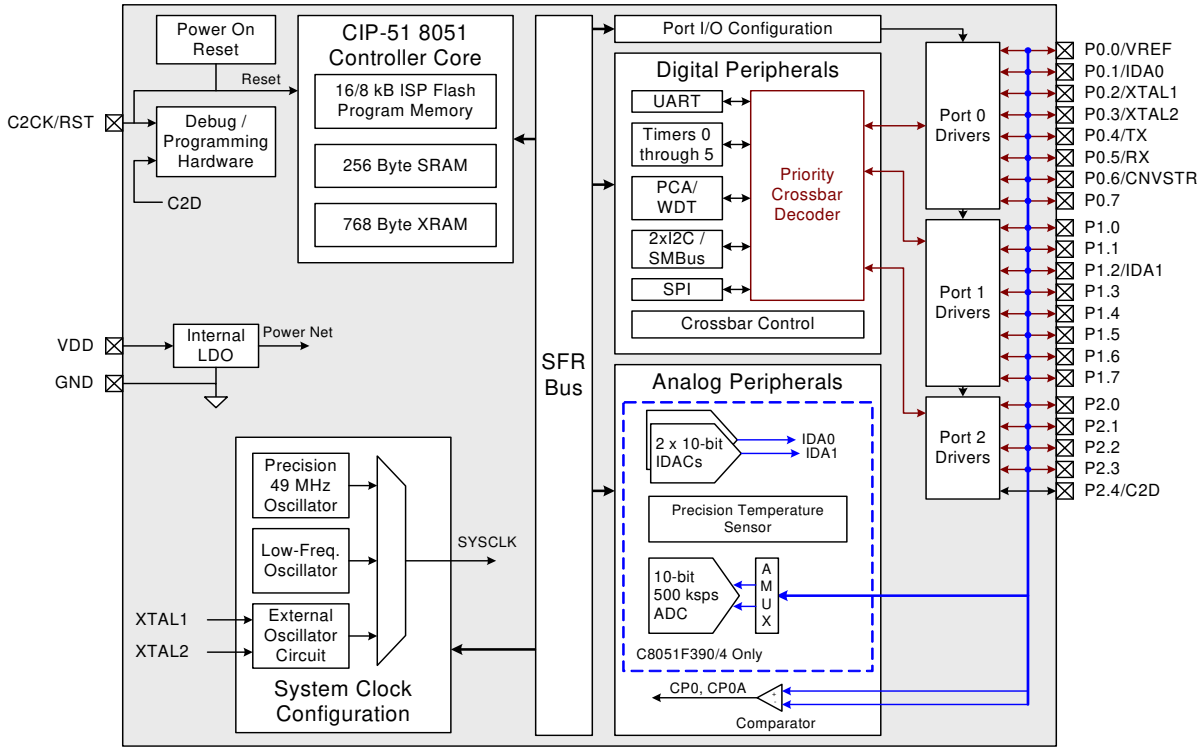

Figure 1.2. C8051F390/1/4/5 Block Diagram

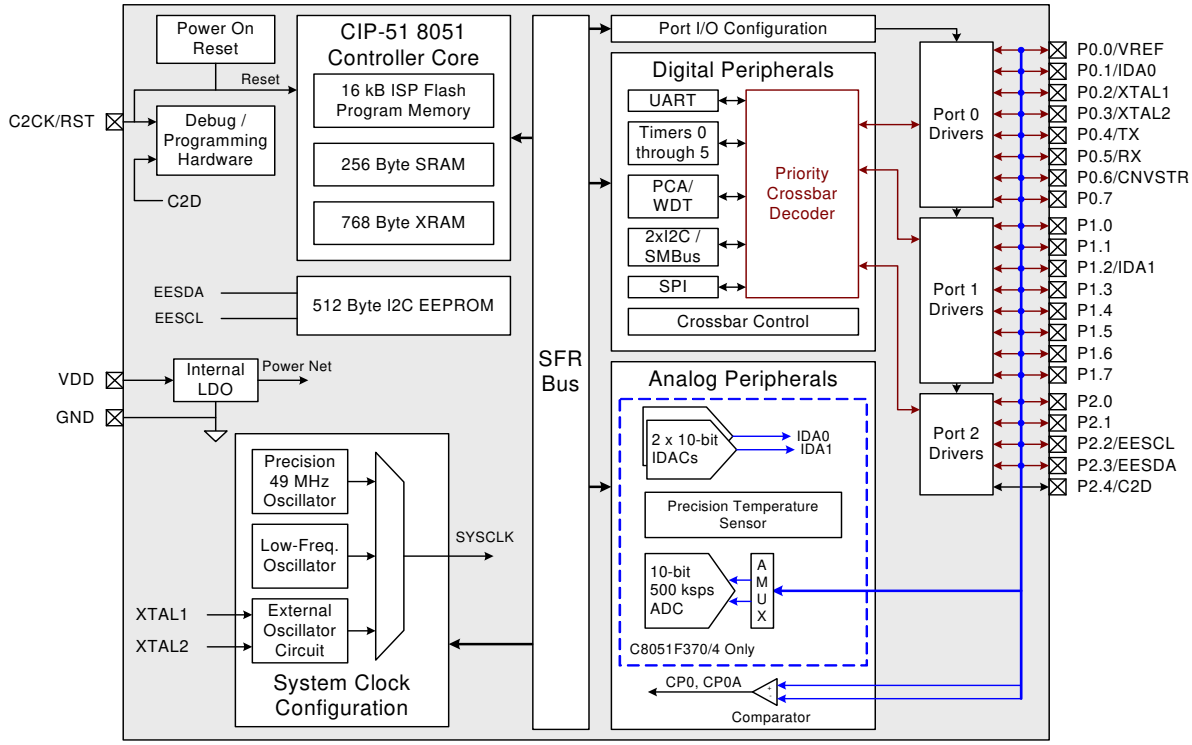

Figure 1.3. C8051F370/1/4/5 Block Diagram

2. Ordering Information

The following features are common to all device in this family:

- 50 MIPS throughput (peak)
- 1 kB of RAM (256 internal bytes and 768 XRAM bytes)
- Calibrated internal 49 MHz oscillator
- Internal 80 kHz oscillator
- Two SMBus/I^2C
- Enhanced SPI, Enhanced UART
- Six Timers
- Three Programmable Counter Array channels
- Analog Comparator
- Lead-free / RoHS Compliant

Table 2.1 shows the features that differentiate the devices in this family.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (Bytes)	EEPROM (Bytes)	Digital Port I/Os	10-bit ADC Channels	10-bit DAC Channels	On-Chip Voltage Reference	Precision Temperature Sensor	Package 4x4 mm
C8051F370-A-GM	16k	512	21	20	2	Y	Y	QFN-24
C8051F371-A-GM	16k	512	21	—	—	—	—	QFN-24
C8051F374-A-GM	8k	512	21	20	2	Y	Y	QFN-24
C8051F375-A-GM	8k	512	21	—	—	—	—	QFN-24
C8051F390-A-GM	16k	—	21	20	2	Y	Y	QFN-24
C8051F391-A-GM	16k	—	21	—	—	—	—	QFN-24
C8051F392-A-GM	16k	—	17	16	2	Y	Y	QFN-20
C8051F393-A-GM	16k	—	17	—	—	—	—	QFN-20
C8051F394-A-GM	8k	—	21	20	2	Y	Y	QFN-24
C8051F395-A-GM	8k	—	21	—	—	—	—	QFN-24
C8051F396-A-GM	8k	—	17	16	2	Y	Y	QFN-20
C8051F397-A-GM	8k	—	17	—	—	—	—	QFN-20
C8051F398-A-GM	4k	—	17	16	2	Y	Y	QFN-20
C8051F399-A-GM	4k	—	17	—	—	—	—	QFN-20

3. C8051F33x Compatibility

The C8051F39x/37x family is designed to be a pin and code compatible replacement for the C8051F33x device family, with an enhanced feature set. The C8051F39x/37x device should function as a drop-in replacement for the C8051F33x devices in most applications. Table 3.1 lists recommended replacement part numbers for C8051F33x devices. See “3.1. Hardware Incompatibilities” to determine if any changes are necessary when upgrading an existing C8051F33x design to the C8051F39x/37x.

Table 3.1. C8051F33x Replacement Part Numbers

C8051F33x Part Number	C8051F39x/37x Part Number
C8051F330-GM	C8051F396-A-GM
C8051F331-GM	C8051F397-A-GM
C8051F332-GM	C8051F398-A-GM
C8051F333-GM	C8051F399-A-GM
C8051F334-GM	C8051F398-A-GM
C8051F335-GM	C8051F399-A-GM
C8051F336-GM	C8051F392-A-GM
C8051F337-GM	C8051F393-A-GM
C8051F338-GM	C8051F390-A-GM
C8051F339-GM	C8051F391-A-GM

3.1. Hardware Incompatibilities

While the C8051F39x/37x family includes a number of new features not found on the C8051F33x family, there are some differences that should be considered for any design port.

- **Internal High-Frequency Oscillator**: The undivided high-frequency oscillator on the C8051F39x/37x is 49 MHz, whereas the undivided high-frequency oscillator on the C8051F33x is 24.5 MHz. Correspondingly, the internal high frequency divide ratios (IFCN) have doubled. Thus, firmware written for the C8051F33x where the CLKSL[1:0] = 00b will result in the same SYSCLK frequency on the C8051F39x/37x.
- **Fabrication Technology**: The C8051F39x/37x is manufactured using a different technology process than the C8051F33x. As a result, many of the electrical performance parameters will have subtle differences. These differences should not affect most systems but it is nonetheless important to review the electrical parameters for any blocks that are used in the design, and ensure they are compatible with the existing hardware.
- **5 V Tolerance**: The port I/O pins on the C8501F39x/37x are not 5 V tolerant, whereas the port I/O pins on the C8051F33x are 5 V tolerant.
- **Lock Byte Address**: The lock byte for C8051F39x/7x devices with 16 kB of Flash resides at address 0x3FFF, whereas the lock byte for C8051F33x devices with 16 kB of Flash resides at address 0x3DFF. The lock byte for C8051F39x/7x devices with 8 kB of Flash resides at address 0x1FFF, whereas the lock byte for C8051F33x devices with 8 kB of Flash resides at address 0x1DFF.

4. Pin Definitions

Table 4.1. Pin Definitions for the C8051F39x/37x

Name	Pin 'F392/3/6/7/8/9	Pin 'F390/1/4/5	Pin 'F370/1/4/5	Type	Description
V_{DD}	3	4	4		Power Supply Voltage.
GND	2	3	3		Ground. This ground connection is required. The center pad may optionally be connected to ground also.
$\overline{RST}$/ C2CK	4	5	5	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 10 µs. Clock signal for the C2 Debug Interface.
C2D	5	6	6	D I/O	Bi-directional data signal for the C2 Debug Interface. Shared with P2.0 on 20-pin packaging and P2.4 on 24-pin packaging.
P0.0/ VREF	1	2	2	D I/O or A In A In	Port 0.0. External VREF input.
P0.1 IDA0	20	1	1	D I/O or A In A Out	Port 0.1. IDA0 Output.
P0.2/ XTAL1	19	24	24	D I/O or A In A In	Port 0.2. External Clock Input. This pin is the external oscillator return for a crystal or resonator.
P0.3/ XTAL2	18	23	23	D I/O or A In A I/O or D In	Port 0.3. External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations.
P0.4	17	22	22	D I/O or A In	Port 0.4.
P0.5	16	21	21	D I/O or A In	Port 0.5.

Table 4.1. Pin Definitions for the C8051F39x/37x (Continued)

Name	Pin ‘F392/3/6/7/8/9	Pin ’F390/1/4/5	Pin ’F370/1/4/5	Type	Description
P0.6/ CNVSTR	15	20	20	D I/O or A In D In	Port 0.6. ADC0 External Convert Start or IDA0 Update Source Input.
P0.7	14	19	19	D I/O or A In	Port 0.7.
P1.0 IDA1	13	—	—	D I/O or A In A Out	Port 1.0. IDA1 Output.
P1.0		18	18	D I/O or A In	Port 1.0.
P1.1	12	17	17	D I/O or A In	Port 1.1.
P1.2 IDA1	-	16	16	D I/O or A In A Out	Port 1.2. IDA1 Output.
P1.2	11	—	—	D I/O or A In	Port 1.2.
P1.3	10	15	15	D I/O or A In	Port 1.3.
P1.4	9	14	14	D I/O or A In	Port 1.4.
P1.5	8	13	13	D I/O or A In	Port 1.5.
P1.6	7	12	12	D I/O or A In	Port 1.6.
P1.7	6	11	11	D I/O or A In	Port 1.7.
P2.0	5	10	10	D I/O or A In	Port 2.0. (Also C2D on 20-pin Packaging)
P2.1	—	9	9	D I/O or A In	Port 2.1.

Table 4.1. Pin Definitions for the C8051F39x/37x (Continued)

Name	Pin ‘F392/3/6/7/8/9	Pin ’F390/1/4/5	Pin ’F370/1/4/5	Type	Description
P2.2	—	8	—	D I/O or A In	Port 2.2.
P2.2 EESCL	-	—	8	D I/O or A In D I/O	Port 2.2. EEPROM SCL Connection.
P2.3	—	7	—	D I/O or A In	Port 2.3.
P2.3 EESDA	-	—	7	D I/O or A In D I/O	Port 2.3. EEPROM SDA Connection.
P2.4	—	6	6	D I/O	Port 2.4. (Also C2D on 24-pin Packaging)

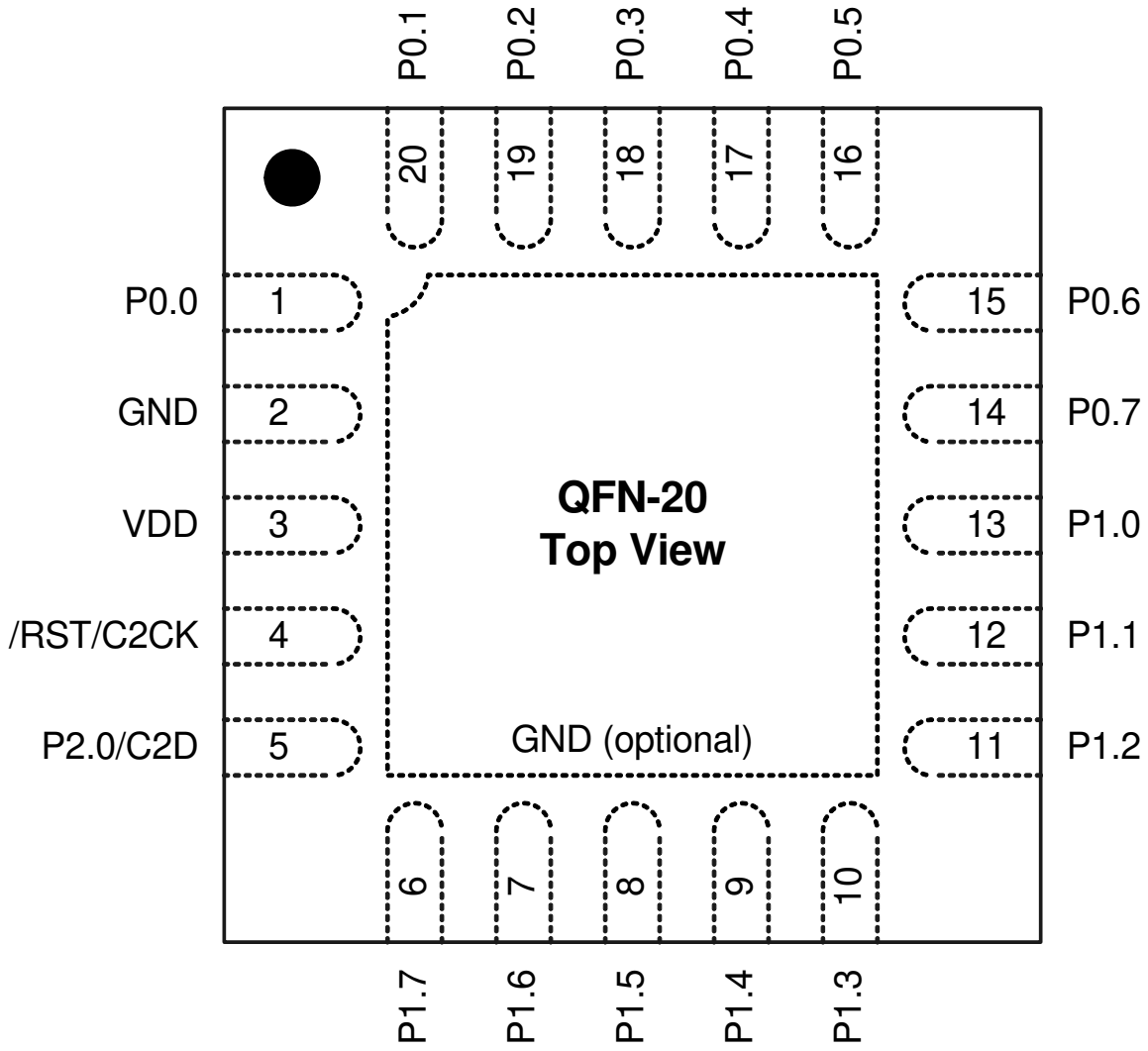

Figure 4.1. C8051F392/3/6/7/8/9 QFN-20 Pinout Diagram (Top View)