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### Analog Peripherals

- **12-Bit ADC**
  - ±1 LSB INL; no missing codes
  - Programmable throughput up to 200 ksps
  - Up to 24 external inputs
  - Data dependent windowed interrupt generator
  - Built-in temperature sensor (±3 °C)
- **Two 12-Bit Current Mode DACs**
- **Two Comparators**
  - Programmable hysteresis and response time
  - Configurable as wake-up or reset source
- **POR/Brownout Detector**
- **Voltage Reference—1.5, 2.2 V (programmable)**

### On-Chip Debug

- On-chip debug circuitry facilitates full-speed, non-intrusive in-system debug (No emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Complete development kit

### Supply Voltage 2.0 to 5.25 V

- Built-in LDO regulator: 2.1 or 2.5 V

### High Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to **50 MIPS** throughput with 50 MHz system clock
- Expanded interrupt handler

### Memory

- 2304 bytes internal data RAM (256 + 2048)
- 32/16 kB Flash; In-system programmable in 512 byte sectors
- 64 bytes battery-backed RAM (smaRTClock)

### Digital Peripherals

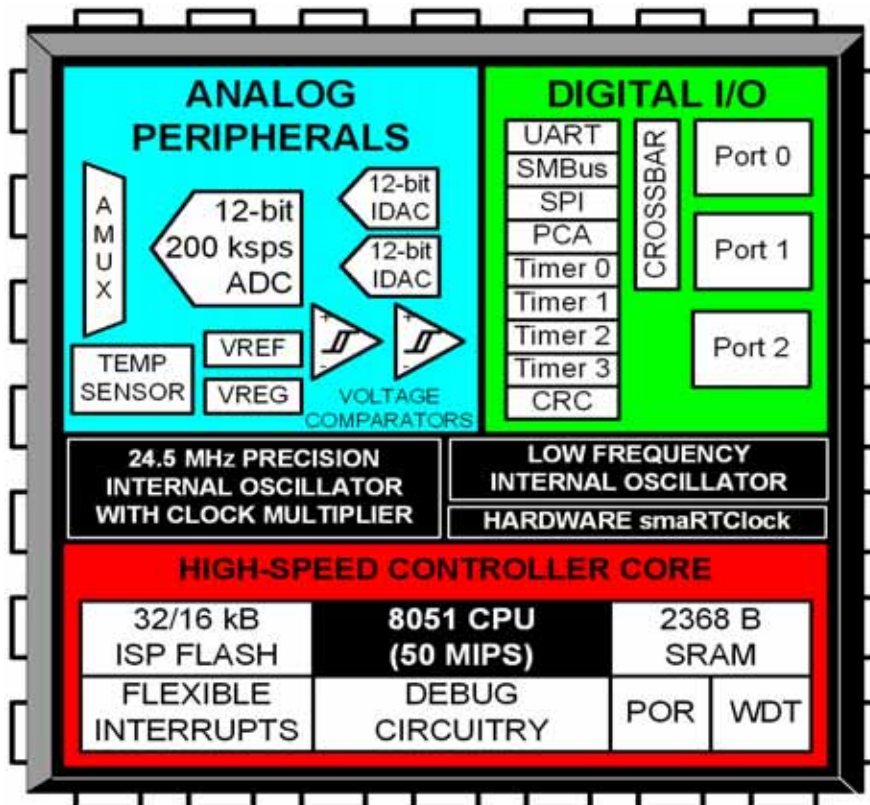
- 24 port I/O; push-pull or open-drain, up to 5.25 V tolerance
- Hardware SMBus™ (I2C™ Compatible), SPI™, and UART serial ports available concurrently
- Four general purpose 16-bit counter/timers
- Programmable 16-bit counter/timer array with six capture/compare modules, WDT
- Hardware smaRTClock operates down to 1 V with 64 bytes battery-backed RAM and backup voltage regulator

### Clock Sources

- Internal oscillators: 24.5 MHz 2% accuracy supports UART operation; clock multiplier up to 50 MHz
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- smaRTClock oscillator: 32 kHz Crystal or self-resonant oscillator
- Can switch between clock sources on-the-fly

### 32-Pin LQFP or 28-Pin 5 x 5 QFN

Temperature Range: -40 to +85 °C



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**NOTES:**

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## 1. System Overview

C8051F41x devices are fully integrated, low power, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

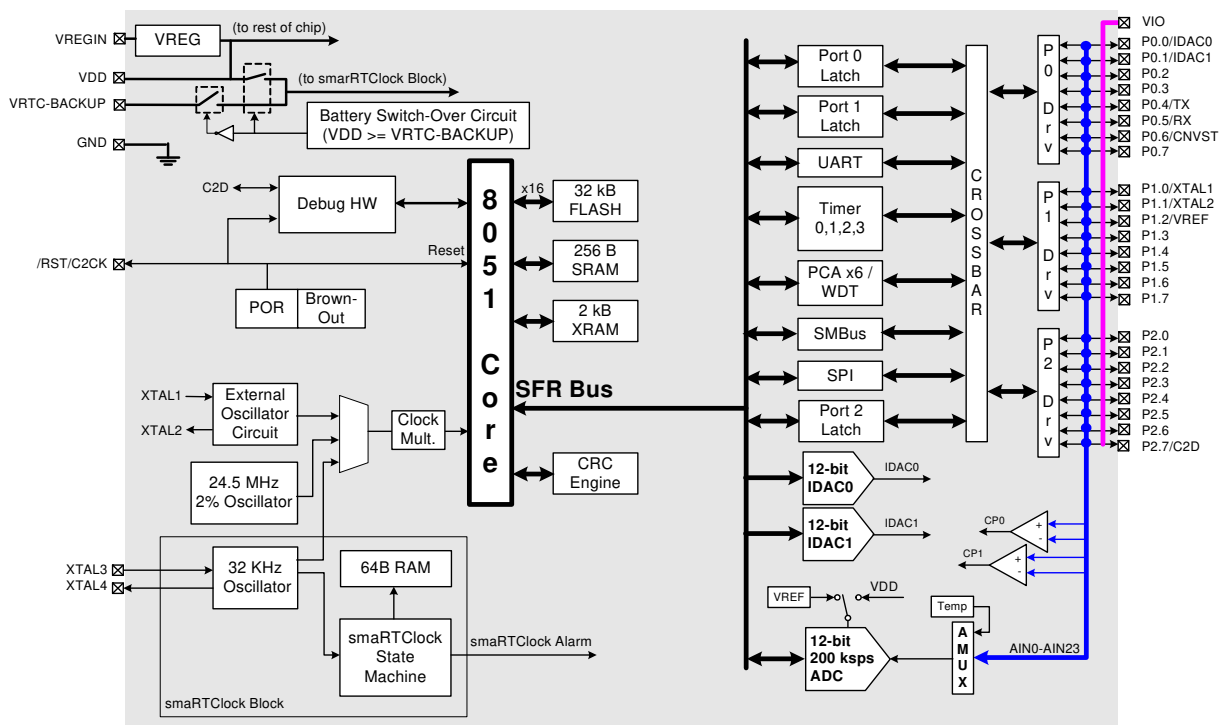
- High-speed pipelined 8051-compatible microcontroller core (up to 50 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 12-bit 200 ksps ADC with analog multiplexer and 24 analog inputs
- Two 12-bit Current Output DACs
- Precision programmable 24.5 MHz internal oscillator
- Up to 32 kB bytes of on-chip Flash memory
- 2304 bytes of on-chip RAM
- SMBus/I2C, Enhanced UART, and SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with six capture/compare modules and Watchdog Timer function
- Hardware smartClock (Real Time Clock) operates down to 1 V with 64 bytes of Backup RAM and a Backup Voltage Regulator
- Hardware CRC Engine
- On-chip Power-On Reset,  $V_{DD}$  Monitor, and Temperature Sensor
- On-chip Voltage Comparators
- Up to 24 Port I/O

With on-chip Power-On Reset,  $V_{DD}$  monitor, Watchdog Timer, and clock oscillator, the C8051F41x devices are truly standalone system-on-a-chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Laboratories 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system programming and debugging without occupying package pins.

Each device is specified for 2.0-to-2.75 V operation (supply voltage can be up to 5.25 V using on-chip regulator) over the industrial temperature range ( $-45$  to  $+85$  °C). The C8051F41x are available in 28-pin QFN (also referred to as MLP or MLF) or 32-pin LQFP packages.





**Figure 1.1. C8051F410 Block Diagram**

# C8051F410/1/2/3

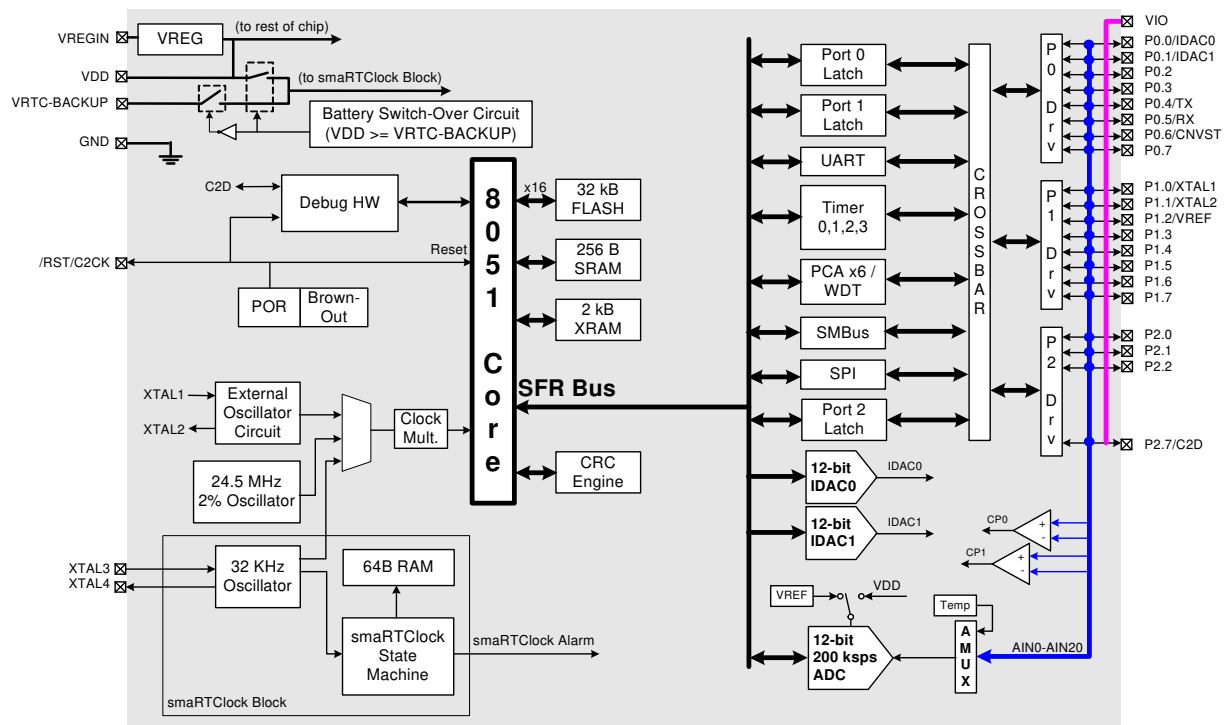


Figure 1.2. C8051F411 Block Diagram

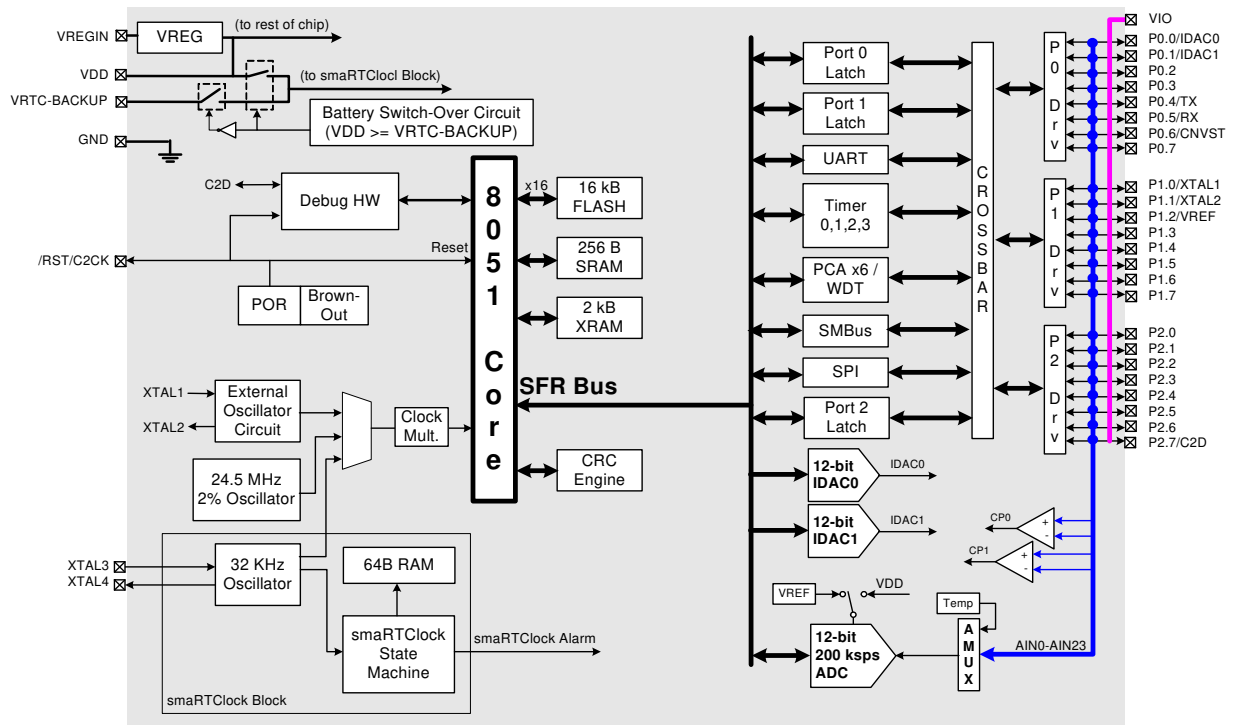


Figure 1.3. C8051F412 Block Diagram



# C8051F410/1/2/3

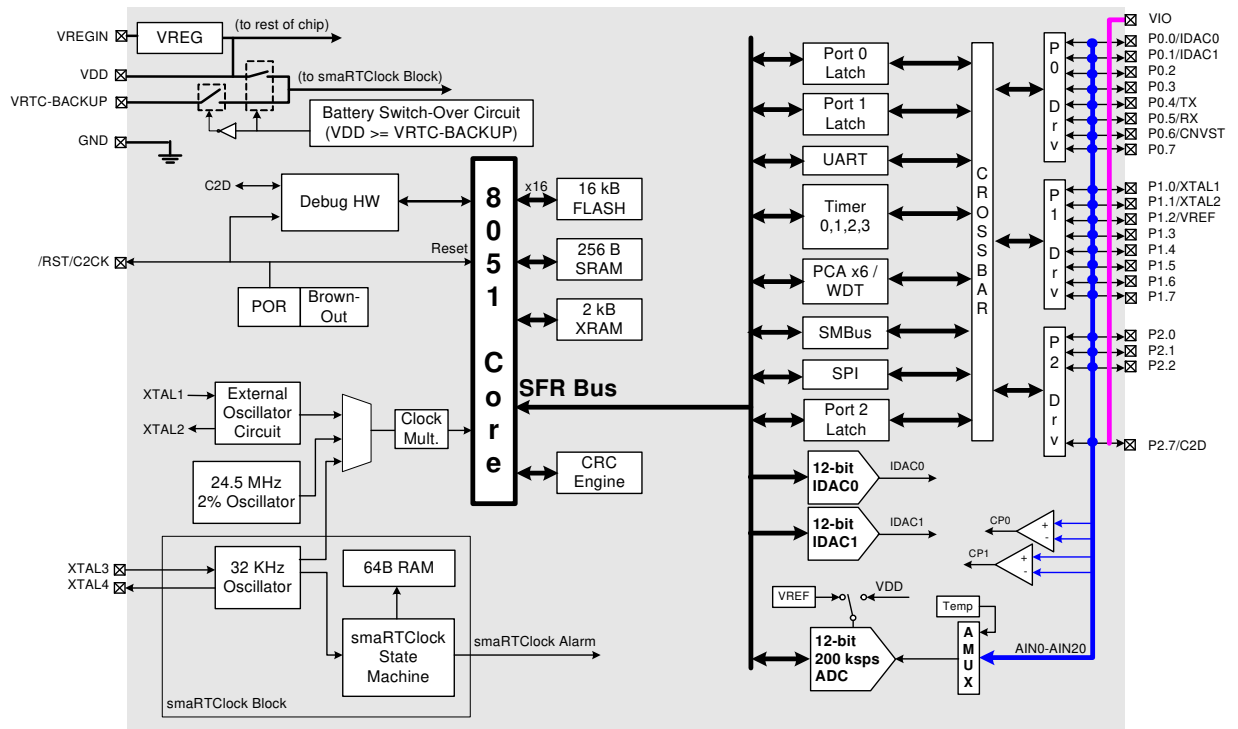


Figure 1.4. C8051F413 Block Diagram

## 1.1. CIP-51™ Microcontroller

### 1.1.1. Fully 8051 Compatible Instruction Set

The C8051F41x devices use Silicon Laboratories' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set. Standard 803x/805x assemblers and compilers can be used to develop software. The C8051F41x family has a superset of all the peripherals included with a standard 8052.

### 1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute, and usually have a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with no instructions taking more than eight system clock cycles.

With the CIP-51's system clock running at 50 MHz, it has a peak throughput of 50 MIPS. The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/4	3	3/5	4	5	4/6	6	8
Number of Instructions	26	50	5	10	7	5	2	1	2	1

### 1.1.3. Additional Features

The C8051F41x SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

An extended interrupt handler allows the numerous analog and digital peripherals to operate independently of the controller core and interrupt the controller only when necessary. By requiring less intervention from the microcontroller core, an interrupt-driven system is more efficient and allows for easier implementation of multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip  $V_{DD}$  monitor, a Watchdog Timer, a Missing Clock Detector, a voltage level detection from Comparator0, a smaRTClock alarm or missing smaRTClock clock detector reset, a forced software reset, an external reset pin, and an illegal Flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The internal oscillator is factory calibrated to 24.5 MHz  $\pm 2\%$ . An external oscillator drive circuit is also included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. A clock multiplier allows for operation at up to 50 MHz. The dedicated smaRTClock oscillator can be extremely useful in low power applications, allowing the system to maintain accurate time while the MCU is not powered, or its internal oscillator is suspended. The MCU can be reset or have its oscillator awakened using the smaRTClock alarm function.