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C8051F52x/F53x

8/4/2 kB ISP Flash MCU Family

Analog Peripherals
- **12-Bit ADC**
  - Programmable throughput up to 200 ksps
  - Up to 6/16 external inputs
  - Data dependent windowed interrupt generator
  - Built-in temperature sensor
- **Comparator**
  - Programmable hysteresis and response time
  - Configurable as wake-up or reset source
  - Low current
- **POR/Brownout Detector**
- **Voltage Reference—1.5 and 2.2 V (programmable)**

On-Chip Debug
- On-chip debug circuitry facilitates full-speed, non-intrusive in-system debug (No emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Complete development kit

Supply Voltage 2.0 to 5.25 V
- Built-in LDO regulator

High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to **25 MIPS** throughput with 25 MHz system clock
- Expanded interrupt handler

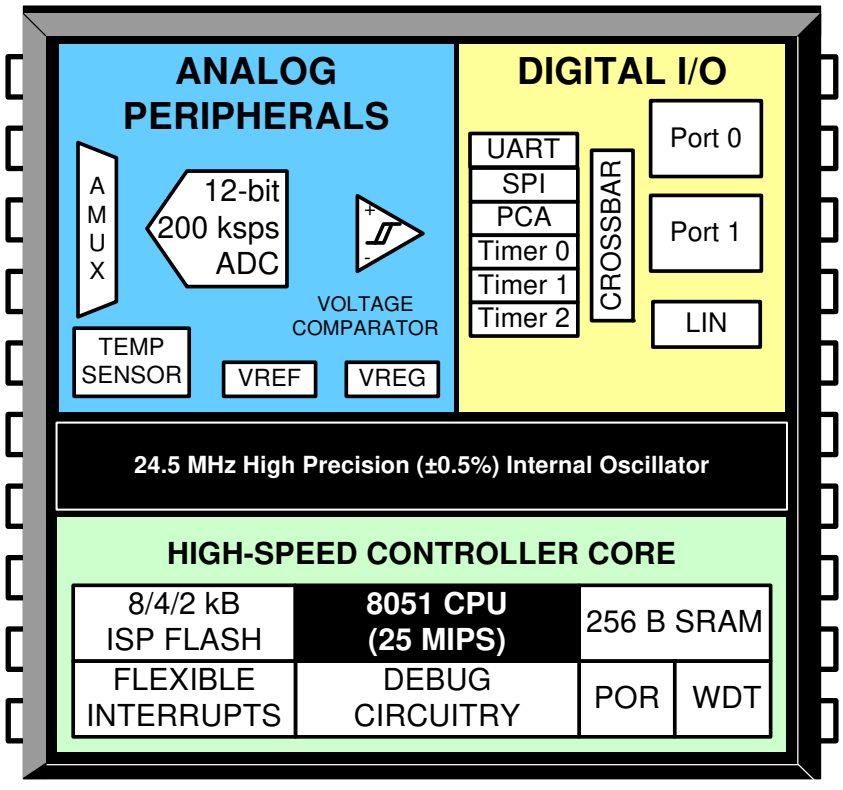
Memory
- 8/4/2 kB Flash; In-system byte programmable in 512 byte sectors
- 256 bytes internal data RAM

Digital Peripherals
- 16/6 port I/O; push-pull or open-drain, 5 V tolerant
- Hardware SPI™, and UART serial port
- LIN 2.1 Controller (Master and Slave capable); no crystal required
- Three general purpose 16-bit counter/timers
- Programmable 16-bit counter/timer array with three capture/compare modules, WDT

Clock Sources
- Internal oscillators: 24.5 MHz **±0.5%** accuracy supports UART and LIN-Master operation
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly

Packages
- 10-Pin DFN (3 x 3 mm)
- 20-pin QFN (4 x 4 mm)
- 20-pin TSSOP

Automotive Qualified
- Temperature Range: –40 to +125 °C
- Compliant to AEC-Q100



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1. System Overview

The C8051F52x/F52xA/F53x/F53xA family of devices are fully integrated, low power, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 12-bit 200 ksps ADC with analog multiplexer and up to 16 analog inputs
- Precision programmable 24.5 MHz internal oscillator that is within ±0.5% across the temperature range and for VDD voltages greater than or equal to the on-chip voltage regulator minimum output at the low setting. The oscillator is within ±1.0% for VDD voltages below this minimum output setting.
- Up to 7680 bytes of on-chip Flash memory
- 256 bytes of on-chip RAM
- Enhanced UART, and SPI serial interfaces implemented in hardware
- LIN 2.1 peripheral (fully backwards compatible, master and slave modes)
- Three general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with three capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, V_{DD} Monitor, and Temperature Sensor
- On-chip Voltage Comparator
- Up to 16 Port I/O

With on-chip Power-On Reset, V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051F52x/F52xA/F53x/F53xA devices are truly standalone system-on-a-chip solutions. The Flash memory is byte writable and can be reprogrammed in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Laboratories 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system programming and debugging without occupying package pins.

Each device is specified for 2.0 to 5.25 V operation (supply voltage can be up to 5.25 V using on-chip regulator) over the automotive temperature range (–40 to +125 °C). The F52x/F52xA is available in the DFN10 (3 x 3 mm) package. The F53x/F53xA is available in the QFN20 (4 x 4 mm) or the TSSOP20 package.

1.1. Ordering Information

The following features are common to all devices in this family:

- 25 MHz system clock and 25 MIPS throughput (peak)
- 256 bytes of internal RAM
- Enhanced SPI peripheral
- Enhanced UART peripheral
- Three Timers
- Three Programmable Counter Array channels
- Internal 24.5 MHz oscillator
- Internal Voltage Regulator
- 12-bit, 200 ksps ADC
- Internal Voltage Reference and Temperature Sensor
- One Analog Comparator

Table 1.1 shows the features that differentiate the devices in this family.

Table 1.1. Product Selection Guide (Recommended for New Designs)

Ordering Part Number	Flash Memory (kB)	Port I/Os	LIN	Package	Ordering Part Number	Flash Memory (kB)	Port I/Os	LIN	Package
C8051F520-C-IM	8	6	✓	DFN-10	C8051F534-C-IM	4	16	—	QFN-20
C8051F521-C-IM	8	6	—	DFN-10	C8051F536-C-IM	2	16	✓	QFN-20
C8051F523-C-IM	4	6	✓	DFN-10	C8051F537-C-IM	2	16	—	QFN-20
C8051F524-C-IM	4	6	—	DFN-10	C8051F530-C-IT	8	16	✓	TSSOP-20
C8051F526-C-IM	2	6	✓	DFN-10	C8051F531-C-IT	8	16	—	TSSOP-20
C8051F527-C-IM	2	6	—	DFN-10	C8051F533-C-IT	4	16	✓	TSSOP-20
C8051F530-C-IM	8	16	✓	QFN-20	C8051F534-C-IT	4	16	—	TSSOP-20
C8051F531-C-IM	8	16	—	QFN-20	C8051F536-C-IT	2	16	✓	TSSOP-20
C8051F533-C-IM	4	16	✓	QFN-20	C8051F537-C-IT	2	16	—	TSSOP-20

All devices in Table 1.1 are also available in an automotive version. For the automotive version, the -I in the ordering part number is replaced with -A. For example, the automotive version of the C8051F520-C-IM is the C8051F520-C-AM.

The -AM and -AT devices receive full automotive quality production status, including AEC-Q100 qualification (fault coverage report available upon request), registration with International Material Data System (IMDS) and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at www.silabs.com with a registered NDA and approved user account. The -AM and -AT devices enable high volume automotive OEM applications with their enhanced testing and processing. Please contact Silicon Labs sales for more information regarding -AM and -AT devices for your automotive project.

Table 1.2. Product Selection Guide (Not Recommended for New Designs)

Ordering Part Number	Flash Memory (kB)	Port I/Os	LIN	Package	Ordering Part Number	Flash Memory (kB)	Port I/Os	LIN	Package
C8051F520-IM C8051F520A-IM	8	6	✓	DFN-10	C8051F534-IM C8051F534A-IM	4	16	—	QFN-20
C8051F521-IM C8051F521A-IM	8	6	—	DFN-10	C8051F536-IM C8051F536A-IM	2	16	✓	QFN-20
C8051F523-IM C8051F523A-IM	4	6	✓	DFN-10	C8051F537-IM C8051F537A-IM	2	16	—	QFN-20
C8051F524-IM C8051F524A-IM	4	6	—	DFN-10	C8051F530-IT C8051F530A-IT	8	16	✓	TSSOP-20
C8051F526-IM C8051F526A-IM	2	6	✓	DFN-10	C8051F531-IT C8051F531A-IT	8	16	—	TSSOP-20
C8051F527-IM C8051F527A-IM	2	6	—	DFN-10	C8051F533-IT C8051F533A-IT	4	16	✓	TSSOP-20
C8051F530-IM C8051F530A-IM	8	16	✓	QFN-20	C8051F534-IT C8051F534A-IT	4	16	—	TSSOP-20
C8051F531-IM C8051F531A-IM	8	16	—	QFN-20	C8051F536-IT C8051F536A-IT	2	16	✓	TSSOP-20
C8051F533-IM C8051F533A-IM	4	16	✓	QFN-20	C8051F537-IT C8051F537A-IT	2	16	—	TSSOP-20

The part numbers in Table 1.2 are not recommended for new designs. Instead, select the corresponding part number from Table 1.1 (silicon revision C) for your design. In Table 1.2, the part numbers in the format similar to C8051F520-IM are silicon revision A devices. The part numbers in the format similar to C8051F520A-IM are silicon revision B devices.

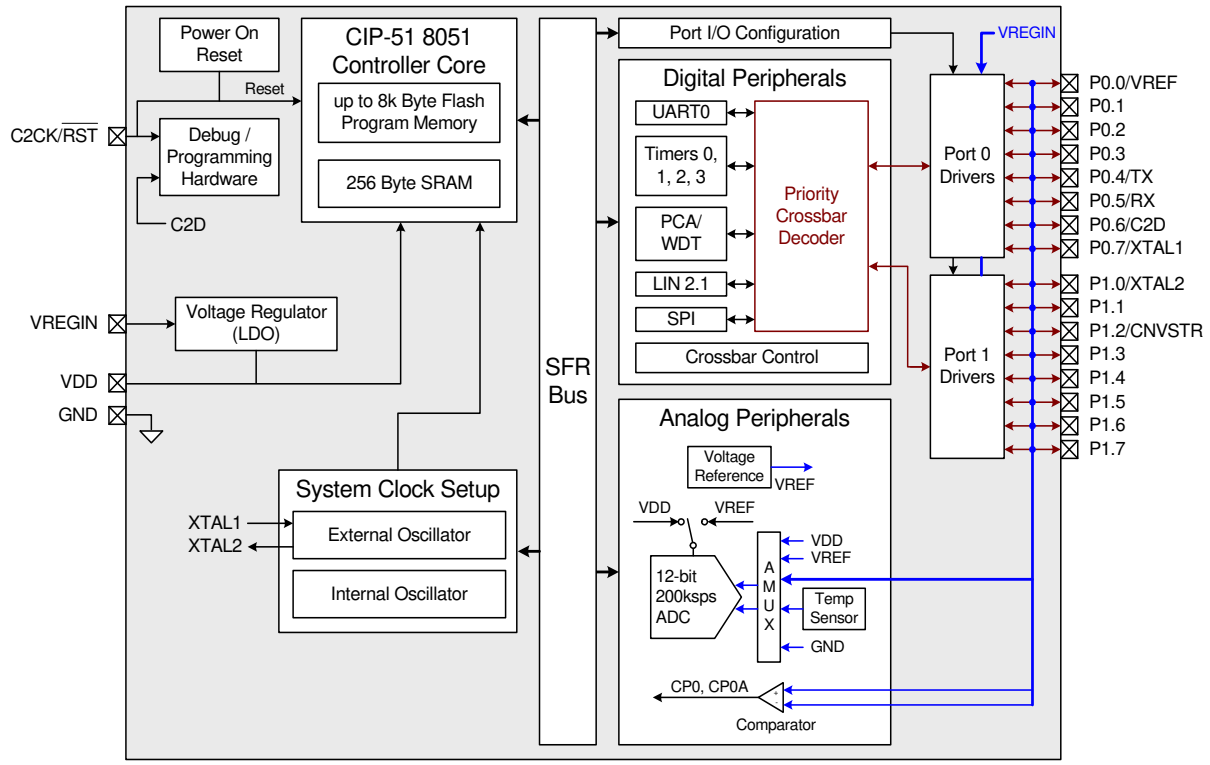

Figure 1.1. C8051F53xA/F53x-C Block Diagram

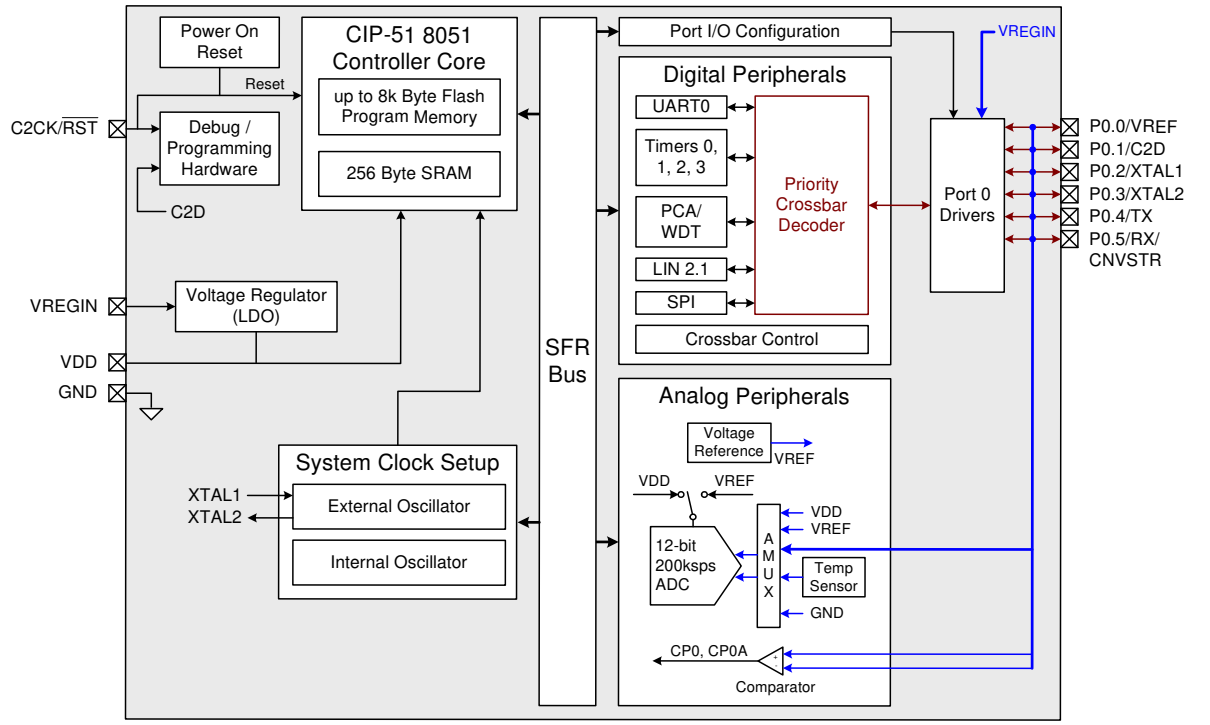

Figure 1.2. C8051F52xA/F52x-C Block Diagram

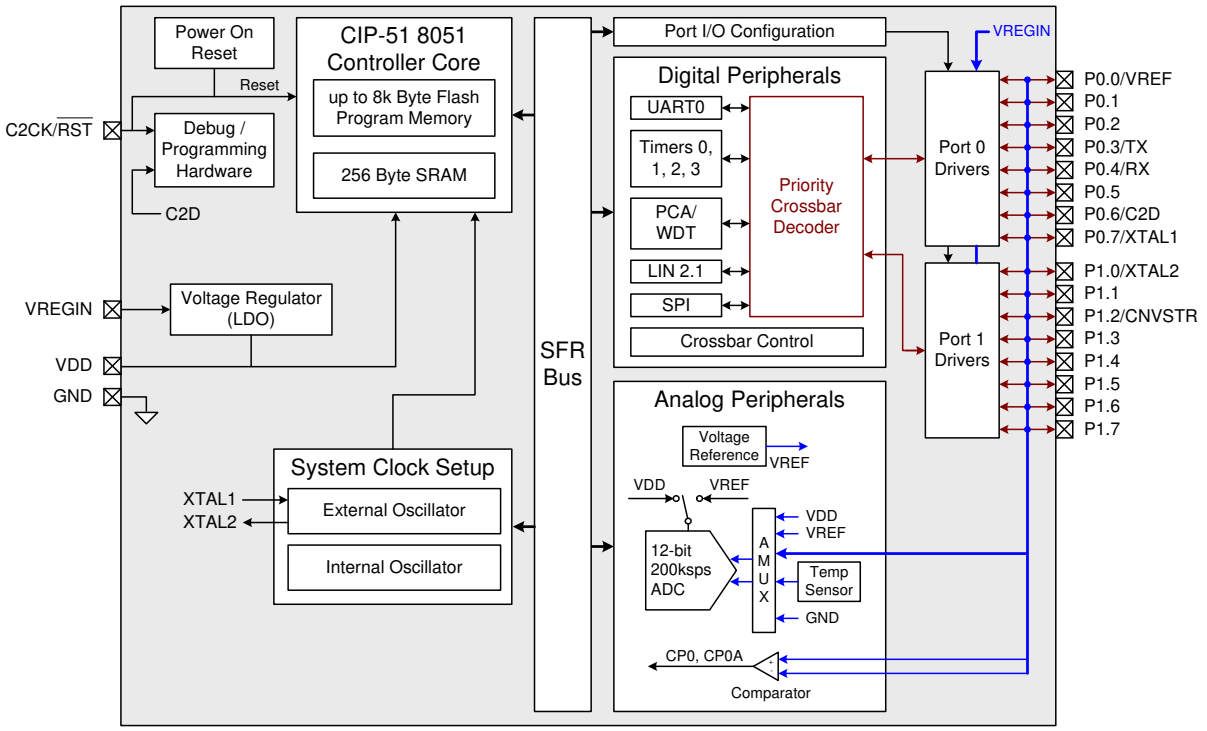

Figure 1.3. C8051F53x Block Diagram (Silicon Revision A)

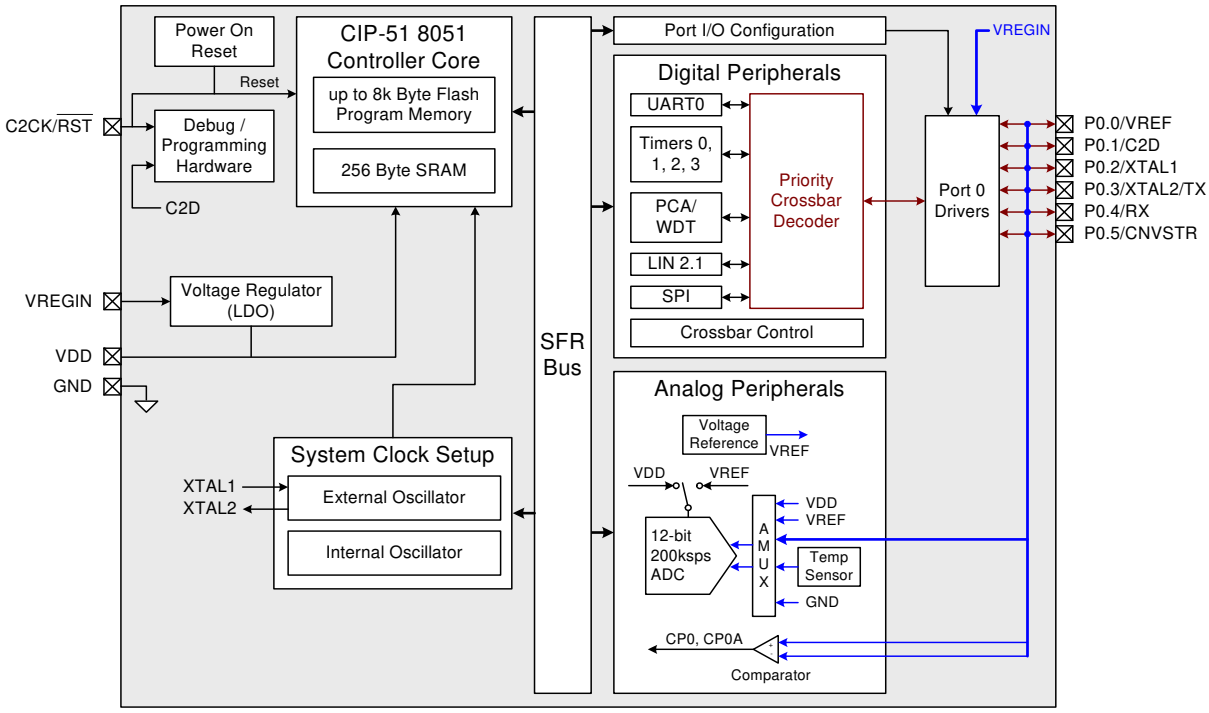

Figure 1.4. C8051F52x Block Diagram (Silicon Revision A)

1.2. CIP-51™ Microcontroller

1.2.1. Fully 8051 Compatible Instruction Set

The C8051F52x/F52xA/F53x/F53xA devices use Silicon Laboratories' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set. Standard 803x/805x assemblers and compilers can be used to develop software. The C8051F52x/F52xA/F53x/F53xA family has a superset of all the peripherals included with a standard 8052.

1.2.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute, and usually have a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with no instructions taking more than eight system clock cycles.

With the CIP-51's system clock running at 25 MHz, it has a peak throughput of 25 MIPS. The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

1.2.3. Additional Features

The C8051F52x/F52xA/F53x/F53xA family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

An extended interrupt handler allows the numerous analog and digital peripherals to operate independently of the controller core and interrupt the controller only when necessary. By requiring less intervention from the microcontroller core, an interrupt-driven system is more efficient and allows for easier implementation of multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} monitor, a Watchdog Timer, a Missing Clock Detector, a voltage level detection from Comparator, a forced software reset, an external reset pin, and an illegal Flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The internal oscillator is factory calibrated to 24.5 MHz ±0.5% across the entire operating temperature and voltage range. An external oscillator drive circuit is also included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock.

1.2.4. On-Chip Debug Circuitry

The C8051F52x/F52xA/F53x/F53xA devices include on-chip Silicon Laboratories 2-Wire (C2) debug circuitry that provides non-intrusive, full speed, in-circuit debugging of the production part *installed in the end application.*

Silicon Laboratories' debugging system supports inspection and modification of memory and registers, breakpoints, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the ADC) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F530DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F52x/F52xA/F53x/F53xA MCUs. The kit

includes software with a developer's studio and debugger, a USB debug adapter, a target application board with the associated MCU installed, and the required cables and wall-mount power supply. The development kit requires a computer with Windows installed. As shown in Figure 1.5, the PC is connected to the USB debug adapter. A six-inch ribbon cable connects the USB debug adapter to the user's application board, picking up the two C2 pins and GND.

The Silicon Laboratories IDE interface is a vastly superior developing and debugging configuration, compared to standard MCU emulators that use on-board "ICE Chips" and require the MCU in the application board to be socketed. Silicon Laboratories' debug paradigm increases ease of use and preserves the performance of the precision analog peripherals.

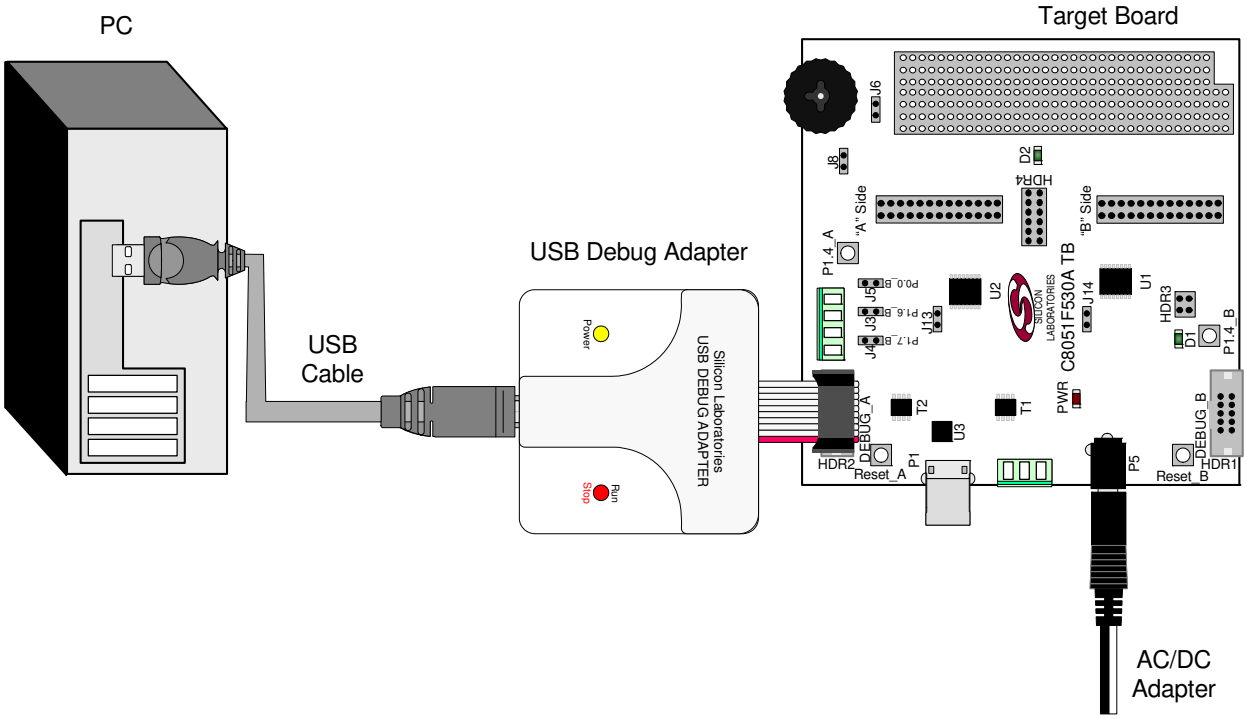

Figure 1.5. Development/In-System Debug Diagram

1.3. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

Program memory consists of 7680 bytes (’F520/0A/1/1A and ’F530/0A/1/1A), 4 kB (’F523/3A/4/4A and C8051F53x/53xA), or 2 kB (’F526/6A/7/7A and ’F536/6A/7/7A) of Flash. This memory is byte writable and erased in 512-byte sectors, and requires no special off-chip programming voltage.

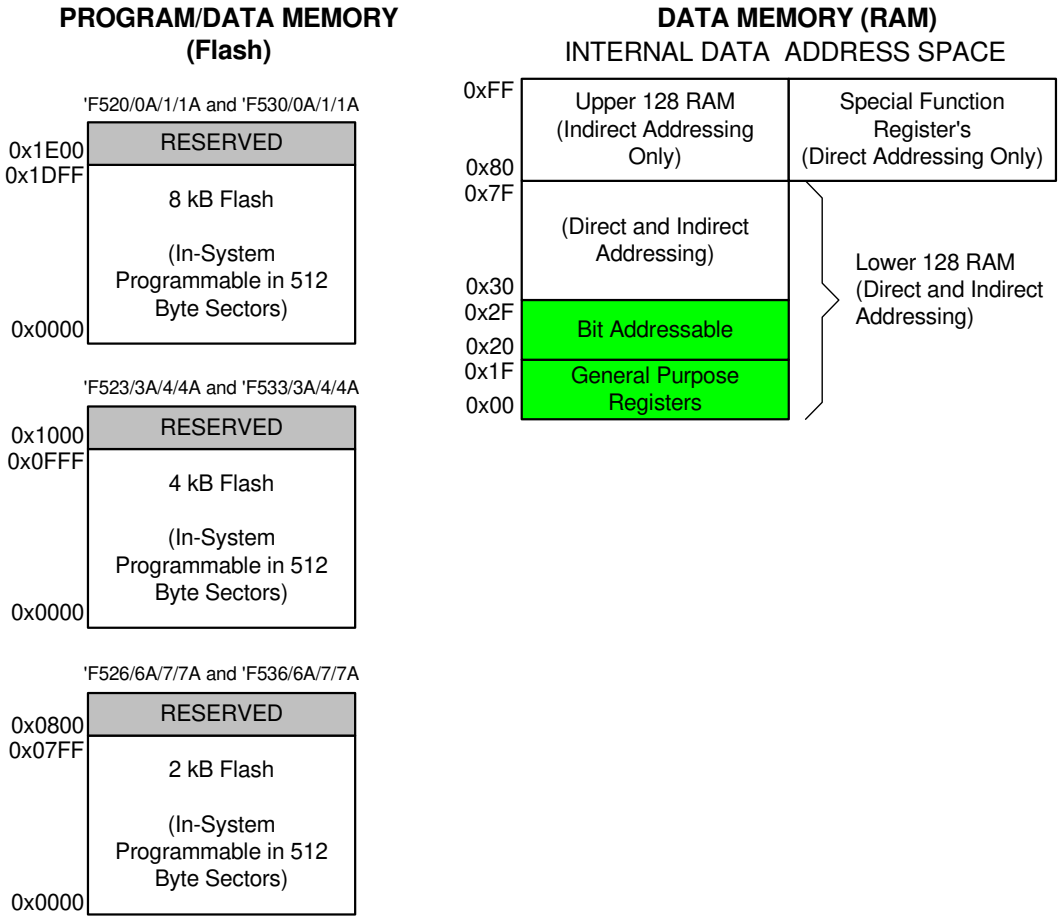

Figure 1.6. Memory Map

1.4. Operating Modes

The C8051F52x/F52xA/F53x/F53xA devices have four operating modes: Active (Normal), Idle, Suspend, and Stop. Active mode occurs during normal operation when the oscillator and peripherals are active. Idle mode halts the CPU while leaving the peripherals and internal clocks active. In Suspend and Stop mode, the CPU is halted, all interrupts and timers are inactive, and the internal oscillator is stopped. The various operating modes are described in Table 1.3 below:

Table 1.3. Operating Modes Summary

	Properties	Power Consumption	How Entered?	How Exited?
Active	■ SYSCLK active ■ CPU active (accessing Flash) ■ Peripherals active or inactive depending on user settings	Full	—	—
Idle	■ SYSCLK active ■ CPU inactive (not accessing Flash) ■ Peripherals active or inactive depending on user settings	Less than Full	IDLE (PCON.0)	Any enabled interrupt or device reset
Suspend	■ Internal oscillator inactive ■ If SYSCLK is derived from the internal oscillator, the peripherals and the CIP-51 will be stopped	Low	SUSPEND (OSCICN.5)	Port 0 event match Port 1 event match Comparator 0 enabled and output is logic 0
Stop	■ SYSCLK inactive ■ CPU inactive (not accessing Flash) ■ Digital peripherals inactive; analog peripherals active or inactive depending on user settings	Very low	STOP (PCON.1)	Device Reset

See Section “8.3. Power Management Modes” on page 89 for Idle and Stop mode details. See Section “14.1.1. Internal Oscillator Suspend Mode” on page 136 for more information on Suspend mode.

1.5. 12-Bit Analog to Digital Converter

The C8051F52x/F52xA/F53x/F53xA devices include an on-chip 12-bit SAR ADC with a maximum throughput of 200 ksps. The ADC system includes a configurable analog multiplexer that selects the positive ADC input, which is measured with respect to GND. Ports 0 and 1 are available as ADC inputs; additionally, the ADC includes an innovative programmable gain stage which allows the ADC to sample inputs sources greater than the VREF voltage. The on-chip Temperature Sensor output and the core supply voltage (V_{DD}) are also available as ADC inputs. User firmware may shut down the ADC or use it in Burst Mode to save power.

Conversions can be initiated in four ways: a software command, an overflow of Timer 1, an overflow of Timer 2, or an external convert start signal. This flexibility allows the start of conversion to be triggered by software events, a periodic signal (timer overflows), or external HW signals. Conversion completions are indicated by a status bit and an interrupt (if enabled) and occur after 1, 4, 8, or 16 samples have been accumulated by a hardware accumulator. The resulting 12-bit to 16-bit data word is latched into the ADC data SFRs upon completion of a conversion. When the system clock is slow, Burst Mode allows ADC0 to automatically wake from a low power shutdown state, acquire and accumulate samples, then re-enter the low power shutdown state without CPU intervention.

Window compare registers for the ADC data can be configured to interrupt the controller when ADC data is either within or outside of a specified range. The ADC can monitor a key voltage continuously in background mode, but not interrupt the controller unless the converted data is within/outside the specified range.

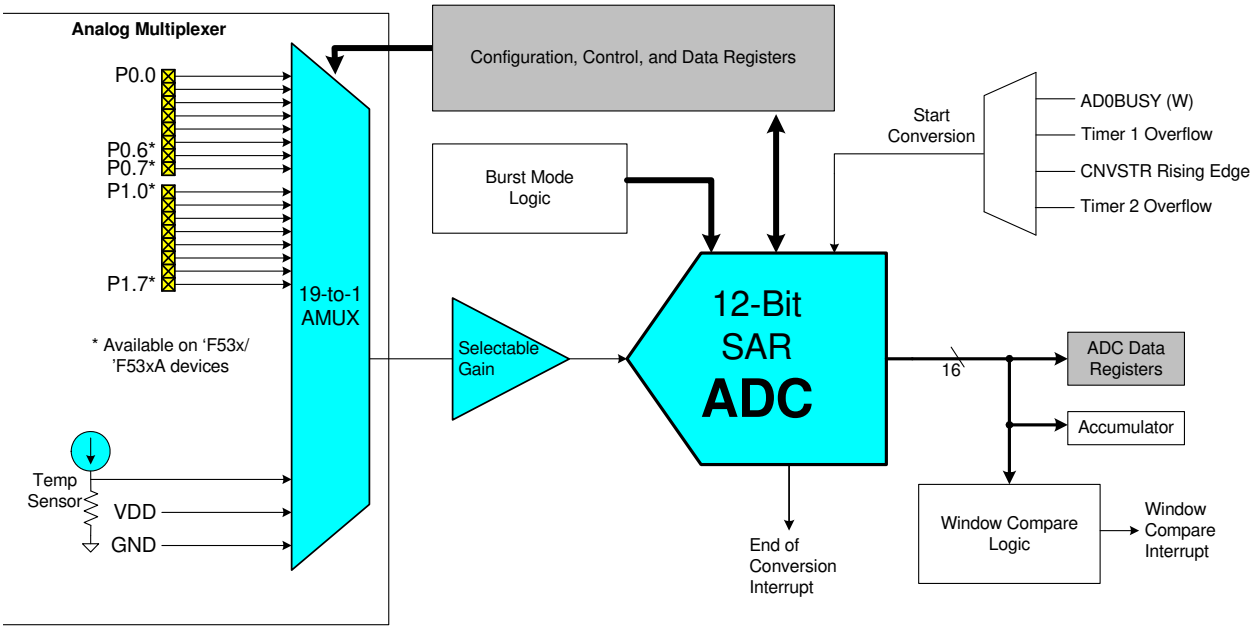

Figure 1.7. 12-Bit ADC Block Diagram

1.6. Programmable Comparator

C8051F52x/F52xA/F53x/F53xA devices include a software-configurable voltage comparator with an input multiplexer. The comparator offers programmable response time and hysteresis and an output that is optionally available at the Port pins: a synchronous “latched” output (CP0). The comparator interrupt may be generated on rising, falling, or both edges. When in IDLE or SUSPEND mode, these interrupts may be used as a “wake-up” source for the processor. The Comparator may also be configured as a reset source. A block diagram of the comparator is shown in Figure 1.8.

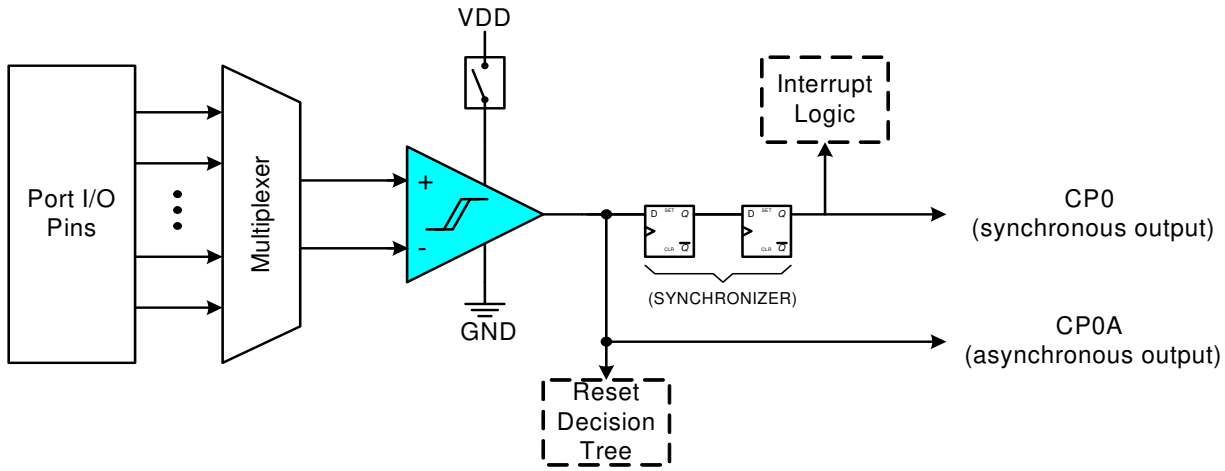

Figure 1.8. Comparator Block Diagram

1.7. Voltage Regulator

C8051F52x/F52xA/F53x/F53xA devices include an on-chip low dropout voltage regulator (REG0). The input to REG0 at the V_{REGIN} pin can be as high as 5.25 V. The output can be selected by software to 2.1 or 2.6 V. When enabled, the output of REG0 powers the device and drives the V_{DD} pin. The voltage regulator can be used to power external devices connected to V_{DD}.

1.8. Serial Port

The C8051F52x/F52xA/F53x/F53xA family includes a full-duplex UART with enhanced baud rate configuration, and an Enhanced SPI interface. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.

1.9. Port Input/Output

C8051F52x/F52xA/F53x/F53xA devices include up to 16 I/O pins. Port pins are organized as two byte-wide ports. The port pins behave like typical 8051 ports with a few enhancements. Each port pin can be configured as a digital or analog I/O pin. Pins selected as digital I/O can be configured for push-pull or open-drain operation. The “weak pullups” that are fixed on typical 8051 devices may be globally disabled to save power.

The Digital Crossbar allows mapping of internal digital system resources to port I/O pins. On-chip counter/timers, serial buses, hardware interrupts, and other digital signals can be configured to appear on the port pins using the Crossbar control registers. This allows the user to select the exact mix of general-purpose port I/O, digital, and analog resources needed for the application.

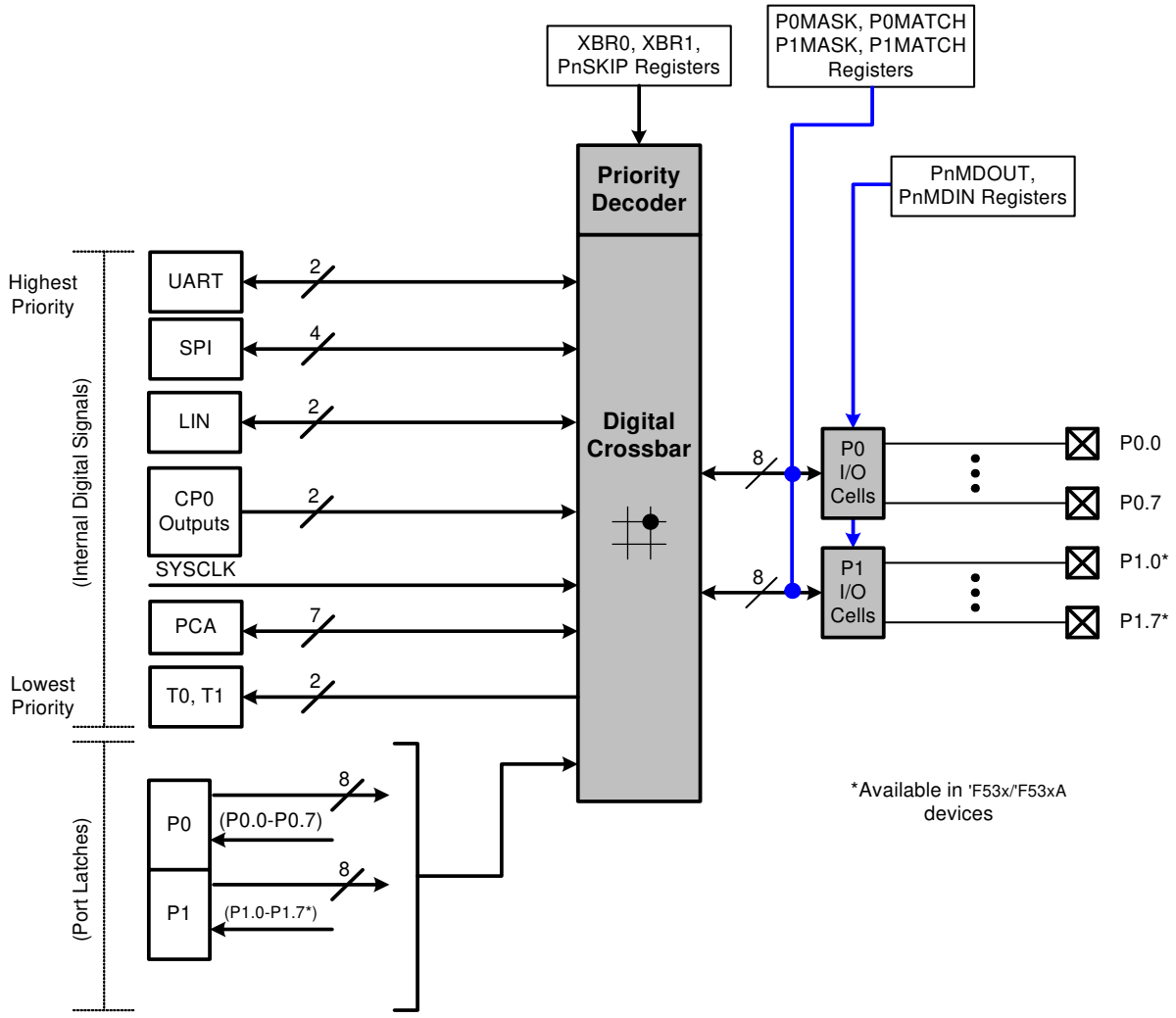

Figure 1.9. Port I/O Functional Block Diagram

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under Bias		–55	—	135	°C
Storage Temperature		–65	—	150	°C
Voltage on V_{REGIN} with Respect to GND		–0.3	—	5.5	V
Voltage on V_{DD} with Respect to GND		–0.3	—	2.8	V
Voltage on XTAL1 with Respect to GND		–0.3	—	V_{REGIN} + 0.3	V
Voltage on XTAL2 with Respect to GND		–0.3	—	V_{REGIN} + 0.3	V
Voltage on any Port I/O Pin or $\overline{RST}$ with Respect to GND		–0.3	—	V_{REGIN} + 0.3	V
Maximum Output Current Sunk by any Port Pin		—	—	100	mA
Maximum Output Current Sourced by any Port Pin		—	—	100	mA
Maximum Total Current through V_{REGIN}, and GND		—	—	500	mA

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.