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C8051F54x

Mixed Signal ISP Flash MCU Family

Analog Peripherals
- **12-Bit ADC**
  - Up to 200 ksps
  - Up to 25 external single-ended inputs
  - VREF from on-chip VREF, external pin or V_{DD}
  - Internal or external start of conversion source
  - Built-in temperature sensor
- **Two Comparators**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source
  - Low current

On-Chip Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Low cost, complete development kit

Supply Voltage 1.8 to 5.25 V
- Typical operating current: 19 mA at 50 MHz; Typical stop mode current: 1 µA

High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz clock
- Expanded interrupt handler

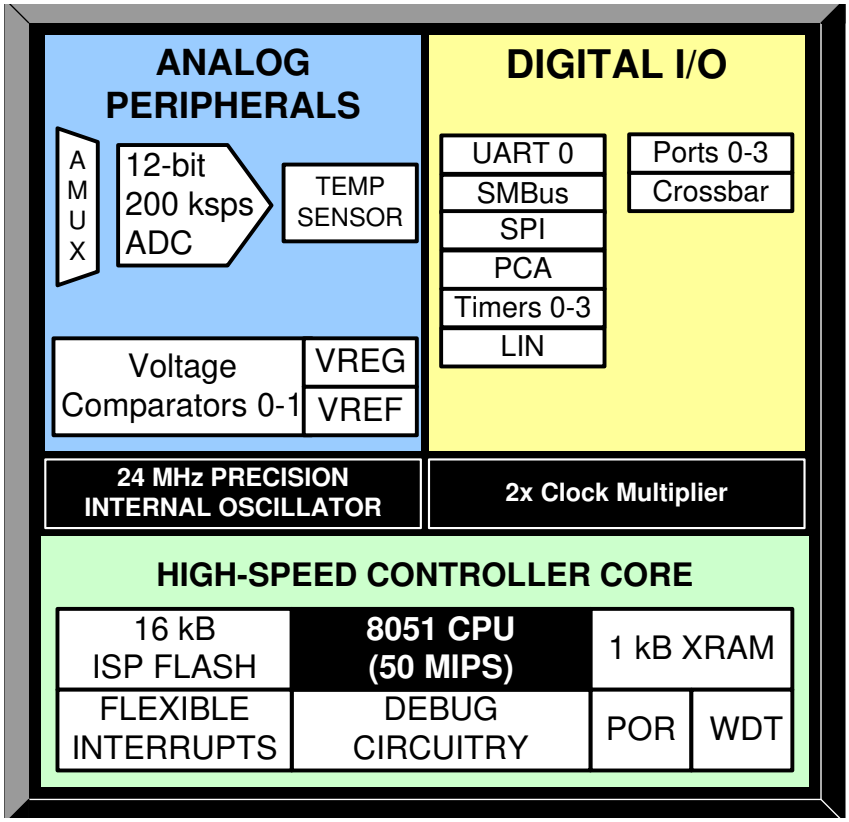
Memory
- 1280 bytes internal data RAM (256 + 1024 XRAM)
- 16 or 8 kB Flash; In-system programmable in 512-byte Sectors

Digital Peripherals
- 25 or 18 Port I/O; All 5 V tolerant
- LIN 2.1 Controller (Master and Slave capable); no crystal required
- Hardware enhanced UART, SMBus™, and enhanced SPI™ serial ports
- Four general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with six capture/compare modules and enhanced PWM functionality

Clock Sources
- Internal 24 MHz with ±0.5% accuracy master LIN operation
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly; useful in power saving modes

Packages
- 32-Pin QFP/QFN (C8051F540/1/4/5)
- 24-Pin QFN (C8051F542/3/6/7)

Automotive Qualified
- Temperature Range: –40 to +125 °C
- Compliant to AEC-Q100



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1. System Overview

C8051F54x devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- High-speed pipelined 8051-compatible microcontroller core (up to 50 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- LIN 2.1 peripheral (fully backwards compatible, master and slave modes) (C8051F540/2/4/6)
- True 12-bit 200 ksps 32-channel single-ended ADC with analog multiplexer
- Precision programmable 24 MHz internal oscillator that is within ±0.5% across the temperature range and for VDD voltages greater than or equal to the on-chip voltage regulator minimum output at the low setting. The oscillator is within ±1.0% for VDD voltages below this minimum output setting.
- On-chip Clock Multiplier to reach up to 50 MHz
- 16 kB (C8051F540/1/2/3) or 8 kB (C8051F544/5/6/7) of on-chip Flash memory
- 1280 bytes of on-chip RAM
- SMBus/I2C, Enhanced UART, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with six capture/compare modules and Watchdog Timer function
- On-chip Voltage Regulator
- On-chip Power-On Reset, V_{DD} Monitor, and Temperature Sensor
- On-chip Voltage Comparator
- 25 or 18 Port I/O (5 V push-pull)

With on-chip Voltage Regulator, Power-On Reset, V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051F54x devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

The devices are specified for 1.8 V to 5.25 V operation over the automotive temperature range (–40 to +125 °C). The C8051F540/1/4/5 devices are available in 32-pin QFP and QFN packages and the C8051F542/3/6/7 devices are available in 32-pin QFN packages. All package options are lead-free and RoHS compliant. See Table 2.1 for ordering information. Block diagrams are included in Figure 1.1 and Figure 1.2.

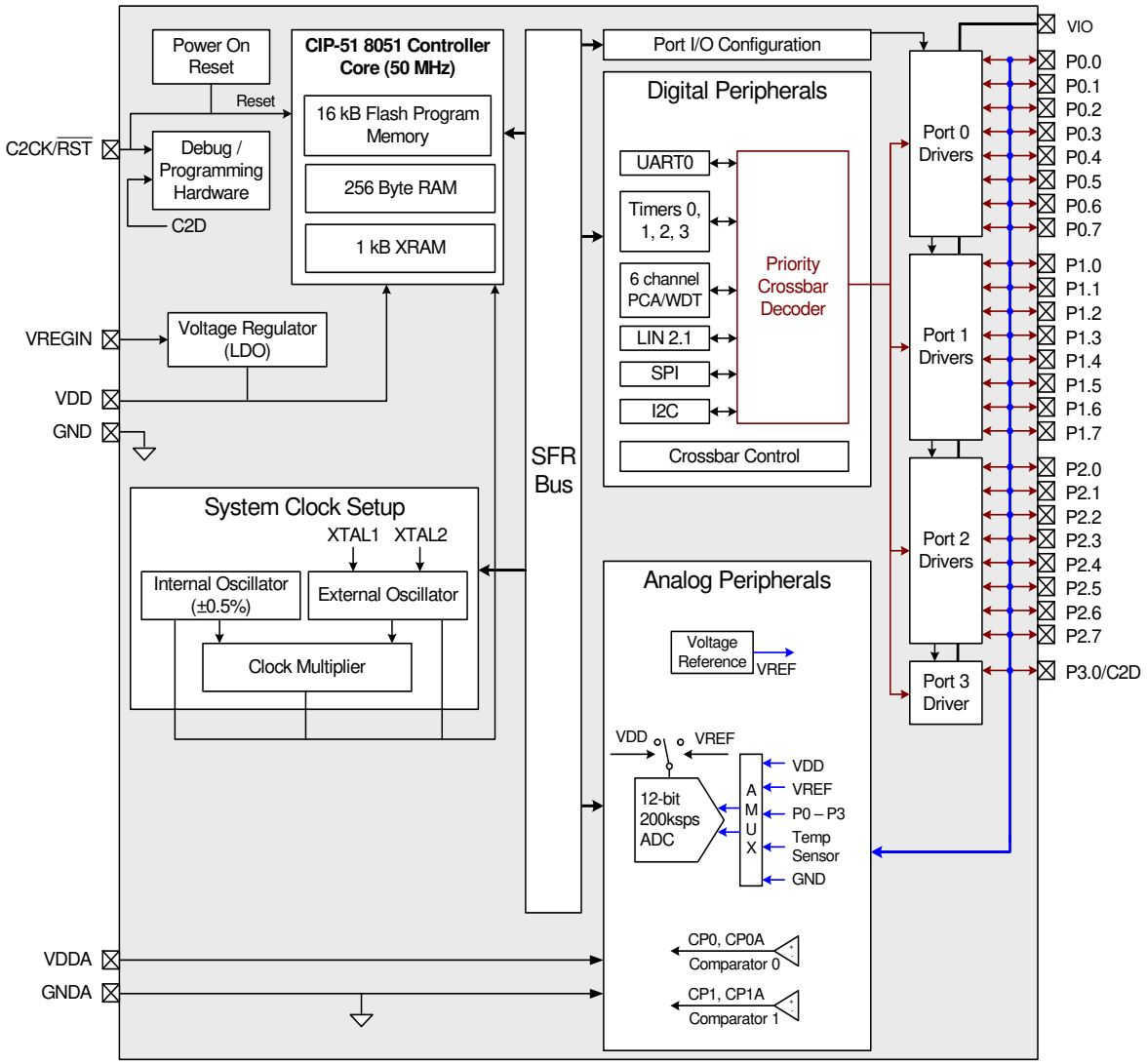

Figure 1.1. C8051F540/1/4/5 Block Diagram

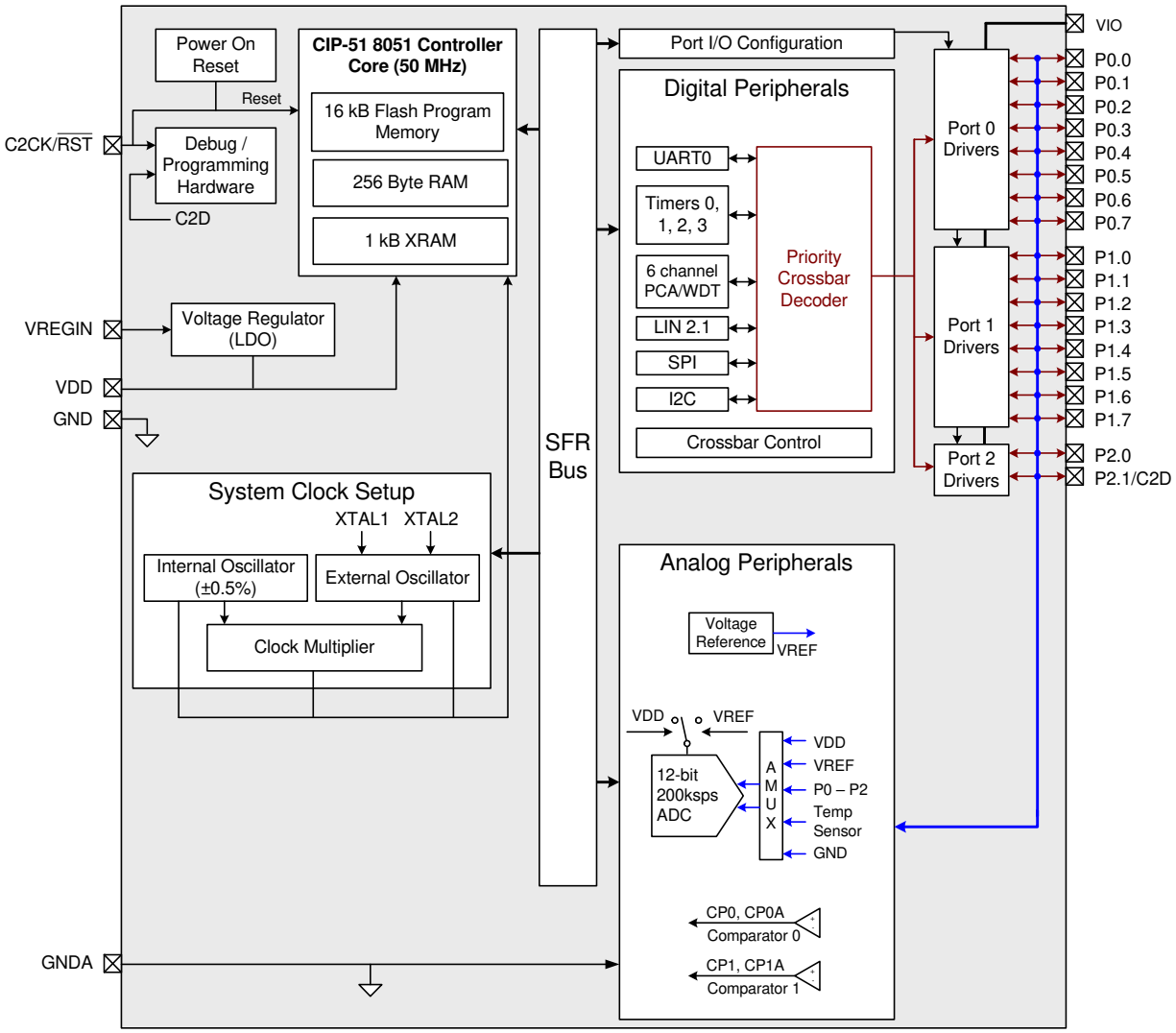

Figure 1.2. C8051F542/3/6/7 Block Diagram

2. Ordering Information

The following features are common to all devices in this family:

- 50 MHz system clock and 50 MIPS throughput (peak)
- 1280 bytes of RAM (256 internal bytes and 1024 XRAM bytes)
- Internal 24 MHz oscillator
- SMBus / I2C, Enhanced SPI, Enhanced UART
- Four Timers
- Six Programmable Counter Array channels
- Internal Voltage Regulator
- 12-bit, 200 ksps ADC, Internal Voltage Reference and Temperature Sensor
- Two Analog Comparators

Table 2.1 shows the features that differentiate the devices in this family.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	LIN2.1	Digital Port I/Os	Package
C8051F540-IQ	16	✓	25	QFP32
C8051F540-IM	16	✓	25	QFN32
C8051F541-IQ	16	—	25	QFP32
C8051F541-IM	16	—	25	QFN32
C8051F542-IM	16	✓	18	QFN24
C8051F543-IM	16	—	18	QFN24
C8051F544-IQ	8	✓	25	QFP32
C8051F544-IM	8	✓	25	QFN32
C8051F545-IQ	8	—	25	QFP32
C8051F545-IM	8	—	25	QFN32
C8051F546-IM	8	✓	18	QFN24
C8051F547-IM	8	—	18	QFN24

Note: The suffix of the part number indicates the device rating and the package. All devices are RoHS compliant.

All of these devices are also available in an automotive version. For the automotive version, the -I in the ordering part number is replaced with -A. For example, the automotive version of the C8051F540-IM is the C8051F540-AM.

The -AM and -AQ devices receive full automotive quality production status, including AEC-Q100 qualification, registration with International Material Data System (IMDS) and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at www.silabs.com with a registered and NDA approved user account. The -AM and -AQ devices enable high volume automotive OEM applications with their enhanced testing and processing. Please contact Silicon Labs sales for more information regarding –AM and -AQ devices for your automotive project.

3. Pin Definitions

Table 3.1. Pin Definitions for the C8051F54x

Name	Pin 'F540/1/4/5 (32-pin)	Pin 'F542/3/6/7 (24-pin)	Type	Description
VDD	4	3		Digital Supply Voltage. Must be connected.
GND	6	4		Digital Ground. Must be connected.
VDDA	5	—		Analog Supply Voltage. Must be connected. Connected internally to VDD on the 24-pin packages.
GNDA	7	5		Analog Ground. Must be connected.
VREGIN	3	2		Voltage Regulator Input
VIO	2	1		Port I/O Supply Voltage. Must be connected.
$\overline{\text{RST}}$/ C2CK	10	8	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} Monitor. Clock signal for the C2 Debug Interface.
P2.1/ C2D	—	7	D I/O or A In D I/O	Port 2.1. See SFR Definition 18.20 for a description. Bi-directional data signal for the C2 Debug Interface.
P3.0/ C2D	9	—	D I/O or A In D I/O	Port 3.0. See SFR Definition 18.24 for a description. Bi-directional data signal for the C2 Debug Interface.
P0.0	8	6	D I/O or A In	Port 0.0. See SFR Definition 18.12 for a description.
P0.1	1	24	D I/O or A In	Port 0.1
P0.2	32	23	D I/O or A In	Port 0.2
P0.3	31	22	D I/O or A In	Port 0.3
P0.4	30	21	D I/O or A In	Port 0.4
P0.5	29	20	D I/O or A In	Port 0.5
P0.6	28	19	D I/O or A In	Port 0.6
P0.7	27	18	D I/O or A In	Port 0.7
P1.0	26	17	D I/O or A In	Port 1.0. See SFR Definition 18.16 for a description.
P1.1	25	16	D I/O or A In	Port 1.1.
P1.2	24	15	D I/O or A In	Port 1.2.

Table 3.1. Pin Definitions for the C8051F54x (Continued)

Name	Pin ‘F540/1/4/5 (32-pin)	Pin ‘F542/3/6/7 (24-pin)	Type	Description
P1.3	23	14	D I/O or A In	Port 1.3.
P1.4	22	13	D I/O or A In	Port 1.4.
P1.5	21	12	D I/O or A In	Port 1.5.
P1.6	20	11	D I/O or A In	Port 1.6.
P1.7	19	10	D I/O or A In	Port 1.7.
P2.0	18	9	D I/O or A In	Port 2.0. See SFR Definition 18.20 for a description.
P2.1	17	—	D I/O or A In	Port 2.1.
P2.2	16	—	D I/O or A In	Port 2.2.
P2.3	15	—	D I/O or A In	Port 2.3.
P2.4	14	—	D I/O or A In	Port 2.4.
P2.5	13	—	D I/O or A In	Port 2.5.
P2.6	12	—	D I/O or A In	Port 2.6.
P2.7	11	—	D I/O or A In	Port 2.7.

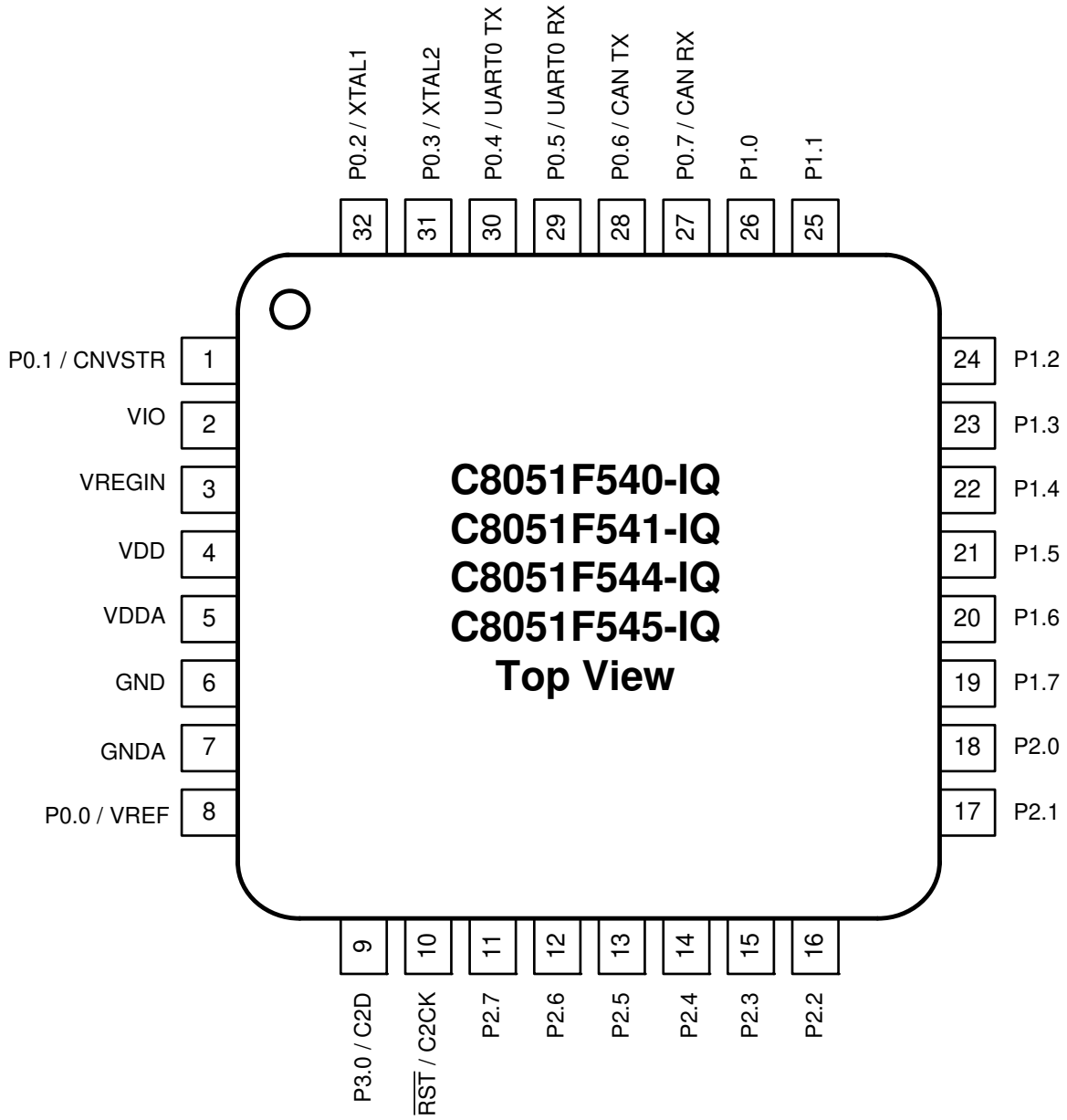

Figure 3.1. QFP-32 Pinout Diagram (Top View)

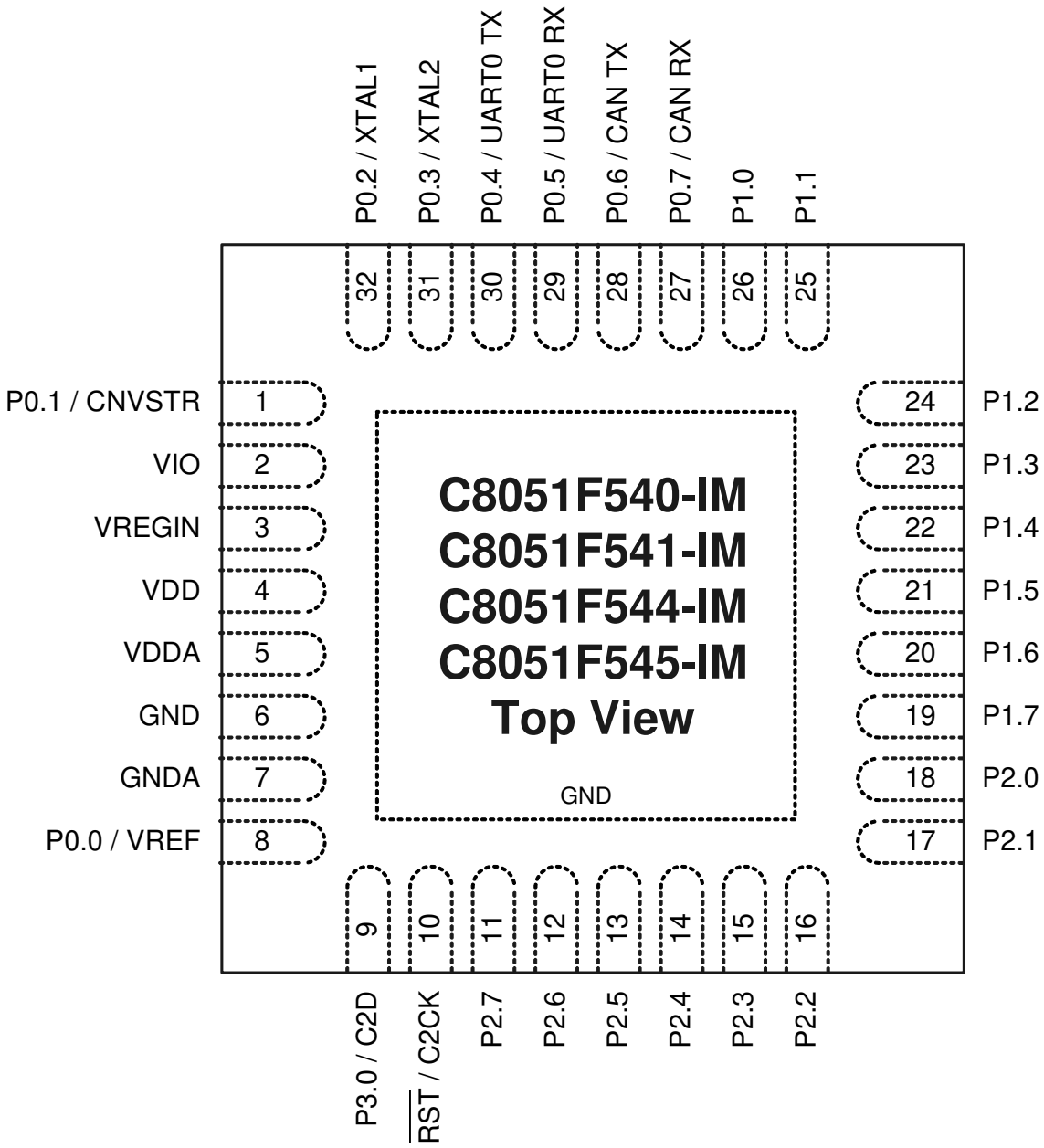

Figure 3.2. QFN-32 Pinout Diagram (Top View)

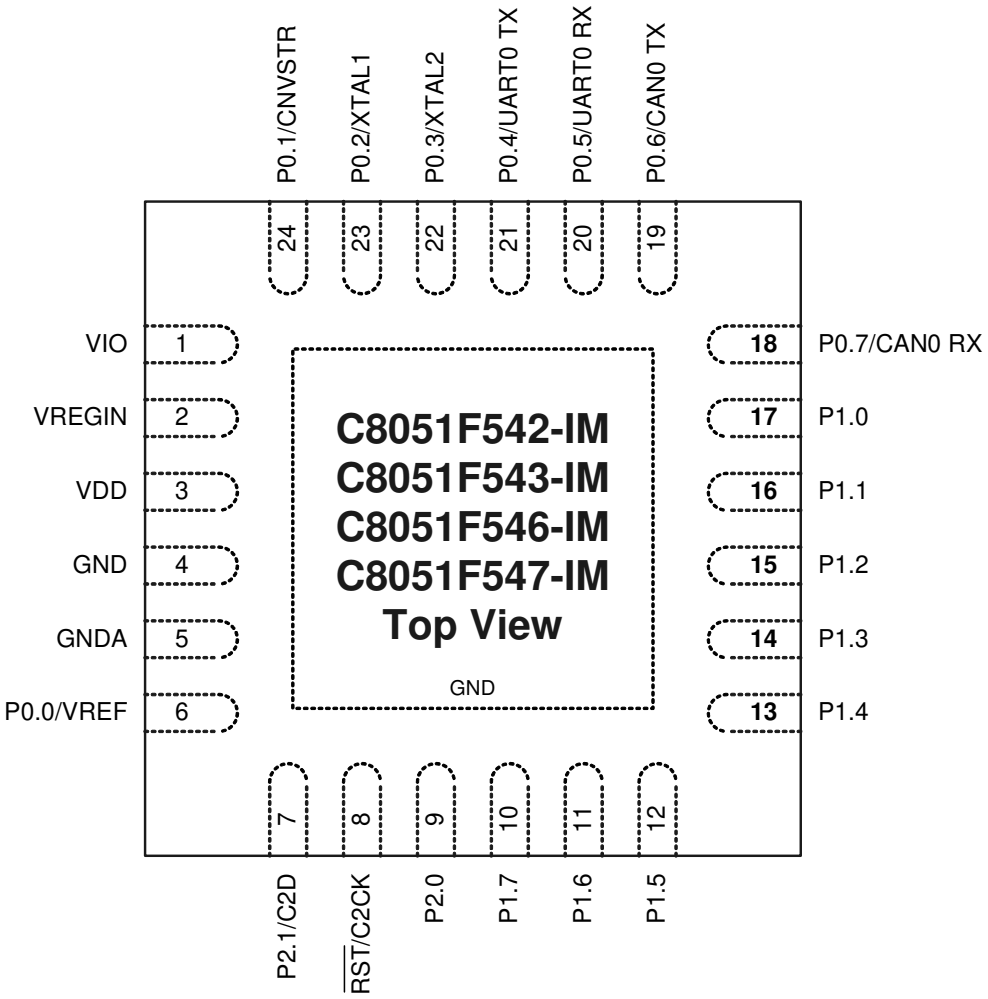

Figure 3.3. QFN-24 Pinout Diagram (Top View)

4. Package Specifications

4.1. QFP-32 Package Specifications

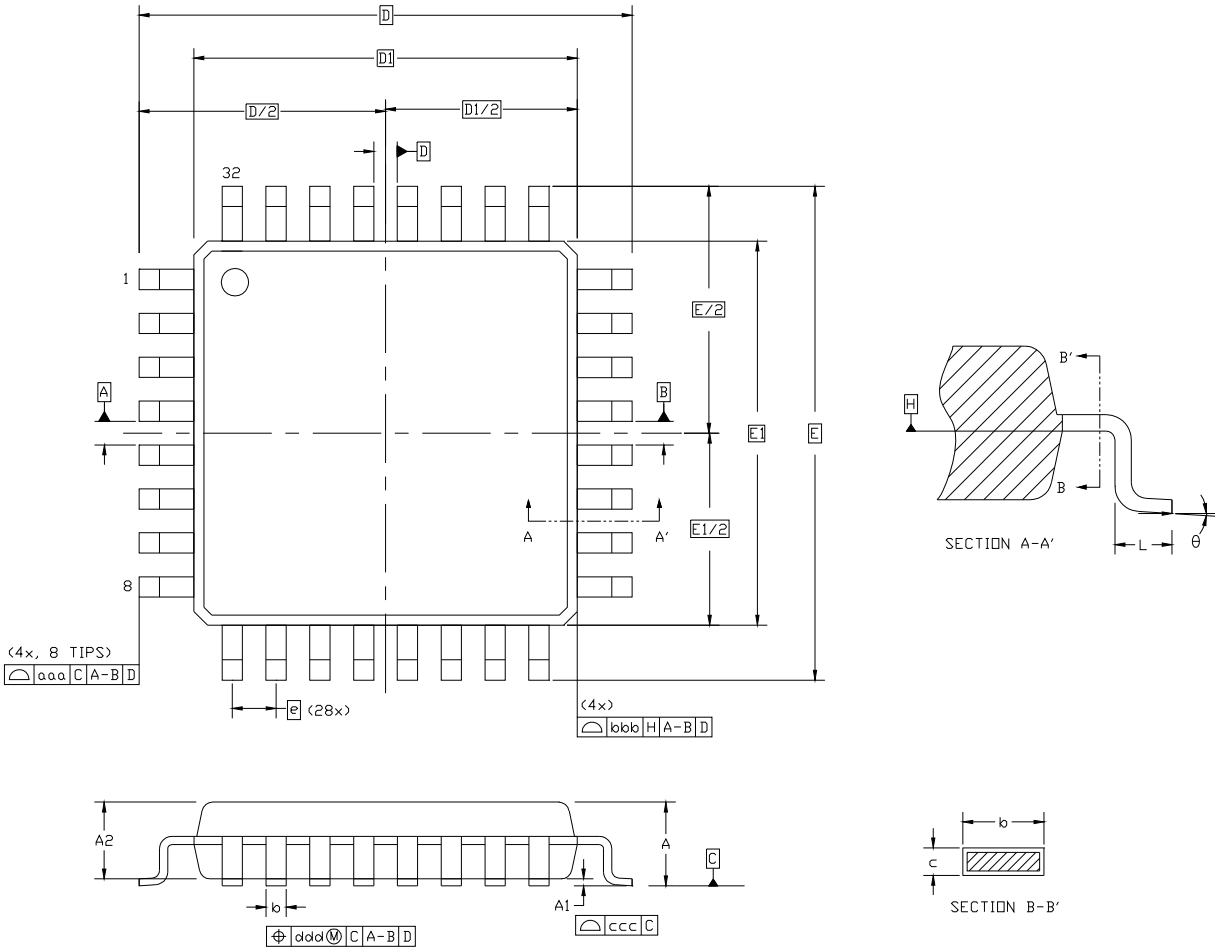

Figure 4.1. QFP-32 Package Drawing

Table 4.1. QFP-32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	—	0.20
D	9.00 BSC.		
D1	7.00 BSC.		
e	0.80 BSC.		

Dimension	Min	Typ	Max
E	9.00 BSC.		
E1	7.00 BSC.		
L	0.45	0.60	0.75
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
θ	0°	3.5°	7°

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

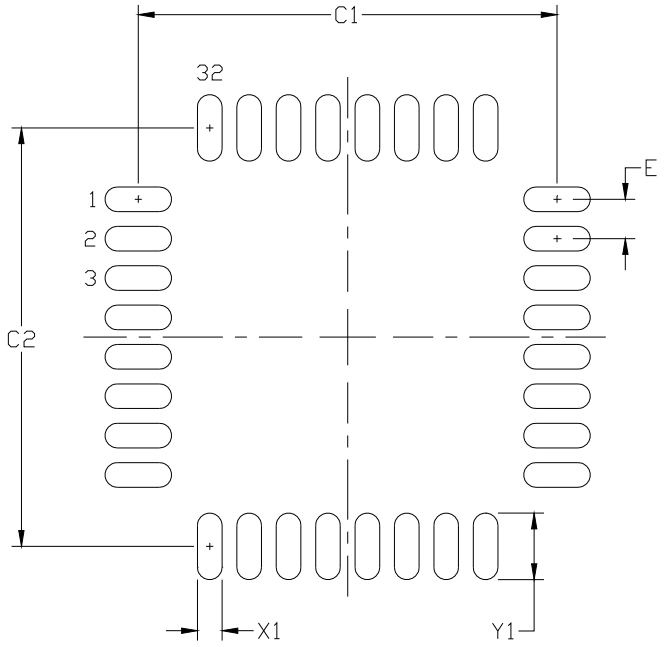

Figure 4.2. QFP-32 Landing Diagram

Table 4.2. QFP-32 Landing Diagram Dimensions

Dimension	Min	Max	Dimension	Min	Max
C1	8.40	8.50	X1	0.40	0.50
C2	8.40	8.50	Y1	1.25	1.35
E	0.80 BSC				

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

Card Assembly

7. A No-Clean, Type-3 solder paste is recommended.
8. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

4.2. QFN-32 Package Specifications

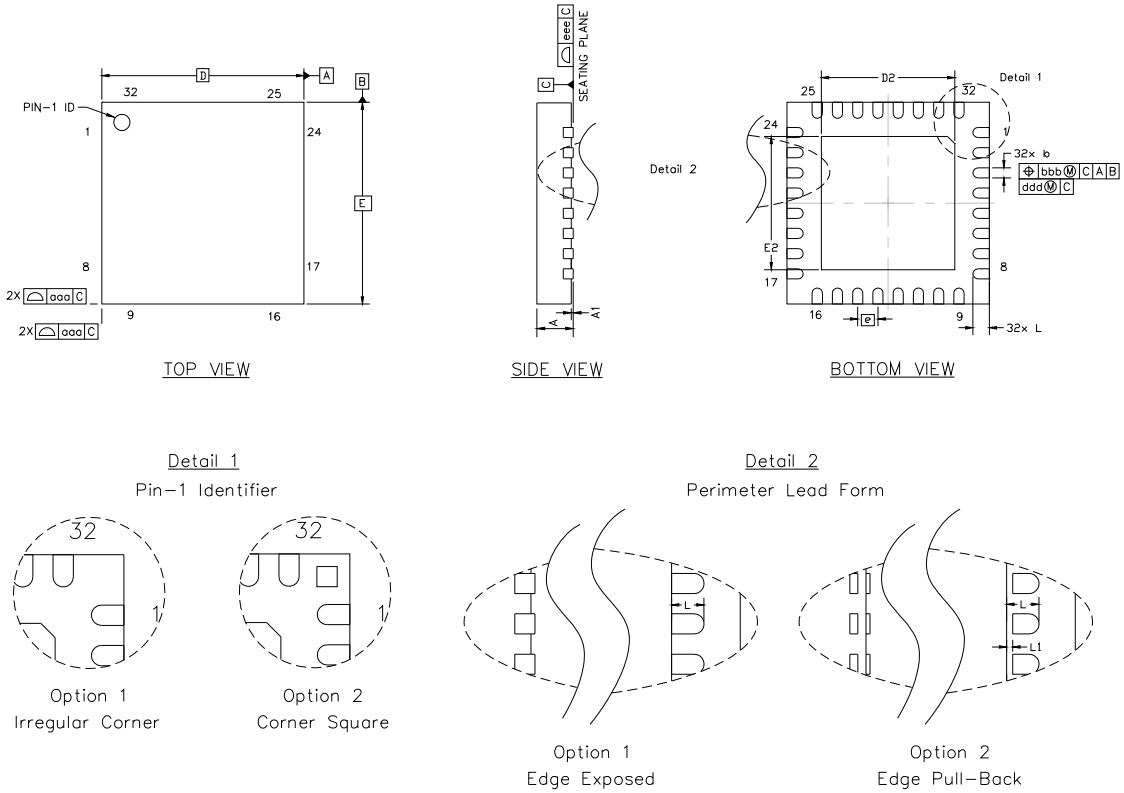

Figure 4.3. QFN-32 Package Drawing

Table 4.3. QFN-32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.9	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		5.00 BSC.	
D2	3.20	3.30	3.40
e		0.50 BSC.	
E		5.00 BSC.	

Dimension	Min	Typ	Max
E2	3.20	3.30	3.40
L	0.30	0.40	0.50
L1	0.00	—	0.15
aaa	—	—	0.15
bbb	—	—	0.15
ddd	—	—	0.05
eee	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.