



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



### Analog Peripherals

- **12-Bit ADC**
  - Up to 200 ksps
  - Up to 25 external single-ended inputs
  - VREF from on-chip VREF, external pin or V<sub>DD</sub>
  - Internal or external start of conversion source
  - Built-in temperature sensor
- **Two Comparators**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source
  - Low current

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Low cost, complete development kit

### Supply Voltage 1.8 to 5.25 V

- Typical operating current: 19 mA at 50 MHz;
- Typical stop mode current: 1 µA

### High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 50 MIPS throughput with 50 MHz clock
- Expanded interrupt handler

### Memory

- 1280 bytes internal data RAM (256 + 1024 XRAM)
- 16 or 8 kB Flash; In-system programmable in 512-byte Sectors

### Digital Peripherals

- 25 or 18 Port I/O; All 5 V tolerant
- LIN 2.1 Controller (Master and Slave capable); no crystal required
- Hardware enhanced UART, SMBus™, and enhanced SPI™ serial ports
- Four general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with six capture/compare modules and enhanced PWM functionality

### Clock Sources

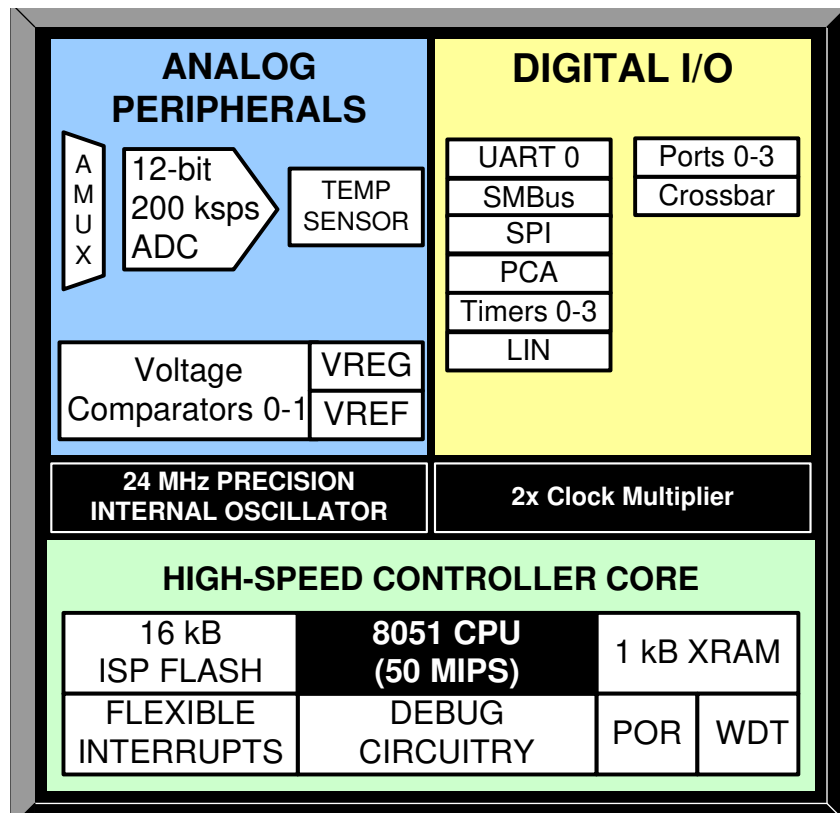
- Internal 24 MHz with ±0.5% accuracy master LIN operation
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly; useful in power saving modes

### Packages

- 32-Pin QFP/QFN (C8051F540/1/4/5)
- 24-Pin QFN (C8051F542/3/6/7)

### Automotive Qualified

- Temperature Range: -40 to +125 °C
- Compliant to AEC-Q100



# C8051F54x

---



---

## Table of Contents

<b>1. System Overview</b> .....	<b>13</b>
<b>2. Ordering Information</b> .....	<b>16</b>
<b>3. Pin Definitions</b> .....	<b>18</b>
<b>4. Package Specifications</b> .....	<b>23</b>
4.1. QFP-32 Package Specifications.....	23
4.2. QFN-32 Package Specifications.....	25
4.3. QFN-24 Package Specifications.....	27
<b>5. 12-Bit ADC (ADC0)</b> .....	<b>29</b>
5.1. Modes of Operation .....	30
5.2. Output Code Formatting .....	34
5.3. Selectable Gain .....	35
5.4. Programmable Window Detector.....	43
<b>6. Electrical Characteristics</b> .....	<b>47</b>
6.1. Absolute Maximum Specifications.....	47
6.2. Electrical Characteristics .....	48
6.1. ADC0 Analog Multiplexer .....	58
6.2. Temperature Sensor.....	60
<b>7. Voltage Reference</b> .....	<b>61</b>
<b>8. Comparators</b> .....	<b>63</b>
8.1. Comparator Multiplexer .....	69
<b>9. Voltage Regulator (REG0)</b> .....	<b>72</b>
<b>10. CIP-51 Microcontroller</b> .....	<b>74</b>
10.1. Performance .....	74
10.2. Instruction Set.....	76
10.3. CIP-51 Register Descriptions .....	80
10.4. Serial Number Special Function Registers (SFRs) .....	84
<b>11. Memory Organization</b> .....	<b>85</b>
11.1. Program Memory.....	85
11.2. Data Memory .....	86
11.3. External RAM .....	87
<b>12. Special Function Registers</b> .....	<b>89</b>
12.1. SFR Paging .....	89
12.2. Interrupts and SFR Paging.....	89
12.3. SFR Page Stack Example .....	91
<b>13. Interrupts</b> .....	<b>105</b>
13.1. MCU Interrupt Sources and Vectors.....	105
13.2. Interrupt Register <u>Descriptions</u> .....	108
13.3. External Interrupts INT0 and INT1.....	115
<b>14. Flash Memory</b> .....	<b>117</b>
14.1. Programming the Flash Memory .....	117
14.2. Non-volatile Data Storage .....	119
14.3. Security Options .....	119
14.4. Flash Write and Erase Guidelines.....	121

# C8051F54x

---

<b>15. Power Management Modes</b> .....	<b>126</b>
15.1. Idle Mode.....	126
15.2. Stop Mode.....	127
15.3. Suspend Mode.....	127
<b>16. Reset Sources</b> .....	<b>129</b>
16.1. Power-On Reset.....	130
16.2. Power-Fail Reset/VDD Monitor.....	130
16.3. External Reset.....	132
16.4. Missing Clock Detector Reset.....	132
16.5. Comparator0 Reset.....	133
16.6. PCA Watchdog Timer Reset.....	133
16.7. Flash Error Reset.....	133
16.8. Software Reset.....	133
<b>17. Oscillators and Clock Selection</b> .....	<b>135</b>
17.1. System Clock Selection.....	135
17.2. Programmable Internal Oscillator.....	137
17.3. Clock Multiplier.....	140
17.4. External Oscillator Drive Circuit.....	142
<b>18. Port Input/Output</b> .....	<b>147</b>
18.1. Port I/O Modes of Operation.....	148
18.2. Assigning Port I/O Pins to Analog and Digital Functions.....	149
18.3. Priority Crossbar Decoder.....	150
18.4. Port I/O Initialization.....	152
18.5. Port Match.....	157
18.6. Special Function Registers for Accessing and Configuring Port I/O.....	161
<b>19. Local Interconnect Network (LIN)</b> .....	<b>170</b>
19.1. Software Interface with the LIN Controller.....	171
19.2. LIN Interface Setup and Operation.....	171
19.3. LIN Master Mode Operation.....	174
19.4. LIN Slave Mode Operation.....	175
19.5. Sleep Mode and Wake-Up.....	176
19.6. Error Detection and Handling.....	176
19.7. LIN Registers.....	177
<b>20. SMBus</b> .....	<b>187</b>
20.1. Supporting Documents.....	188
20.2. SMBus Configuration.....	188
20.3. SMBus Operation.....	188
20.4. Using the SMBus.....	190
20.5. SMBus Transfer Modes.....	197
20.6. SMBus Status Decoding.....	201
<b>21. UART0</b> .....	<b>205</b>
21.1. Baud Rate Generator.....	205
21.2. Data Format.....	207
21.3. Configuration and Operation.....	208
<b>22. Enhanced Serial Peripheral Interface (SPI0)</b> .....	<b>214</b>

---

---

22.1. Signal Descriptions.....	215
22.2. SPI0 Master Mode Operation.....	216
22.3. SPI0 Slave Mode Operation.....	218
22.4. SPI0 Interrupt Sources.....	218
22.5. Serial Clock Phase and Polarity.....	219
22.6. SPI Special Function Registers.....	220
<b>23. Timers.....</b>	<b>227</b>
23.1. Timer 0 and Timer 1.....	229
23.2. Timer 2.....	237
23.3. Timer 3.....	243
<b>24. Programmable Counter Array.....</b>	<b>249</b>
24.1. PCA Counter/Timer.....	250
24.2. PCA0 Interrupt Sources.....	251
24.3. Capture/Compare Modules.....	252
24.4. Watchdog Timer Mode.....	260
24.5. Register Descriptions for PCA0.....	263
<b>25. C2 Interface.....</b>	<b>269</b>
25.1. C2 Interface Registers.....	269
25.2. C2 Pin Sharing.....	272

## List of Figures

Figure 1.1. C8051F540/1/4/5 Block Diagram .....	14
Figure 1.2. C8051F542/3/6/7 Block Diagram .....	15
Figure 3.1. QFP-32 Pinout Diagram (Top View) .....	20
Figure 3.2. QFN-32 Pinout Diagram (Top View) .....	21
Figure 3.3. QFN-24 Pinout Diagram (Top View) .....	22
Figure 4.1. QFP-32 Package Drawing .....	23
Figure 4.2. QFP-32 Landing Diagram .....	24
Figure 4.3. QFN-32 Package Drawing .....	25
Figure 4.4. QFN-32 Landing Diagram .....	26
Figure 4.5. QFN-24 Package Drawing .....	27
Figure 4.6. QFN-24 Landing Diagram .....	28
Figure 5.1. ADC0 Functional Block Diagram .....	29
Figure 5.2. ADC0 Tracking Modes .....	31
Figure 5.3. 12-Bit ADC Tracking Mode Example .....	32
Figure 5.4. 12-Bit ADC Burst Mode Example With Repeat Count Set to 4 .....	33
Figure 5.5. ADC0 Equivalent Input Circuit .....	35
Figure 5.6. ADC Window Compare Example: Right-Justified Data .....	46
Figure 5.7. ADC Window Compare Example: Left-Justified Data .....	46
Figure 6.1. Minimum VDD Monitor Threshold vs. System Clock Frequency .....	50
Figure 6.2. ADC0 Multiplexer Block Diagram .....	58
Figure 6.3. Temperature Sensor Transfer Function .....	60
Figure 7.1. Voltage Reference Functional Block Diagram .....	61
Figure 8.1. Comparator Functional Block Diagram .....	63
Figure 8.2. Comparator Hysteresis Plot .....	64
Figure 8.3. Comparator Input Multiplexer Block Diagram .....	69
Figure 9.1. External Capacitors for Voltage Regulator Input/Output— Regulator Enabled .....	72
Figure 9.2. External Capacitors for Voltage Regulator Input/Output—Regulator Dis- abled .....	73
Figure 10.1. CIP-51 Block Diagram .....	75
Figure 11.1. C8051F54x Memory Map .....	85
Figure 11.2. Flash Program Memory Map .....	86
Figure 12.1. SFR Page Stack .....	90
Figure 12.2. SFR Page Stack While Using SFR Page 0x0 To Access SMB0ADR ..	91
Figure 12.3. SFR Page Stack After SPI0 Interrupt Occurs .....	92
Figure 12.4. SFR Page Stack Upon PCA Interrupt Occurring During a SPI0 ISR ..	93
Figure 12.5. SFR Page Stack Upon Return From PCA Interrupt .....	94
Figure 12.6. SFR Page Stack Upon Return From SPI0 Interrupt .....	95
Figure 14.1. Flash Program Memory Map .....	119
Figure 16.1. Reset Sources .....	129
Figure 16.2. Power-On and VDD Monitor Reset Timing .....	130
Figure 17.1. Oscillator Options .....	135
Figure 17.2. Example Clock Multiplier Output .....	140

# C8051F54x

---

Figure 17.3. External 32.768 kHz Quartz Crystal Oscillator Connection Diagram	145
Figure 18.1. Port I/O Functional Block Diagram	147
Figure 18.2. Port I/O Cell Block Diagram	148
Figure 18.3. Peripheral Availability on Port I/O Pins	151
Figure 18.4. Crossbar Priority Decoder in Example Configuration	152
Figure 19.1. LIN Block Diagram	170
Figure 20.1. SMBus Block Diagram	187
Figure 20.2. Typical SMBus Configuration	188
Figure 20.3. SMBus Transaction	189
Figure 20.4. Typical SMBus SCL Generation	191
Figure 20.5. Typical Master Write Sequence	198
Figure 20.6. Typical Master Read Sequence	199
Figure 20.7. Typical Slave Write Sequence	200
Figure 20.8. Typical Slave Read Sequence	201
Figure 21.1. UART0 Block Diagram	205
Figure 21.2. UART0 Timing Without Parity or Extra Bit	207
Figure 21.3. UART0 Timing With Parity	207
Figure 21.4. UART0 Timing With Extra Bit	207
Figure 21.5. Typical UART Interconnect Diagram	208
Figure 21.6. UART Multi-Processor Mode Interconnect Diagram	209
Figure 22.1. SPI Block Diagram	214
Figure 22.2. Multiple-Master Mode Connection Diagram	217
Figure 22.3. 3-Wire Single Master and 3-Wire Single Slave Mode Connection Diagram	217
Figure 22.4. 4-Wire Single Master Mode and 4-Wire Slave Mode Connection Diagram	217
Figure 22.5. Master Mode Data/Clock Timing	219
Figure 22.6. Slave Mode Data/Clock Timing (CKPHA = 0)	220
Figure 22.7. Slave Mode Data/Clock Timing (CKPHA = 1)	220
Figure 22.8. SPI Master Timing (CKPHA = 0)	224
Figure 22.9. SPI Master Timing (CKPHA = 1)	224
Figure 22.10. SPI Slave Timing (CKPHA = 0)	225
Figure 22.11. SPI Slave Timing (CKPHA = 1)	225
Figure 23.1. T0 Mode 0 Block Diagram	230
Figure 23.2. T0 Mode 2 Block Diagram	231
Figure 23.3. T0 Mode 3 Block Diagram	232
Figure 23.4. Timer 2 16-Bit Mode Block Diagram	237
Figure 23.5. Timer 2 8-Bit Mode Block Diagram	238
Figure 23.6. Timer 2 External Oscillator Capture Mode Block Diagram	239
Figure 23.7. Timer 3 16-Bit Mode Block Diagram	243
Figure 23.8. Timer 3 8-Bit Mode Block Diagram	244
Figure 23.9. Timer 3 External Oscillator Capture Mode Block Diagram	245
Figure 24.1. PCA Block Diagram	249
Figure 24.2. PCA Counter/Timer Block Diagram	251

---



---

Figure 24.3. PCA Interrupt Block Diagram .....	252
Figure 24.4. PCA Capture Mode Diagram .....	254
Figure 24.5. PCA Software Timer Mode Diagram .....	255
Figure 24.6. PCA High-Speed Output Mode Diagram .....	256
Figure 24.7. PCA Frequency Output Mode .....	257
Figure 24.8. PCA 8-Bit PWM Mode Diagram .....	258
Figure 24.9. PCA 9, 10 and 11-Bit PWM Mode Diagram .....	259
Figure 24.10. PCA 16-Bit PWM Mode .....	260
Figure 24.11. PCA Module 2 with Watchdog Timer Enabled .....	261
Figure 25.1. Typical C2 Pin Sharing .....	272

## List of Tables

Table 2.1. Product Selection Guide .....	17
Table 3.1. Pin Definitions for the C8051F54x .....	18
Table 4.1. QFP-32 Package Dimensions .....	23
Table 4.2. QFP-32 Landing Diagram Dimensions .....	24
Table 4.3. QFN-32 Package Dimensions .....	25
Table 4.4. QFN-32 Landing Diagram Dimensions .....	26
Table 4.5. QFN-24 Package Dimensions .....	27
Table 4.6. QFN-24 Landing Diagram Dimensions .....	28
Table 6.1. Absolute Maximum Ratings .....	47
Table 6.2. Global Electrical Characteristics .....	48
Table 6.3. Port I/O DC Electrical Characteristics .....	51
Table 6.4. Reset Electrical Characteristics .....	52
Table 6.5. Flash Electrical Characteristics .....	52
Table 6.6. Internal High-Frequency Oscillator Electrical Characteristics .....	53
Table 6.7. Clock Multiplier Electrical Specifications .....	54
Table 6.8. Voltage Regulator Electrical Characteristics .....	54
Table 6.9. ADC0 Electrical Characteristics .....	55
Table 6.10. Temperature Sensor Electrical Characteristics .....	56
Table 6.11. Voltage Reference Electrical Characteristics .....	56
Table 6.12. Comparator 0 and Comparator 1 Electrical Characteristics .....	57
Table 10.1. CIP-51 Instruction Set Summary .....	77
Table 12.1. Special Function Register (SFR) Memory Map for Pages 0x0 and 0xF .....	100
Table 12.2. Special Function Registers .....	101
Table 13.1. Interrupt Summary .....	107
Table 14.1. Flash Security Summary .....	120
Table 18.1. Port I/O Assignment for Analog Functions .....	149
Table 18.2. Port I/O Assignment for Digital Functions .....	149
Table 18.3. Port I/O Assignment for External Digital Event Capture Functions ....	150
Table 19.1. Baud Rate Calculation Variable Ranges .....	171
Table 19.2. Manual Baud Rate Parameters Examples .....	173
Table 19.3. Autobaud Parameters Examples .....	174
Table 19.4. LIN Registers* (Indirectly Addressable) .....	179
Table 20.1. SMBus Clock Source Selection .....	191
Table 20.2. Minimum SDA Setup and Hold Times .....	192
Table 20.3. Sources for Hardware Changes to SMB0CN .....	196
Table 20.4. SMBus Status Decoding .....	202
Table 21.1. Baud Rate Generator Settings for Standard Baud Rates .....	206
Table 22.1. SPI Slave Timing Parameters .....	226
Table 24.1. PCA Timebase Input Options .....	250
Table 24.2. PCA0CPM and PCA0PWM Bit Settings for PCA Capture/Compare Modules .....	253
Table 24.3. Watchdog Timer Timeout Intervals1 .....	262

---

## List of Registers

SFR Definition 5.4. ADC0CF: ADC0 Configuration .....	40
SFR Definition 5.5. ADC0H: ADC0 Data Word MSB .....	41
SFR Definition 5.6. ADC0L: ADC0 Data Word LSB .....	41
SFR Definition 5.7. ADC0CN: ADC0 Control .....	42
SFR Definition 5.8. ADC0TK: ADC0 Tracking Mode Select .....	43
SFR Definition 5.9. ADC0GTH: ADC0 Greater-Than Data High Byte .....	44
SFR Definition 5.10. ADC0GTL: ADC0 Greater-Than Data Low Byte .....	44
SFR Definition 5.11. ADC0LTH: ADC0 Less-Than Data High Byte .....	45
SFR Definition 5.12. ADC0LTL: ADC0 Less-Than Data Low Byte .....	45
SFR Definition 6.3. ADC0MX: ADC0 Channel Select .....	59
SFR Definition 7.1. REF0CN: Reference Control .....	62
SFR Definition 8.1. CPT0CN: Comparator0 Control .....	65
SFR Definition 8.2. CPT0MD: Comparator0 Mode Selection .....	66
SFR Definition 8.3. CPT1CN: Comparator1 Control .....	67
SFR Definition 8.4. CPT1MD: Comparator1 Mode Selection .....	68
SFR Definition 8.5. CPT0MX: Comparator0 MUX Selection .....	70
SFR Definition 8.6. CPT1MX: Comparator1 MUX Selection .....	71
SFR Definition 9.1. REG0CN: Regulator Control .....	73
SFR Definition 10.1. DPL: Data Pointer Low Byte .....	81
SFR Definition 10.2. DPH: Data Pointer High Byte .....	81
SFR Definition 10.3. SP: Stack Pointer .....	82
SFR Definition 10.4. ACC: Accumulator .....	82
SFR Definition 10.5. B: B Register .....	82
SFR Definition 10.6. PSW: Program Status Word .....	83
SFR Definition 10.7. SNn: Serial Number n .....	84
SFR Definition 11.1. EMI0CN: External Memory Interface Control .....	88
SFR Definition 12.1. SFR0CN: SFR Page Control .....	96
SFR Definition 12.2. SFRPAGE: SFR Page .....	97
SFR Definition 12.3. SFRNEXT: SFR Next .....	98
SFR Definition 12.4. SFRLAST: SFR Last .....	99
SFR Definition 13.1. IE: Interrupt Enable .....	109
SFR Definition 13.2. IP: Interrupt Priority .....	110
SFR Definition 13.3. EIE1: Extended Interrupt Enable 1 .....	111
SFR Definition 13.4. EIP1: Extended Interrupt Priority 1 .....	112
SFR Definition 13.5. EIE2: Extended Interrupt Enable 2 .....	113
SFR Definition 13.6. EIP2: Extended Interrupt Priority Enabled 2 .....	114
SFR Definition 13.7. IT01CF: INT0/INT1 Configuration .....	116
SFR Definition 14.1. PSCTL: Program Store R/W Control .....	122
SFR Definition 14.2. FLKEY: Flash Lock and Key .....	123
SFR Definition 14.3. FLSCL: Flash Scale .....	124
SFR Definition 14.4. CCH0CN: Cache Control .....	125
SFR Definition 14.5. ONESHOT: Flash Oneshot Period .....	125
SFR Definition 15.1. PCON: Power Control .....	128

# C8051F54x

---

SFR Definition 16.1. VDM0CN: VDD Monitor Control .....	132
SFR Definition 16.2. RSTSRC: Reset Source .....	134
SFR Definition 17.1. CLKSEL: Clock Select .....	136
SFR Definition 17.2. OSCICN: Internal Oscillator Control .....	138
SFR Definition 17.3. OSCICRS: Internal Oscillator Coarse Calibration .....	139
SFR Definition 17.4. OSCIFIN: Internal Oscillator Fine Calibration .....	139
SFR Definition 17.5. CLKMUL: Clock Multiplier .....	141
SFR Definition 17.6. OSCXCN: External Oscillator Control .....	143
SFR Definition 18.1. XBR0: Port I/O Crossbar Register 0 .....	154
SFR Definition 18.2. XBR1: Port I/O Crossbar Register 1 .....	155
SFR Definition 18.3. XBR2: Port I/O Crossbar Register 1 .....	156
SFR Definition 18.4. P0MASK: Port 0 Mask Register .....	157
SFR Definition 18.5. P0MAT: Port 0 Match Register .....	157
SFR Definition 18.6. P1MASK: Port 1 Mask Register .....	158
SFR Definition 18.7. P1MAT: Port 1 Match Register .....	158
SFR Definition 18.8. P2MASK: Port 2 Mask Register .....	159
SFR Definition 18.9. P2MAT: Port 2 Match Register .....	159
SFR Definition 18.10. P3MASK: Port 3 Mask Register .....	160
SFR Definition 18.11. P3MAT: Port 3 Match Register .....	160
SFR Definition 18.12. P0: Port 0 .....	161
SFR Definition 18.13. P0MDIN: Port 0 Input Mode .....	162
SFR Definition 18.14. P0MDOUT: Port 0 Output Mode .....	162
SFR Definition 18.15. P0SKIP: Port 0 Skip .....	163
SFR Definition 18.16. P1: Port 1 .....	163
SFR Definition 18.17. P1MDIN: Port 1 Input Mode .....	164
SFR Definition 18.18. P1MDOUT: Port 1 Output Mode .....	164
SFR Definition 18.19. P1SKIP: Port 1 Skip .....	165
SFR Definition 18.20. P2: Port 2 .....	165
SFR Definition 18.21. P2MDIN: Port 2 Input Mode .....	166
SFR Definition 18.22. P2MDOUT: Port 2 Output Mode .....	166
SFR Definition 18.23. P2SKIP: Port 2 Skip .....	167
SFR Definition 18.24. P3: Port 3 .....	167
SFR Definition 18.25. P3MDIN: Port 3 Input Mode .....	168
SFR Definition 18.26. P3MDOUT: Port 3 Output Mode .....	168
SFR Definition 18.27. P3SKIP: Port 3Skip .....	169
SFR Definition 19.1. LIN0ADR: LIN0 Indirect Address Register .....	177
SFR Definition 19.2. LIN0DAT: LIN0 Indirect Data Register .....	177
SFR Definition 19.3. LIN0CF: LIN0 Control Mode Register .....	178
SFR Definition 20.1. SMB0CF: SMBus Clock/Configuration .....	193
SFR Definition 20.2. SMB0CN: SMBus Control .....	195
SFR Definition 20.3. SMB0DAT: SMBus Data .....	197
SFR Definition 21.1. SCON0: Serial Port 0 Control .....	210
SFR Definition 21.2. SMOD0: Serial Port 0 Control .....	211
SFR Definition 21.3. SBUF0: Serial (UART0) Port Data Buffer .....	212
SFR Definition 21.4. SBCON0: UART0 Baud Rate Generator Control .....	212

---

---

SFR Definition 21.6. SBRLLO: UART0 Baud Rate Generator Reload Low Byte .....	213
SFR Definition 21.5. SBRLH0: UART0 Baud Rate Generator Reload High Byte .....	213
SFR Definition 22.1. SPI0CFG: SPI0 Configuration .....	221
SFR Definition 22.2. SPI0CN: SPI0 Control .....	222
SFR Definition 22.3. SPI0CKR: SPI0 Clock Rate .....	223
SFR Definition 22.4. SPI0DAT: SPI0 Data .....	223
SFR Definition 23.1. CKCON: Clock Control .....	228
SFR Definition 23.2. TCON: Timer Control .....	233
SFR Definition 23.3. TMOD: Timer Mode .....	234
SFR Definition 23.4. TL0: Timer 0 Low Byte .....	235
SFR Definition 23.5. TL1: Timer 1 Low Byte .....	235
SFR Definition 23.6. TH0: Timer 0 High Byte .....	236
SFR Definition 23.7. TH1: Timer 1 High Byte .....	236
SFR Definition 23.8. TMR2CN: Timer 2 Control .....	240
SFR Definition 23.9. TMR2RLL: Timer 2 Reload Register Low Byte .....	241
SFR Definition 23.10. TMR2RLH: Timer 2 Reload Register High Byte .....	241
SFR Definition 23.11. TMR2L: Timer 2 Low Byte .....	242
SFR Definition 23.12. TMR2H: Timer 2 High Byte .....	242
SFR Definition 23.13. TMR3CN: Timer 3 Control .....	246
SFR Definition 23.14. TMR3RLL: Timer 3 Reload Register Low Byte .....	247
SFR Definition 23.15. TMR3RLH: Timer 3 Reload Register High Byte .....	247
SFR Definition 23.16. TMR3L: Timer 3 Low Byte .....	248
SFR Definition 23.17. TMR3H: Timer 3 High Byte .....	248
SFR Definition 24.1. PCA0CN: PCA Control .....	263
SFR Definition 24.2. PCA0MD: PCA Mode .....	264
SFR Definition 24.3. PCA0PWM: PCA PWM Configuration .....	265
SFR Definition 24.4. PCA0CPMn: PCA Capture/Compare Mode .....	266
SFR Definition 24.5. PCA0L: PCA Counter/Timer Low Byte .....	267
SFR Definition 24.6. PCA0H: PCA Counter/Timer High Byte .....	267
SFR Definition 24.7. PCA0CPLn: PCA Capture Module Low Byte .....	268
SFR Definition 24.8. PCA0CPHn: PCA Capture Module High Byte .....	268

## 1. System Overview

C8051F54x devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- High-speed pipelined 8051-compatible microcontroller core (up to 50 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- LIN 2.1 peripheral (fully backwards compatible, master and slave modes) (C8051F540/2/4/6)
- True 12-bit 200 ksps 32-channel single-ended ADC with analog multiplexer
- Precision programmable 24 MHz internal oscillator that is within  $\pm 0.5\%$  across the temperature range and for VDD voltages greater than or equal to the on-chip voltage regulator minimum output at the low setting. The oscillator is within  $\pm 1.0\%$  for VDD voltages below this minimum output setting.
- On-chip Clock Multiplier to reach up to 50 MHz
- 16 kB (C8051F540/1/2/3) or 8 kB (C8051F544/5/6/7) of on-chip Flash memory
- 1280 bytes of on-chip RAM
- SMBus/I2C, Enhanced UART, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with six capture/compare modules and Watchdog Timer function
- On-chip Voltage Regulator
- On-chip Power-On Reset, V<sub>DD</sub> Monitor, and Temperature Sensor
- On-chip Voltage Comparator
- 25 or 18 Port I/O (5 V push-pull)

With on-chip Voltage Regulator, Power-On Reset, V<sub>DD</sub> monitor, Watchdog Timer, and clock oscillator, the C8051F54x devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

The devices are specified for 1.8 V to 5.25 V operation over the automotive temperature range ( $-40$  to  $+125$  °C). The C8051F540/1/4/5 devices are available in 32-pin QFP and QFN packages and the C8051F542/3/6/7 devices are available in 32-pin QFN packages. All package options are lead-free and RoHS compliant. See Table 2.1 for ordering information. Block diagrams are included in Figure 1.1 and Figure 1.2.

# C8051F54x

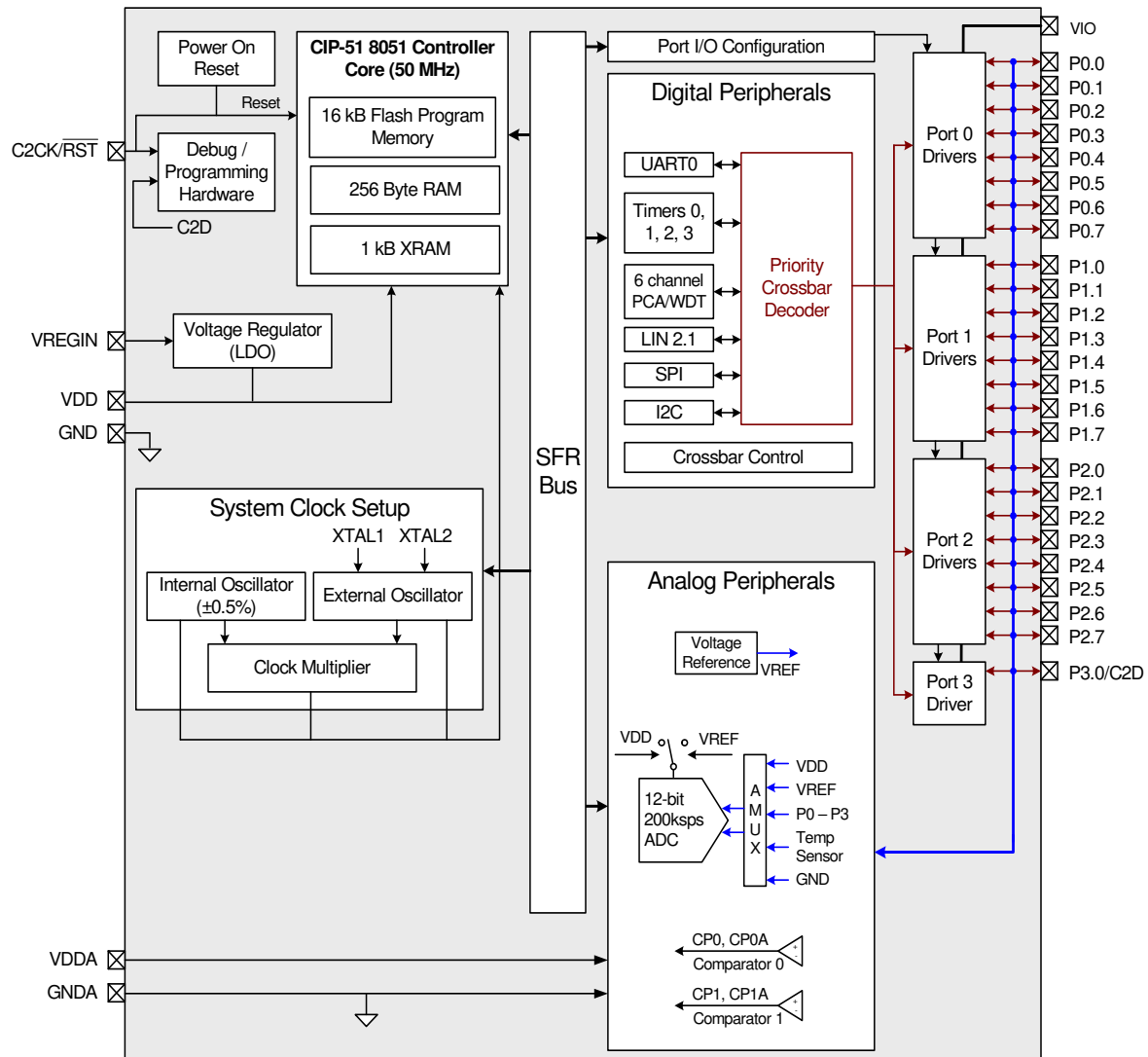


Figure 1.1. C8051F540/1/4/5 Block Diagram

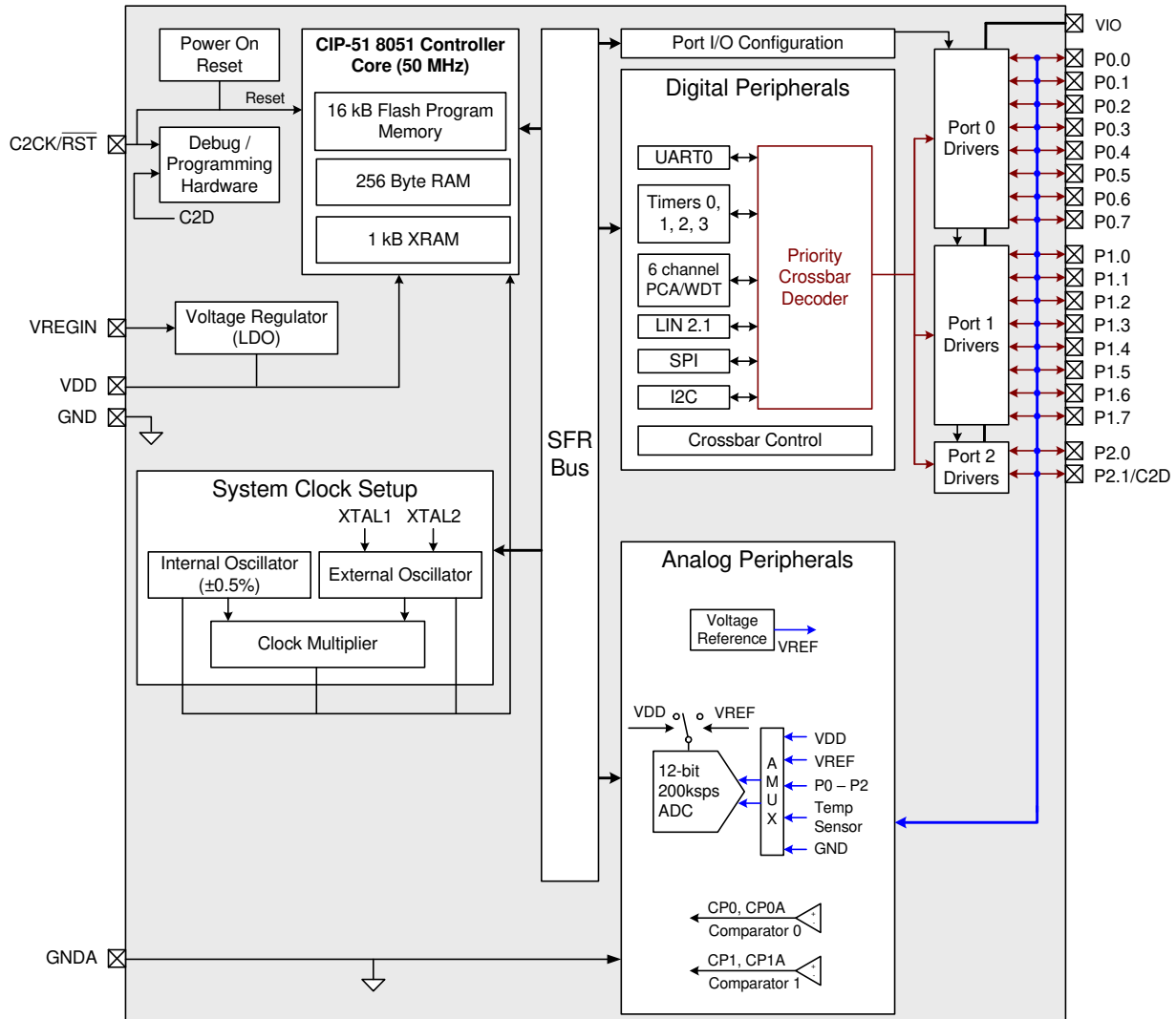


Figure 1.2. C8051F542/3/6/7 Block Diagram



## 2. Ordering Information

The following features are common to all devices in this family:

- 50 MHz system clock and 50 MIPS throughput (peak)
- 1280 bytes of RAM (256 internal bytes and 1024 XRAM bytes)
- Internal 24 MHz oscillator
- SMBus / I2C, Enhanced SPI, Enhanced UART
- Four Timers
- Six Programmable Counter Array channels
- Internal Voltage Regulator
- 12-bit, 200 ksps ADC, Internal Voltage Reference and Temperature Sensor
- Two Analog Comparators

Table 2.1 shows the features that differentiate the devices in this family.

**Table 2.1. Product Selection Guide**

Ordering Part Number	Flash Memory (kB)	LIN2.1	Digital Port I/Os	Package
C8051F540-IQ	16	✓	25	QFP32
C8051F540-IM	16	✓	25	QFN32
C8051F541-IQ	16	—	25	QFP32
C8051F541-IM	16	—	25	QFN32
C8051F542-IM	16	✓	18	QFN24
C8051F543-IM	16	—	18	QFN24
C8051F544-IQ	8	✓	25	QFP32
C8051F544-IM	8	✓	25	QFN32
C8051F545-IQ	8	—	25	QFP32
C8051F545-IM	8	—	25	QFN32
C8051F546-IM	8	✓	18	QFN24
C8051F547-IM	8	—	18	QFN24

**Note:** The suffix of the part number indicates the device rating and the package. All devices are RoHS compliant.

All of these devices are also available in an automotive version. For the automotive version, the -I in the ordering part number is replaced with -A. For example, the automotive version of the C8051F540-IM is the C8051F540-AM.

The -AM and -AQ devices receive full automotive quality production status, including AEC-Q100 qualification, registration with International Material Data System (IMDS) and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at [www.silabs.com](http://www.silabs.com) with a registered and NDA approved user account. The -AM and -AQ devices enable high volume automotive OEM applications with their enhanced testing and processing. Please contact Silicon Labs sales for more information regarding -AM and -AQ devices for your automotive project.

## 3. Pin Definitions

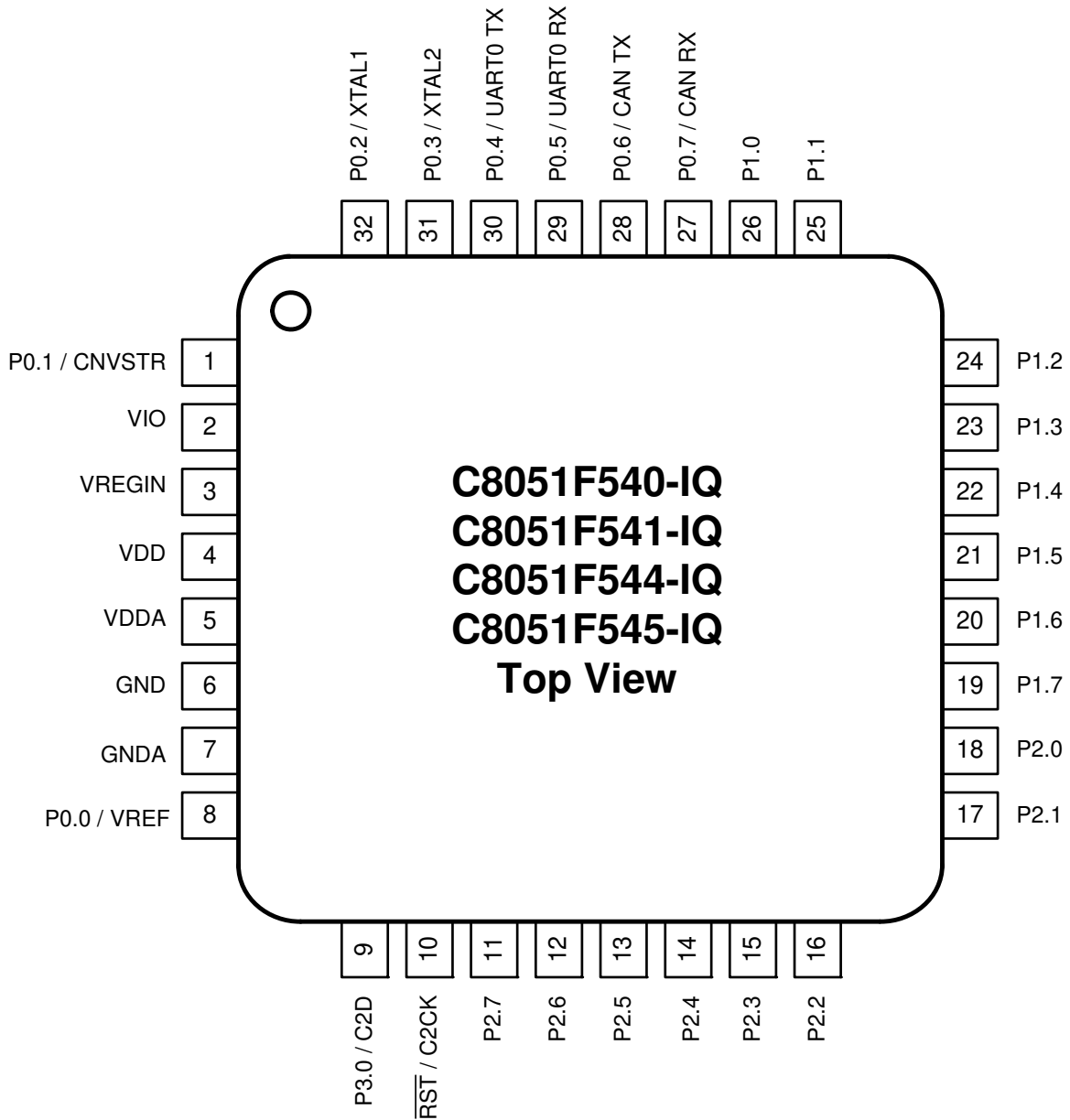
**Table 3.1. Pin Definitions for the C8051F54x**

Name	Pin 'F540/1/4/5 (32-pin)	Pin 'F542/3/6/7 (24-pin)	Type	Description
VDD	4	3		Digital Supply Voltage. Must be connected.
GND	6	4		Digital Ground. Must be connected.
VDDA	5	—		Analog Supply Voltage. Must be connected. Connected internally to VDD on the 24-pin packages.
GNDA	7	5		Analog Ground. Must be connected.
VREGIN	3	2		Voltage Regulator Input
VIO	2	1		Port I/O Supply Voltage. Must be connected.
$\overline{\text{RST}}$	10	8	D I/O	Device Reset. Open-drain output of internal POR or $V_{DD}$ Monitor.
C2CK			D I/O	Clock signal for the C2 Debug Interface.
P2.1/	—	7	D I/O or A In	Port 2.1. See SFR Definition 18.20 for a description.
C2D			D I/O	Bi-directional data signal for the C2 Debug Interface.
P3.0/	9	—	D I/O or A In	Port 3.0. See SFR Definition 18.24 for a description.
C2D			D I/O	Bi-directional data signal for the C2 Debug Interface.
P0.0	8	6	D I/O or A In	Port 0.0. See SFR Definition 18.12 for a description.
P0.1	1	24	D I/O or A In	Port 0.1
P0.2	32	23	D I/O or A In	Port 0.2
P0.3	31	22	D I/O or A In	Port 0.3
P0.4	30	21	D I/O or A In	Port 0.4
P0.5	29	20	D I/O or A In	Port 0.5
P0.6	28	19	D I/O or A In	Port 0.6
P0.7	27	18	D I/O or A In	Port 0.7
P1.0	26	17	D I/O or A In	Port 1.0. See SFR Definition 18.16 for a description.
P1.1	25	16	D I/O or A In	Port 1.1.
P1.2	24	15	D I/O or A In	Port 1.2.

# C8051F54x

Table 3.1. Pin Definitions for the C8051F54x (Continued)

Name	Pin 'F540/1/4/5 (32-pin)	Pin 'F542/3/6/7 (24-pin)	Type	Description
P1.3	23	14	D I/O or A In	Port 1.3.
P1.4	22	13	D I/O or A In	Port 1.4.
P1.5	21	12	D I/O or A In	Port 1.5.
P1.6	20	11	D I/O or A In	Port 1.6.
P1.7	19	10	D I/O or A In	Port 1.7.
P2.0	18	9	D I/O or A In	Port 2.0. See SFR Definition 18.20 for a description.
P2.1	17	—	D I/O or A In	Port 2.1.
P2.2	16	—	D I/O or A In	Port 2.2.
P2.3	15	—	D I/O or A In	Port 2.3.
P2.4	14	—	D I/O or A In	Port 2.4.
P2.5	13	—	D I/O or A In	Port 2.5.
P2.6	12	—	D I/O or A In	Port 2.6.
P2.7	11	—	D I/O or A In	Port 2.7.



**Figure 3.1. QFP-32 Pinout Diagram (Top View)**

# C8051F54x

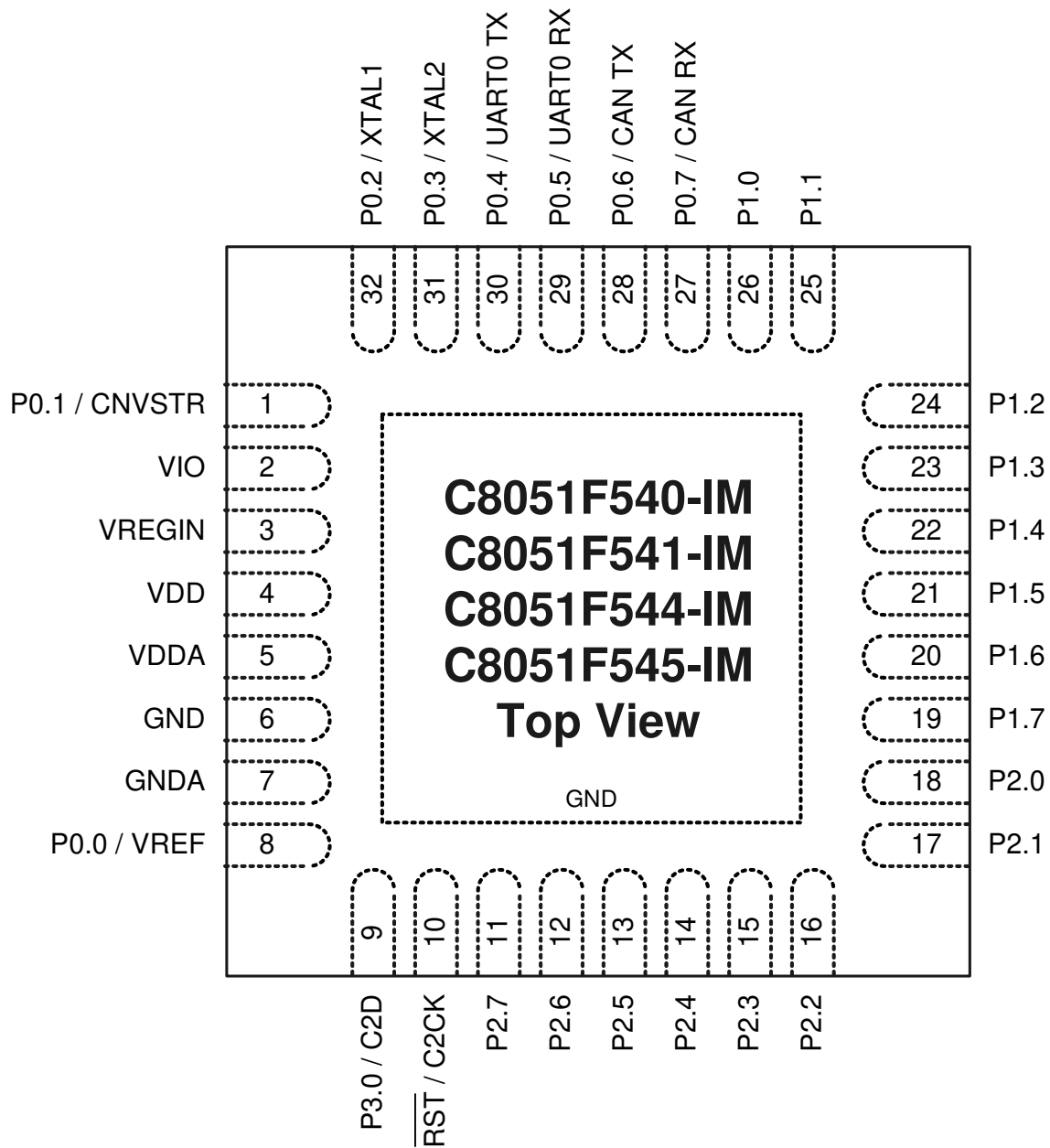
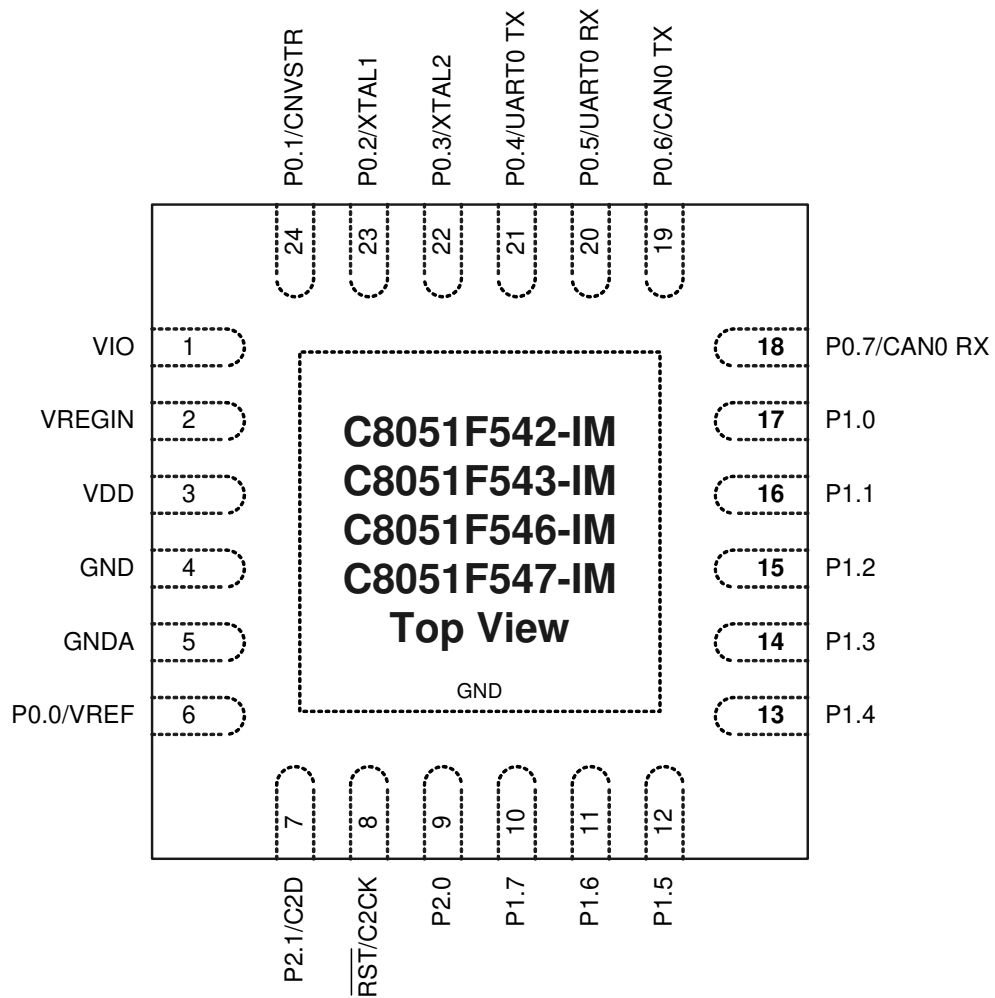


Figure 3.2. QFN-32 Pinout Diagram (Top View)



**Figure 3.3. QFN-24 Pinout Diagram (Top View)**

## 4. Package Specifications

### 4.1. QFP-32 Package Specifications

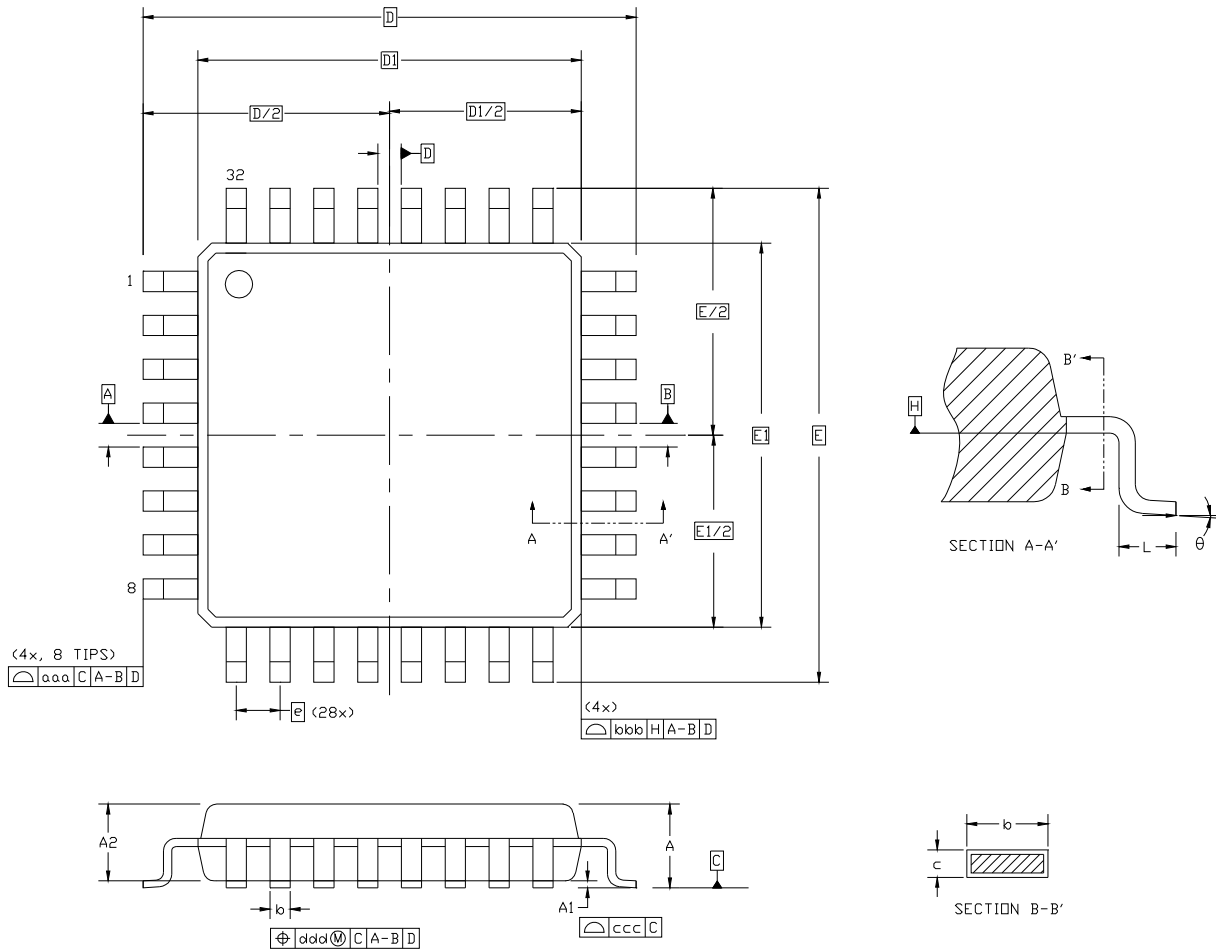


Figure 4.1. QFP-32 Package Drawing

Table 4.1. QFP-32 Package Dimensions

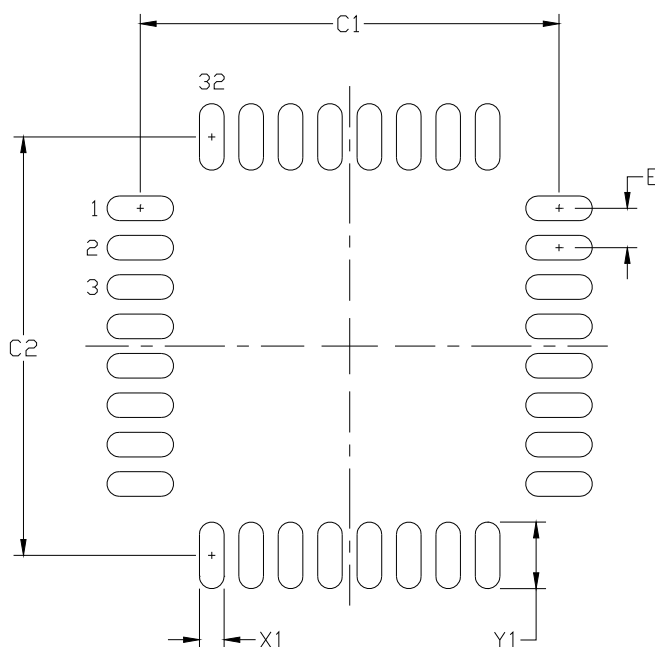
Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	—	—	1.60	E	9.00 BSC.		
A1	0.05	—	0.15	E1	7.00 BSC.		
A2	1.35	1.40	1.45	L	0.45	0.60	0.75
b	0.30	0.37	0.45	aaa	0.20		
c	0.09	—	0.20	bbb	0.20		
D	9.00 BSC.			ccc	0.10		
D1	7.00 BSC.			ddd	0.20		
e	0.80 BSC.			θ	0°	3.5°	7°

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



# C8051F54x



**Figure 4.2. QFP-32 Landing Diagram**

**Table 4.2. QFP-32 Landing Diagram Dimensions**

Dimension	Min	Max	Dimension	Min	Max
C1	8.40	8.50	X1	0.40	0.50
C2	8.40	8.50	Y1	1.25	1.35
E	0.80 BSC				

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

**Solder Mask Design**

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.

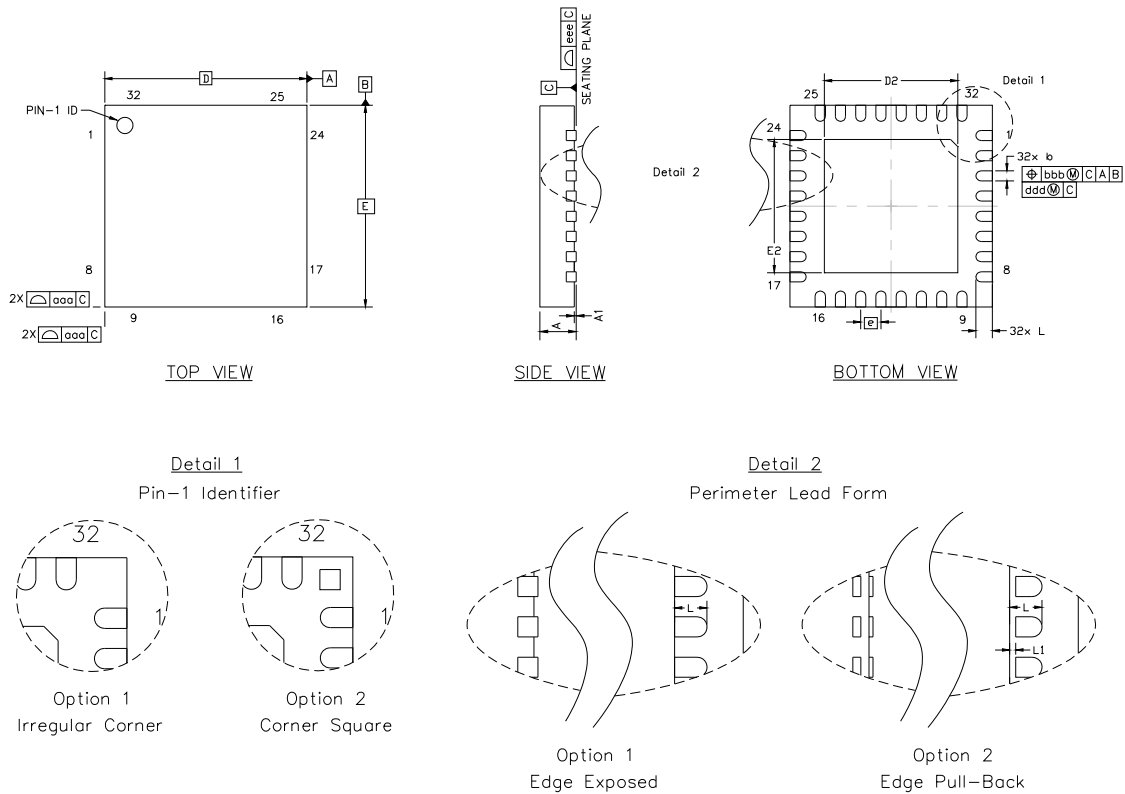
**Stencil Design**

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

**Card Assembly**

7. A No-Clean, Type-3 solder paste is recommended.
8. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 4.2. QFN-32 Package Specifications



**Figure 4.3. QFN-32 Package Drawing**

**Table 4.3. QFN-32 Package Dimensions**

Dimension	Min	Typ	Max
A	0.80	0.9	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	5.00 BSC.		
D2	3.20	3.30	3.40
e	0.50 BSC.		
E	5.00 BSC.		
E2	3.20	3.30	3.40
L	0.30	0.40	0.50
L1	0.00	—	0.15
aaa	—	—	0.15
bbb	—	—	0.15
ddd	—	—	0.05
eee	—	—	0.08

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.