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Capacitance to Digital Converter

- Supports buttons, sliders, wheels, capacitive proximity, and touch screen sensing
- Up to 38 input channels
- Fast 40 μ s per channel conversion time
- 12, 13, 14, or 16-bit output
- Auto-scan and wake-on-touch
- Auto-accumulate 4, 8, 16, 32, or 64 samples

10-Bit Analog to Digital Converter

- Up to 500 ksp/s
- Up to 16 external single-ended inputs
- VREF from on-chip VREF, external pin or V_{DD}
- Internal or external start of conversion source
- Built-in temperature sensor

Analog Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source

On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Low cost, **complete** development kit

Supply Voltage 1.8 to 3.6 V

- Built-in voltage supply monitor

High-Speed 8051 μ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

Memory

- 512 bytes internal data RAM (256 + 256)
- Up to 16 kB Flash; In-system programmable in 512-byte Sectors
- Up to 32-byte data EEPROM

Digital Peripherals

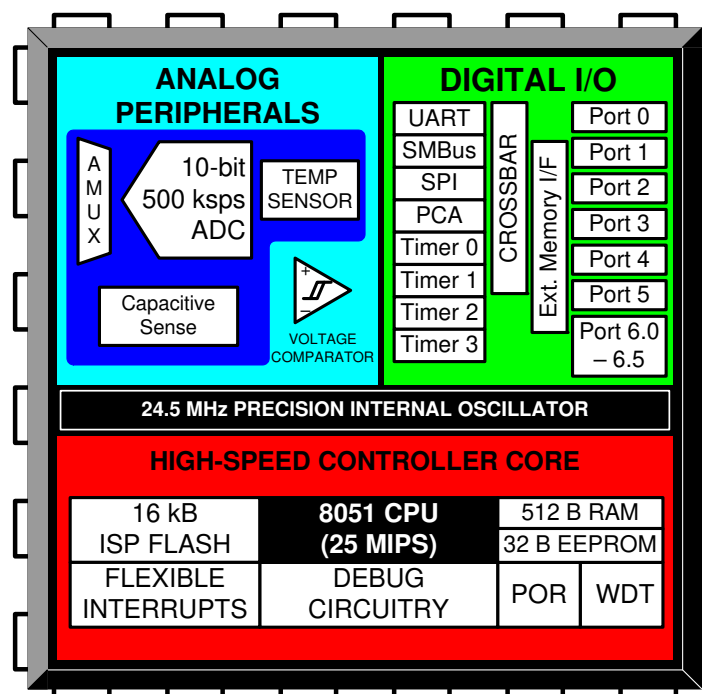
- Up to 54 Port I/O with high sink current
- Hardware enhanced UART, SMBus™ (I²C compatible), and enhanced SPI™ serial ports
- Four general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with 3 capture/compare modules and enhanced PWM functionality
- Real time clock mode using timer and crystal

Clock Sources

- 24.5 MHz \pm 2% Oscillator Supports crystal-less UART operation
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly; useful in power saving modes

64-Pin TQFP, 48-Pin TQFP, 48-Pin QFN, 32-Pin QFN, 24-Pin QFN

Temperature Range: -40 to +85 °C



C8051F70x/71x



Table of Contents

1. System Overview	17
2. Ordering Information	26
3. Pin Definitions	28
4. TQFP-64 Package Specifications	37
5. TQFP-48 Package Specifications	39
6. QFN-48 Package Specifications	41
7. QFN-32 Package Specifications	43
8. QFN-24 Package Specifications	45
9. Electrical Characteristics	47
9.1. Absolute Maximum Specifications	47
9.2. Electrical Characteristics	48
10. 10-Bit ADC (ADC0)	55
10.1. Output Code Formatting	56
10.2. 8-Bit Mode	56
10.3. Modes of Operation	56
10.3.1. Starting a Conversion.....	56
10.3.2. Tracking Modes.....	57
10.3.3. Settling Time Requirements.....	58
10.4. Programmable Window Detector.....	62
10.4.1. Window Detector Example.....	64
10.5. ADC0 Analog Multiplexer	65
11. Temperature Sensor	67
11.1. Calibration	67
12. Voltage and Ground Reference Options	69
12.1. External Voltage References.....	70
12.2. Internal Voltage Reference Options	70
12.3. Analog Ground Reference.....	70
12.4. Temperature Sensor Enable	70
13. Voltage Regulator (REG0)	72
14. Comparator0	74
14.1. Comparator Multiplexer	78
15. Capacitive Sense (CS0)	80
15.1. Configuring Port Pins as Capacitive Sense Inputs	81
15.2. CS0 Gain Adjustment	81
15.3. Capacitive Sense Start-Of-Conversion Sources	81
15.4. Automatic Scanning.....	83
15.5. CS0 Comparator.....	84
15.6. CS0 Conversion Accumulator	85
15.7. CS0 Pin Monitor	86
15.8. Adjusting CS0 For Special Situations.....	87
15.9. Capacitive Sense Multiplexer	96
16. CIP-51 Microcontroller	98
16.1. Instruction Set.....	99

C8051F70x/71x

16.1.1. Instruction and CPU Timing	99
16.2. CIP-51 Register Descriptions	104
17. Memory Organization	108
17.1. Program Memory	109
17.1.1. MOVX Instruction and Program Memory	109
17.2. EEPROM Memory	109
17.3. Data Memory	109
17.3.1. Internal RAM	109
17.3.1.1. General Purpose Registers	110
17.3.1.2. Bit Addressable Locations	110
17.3.1.3. Stack	110
18. External Data Memory Interface and On-Chip XRAM	111
18.1. Accessing XRAM	111
18.1.1. 16-Bit MOVX Example	111
18.1.2. 8-Bit MOVX Example	111
18.2. Configuring the External Memory Interface	112
18.3. Port Configuration	112
18.4. Multiplexed and Non-multiplexed Selection	115
18.4.1. Multiplexed Configuration	115
18.4.2. Non-multiplexed Configuration	116
18.5. Memory Mode Selection	117
18.5.1. Internal XRAM Only	117
18.5.2. Split Mode without Bank Select	117
18.5.3. Split Mode with Bank Select	118
18.5.4. External Only	118
18.6. Timing	118
18.6.1. Non-Multiplexed Mode	120
18.6.1.1. 16-bit MOVX: EMIOCF[4:2] = 101, 110, or 111	120
18.6.1.2. 8-bit MOVX without Bank Select: EMIOCF[4:2] = 101 or 111	121
18.6.1.3. 8-bit MOVX with Bank Select: EMIOCF[4:2] = 110	122
18.6.2. Multiplexed Mode	123
18.6.2.1. 16-bit MOVX: EMIOCF[4:2] = 001, 010, or 011	123
18.6.2.2. 8-bit MOVX without Bank Select: EMIOCF[4:2] = 001 or 011	124
18.6.2.3. 8-bit MOVX with Bank Select: EMIOCF[4:2] = 010	125
19. In-System Device Identification	128
20. Special Function Registers	130
21. Interrupts	137
21.1. MCU Interrupt Sources and Vectors	138
21.1.1. Interrupt Priorities	138
21.1.2. Interrupt Latency	138
21.2. Interrupt Register Descriptions	140
21.3. INT0 and INT1 External Interrupts	146
22. Flash Memory	148
22.1. Programming The Flash Memory	148
22.1.1. Flash Lock and Key Functions	148

22.1.2. Flash Erase Procedure	148
22.1.3. Flash Write Procedure	149
22.2. Non-volatile Data Storage	149
22.3. Security Options	149
22.4. Flash Write and Erase Guidelines	150
22.4.1. VDD Maintenance and the VDD Monitor	151
22.4.2. PSWE Maintenance	151
22.4.3. System Clock	152
23. EEPROM	155
23.1. RAM Reads and Writes	155
23.2. Auto Increment	155
23.3. Interfacing with the EEPROM	155
23.4. EEPROM Security	156
24. Power Management Modes	160
24.1. Idle Mode	160
24.2. Stop Mode	161
24.3. Suspend Mode	161
25. Reset Sources	163
25.1. Power-On Reset	164
25.2. Power-Fail Reset / VDD Monitor	165
25.3. External Reset	166
25.4. Missing Clock Detector Reset	166
25.5. Comparator0 Reset	167
25.6. Watchdog Timer Reset	167
25.7. Flash Error Reset	167
25.8. Software Reset	167
26. Watchdog Timer	169
26.1. Enable/Reset WDT	169
26.2. Disable WDT	169
26.3. Disable WDT Lockout	169
26.4. Setting WDT Interval	169
27. Oscillators and Clock Selection	171
27.1. System Clock Selection	171
27.2. Programmable Internal High-Frequency (H-F) Oscillator	173
27.3. External Oscillator Drive Circuit	175
27.3.1. External Crystal Example	177
27.3.2. External RC Example	178
27.3.3. External Capacitor Example	179
28. Port Input/Output	180
28.1. Port I/O Modes of Operation	181
28.1.1. Port Pins Configured for Analog I/O	181
28.1.2. Port Pins Configured For Digital I/O	181
28.1.3. Interfacing Port I/O to 5 V Logic	182
28.1.4. Increasing Port I/O Drive Strength	182
28.2. Assigning Port I/O Pins to Analog and Digital Functions	182

C8051F70x/71x

28.2.1. Assigning Port I/O Pins to Analog Functions	182
28.2.2. Assigning Port I/O Pins to Digital Functions.....	184
28.2.3. Assigning Port I/O Pins to External Event Trigger Functions.....	184
28.3. Priority Crossbar Decoder	185
28.4. Port I/O Initialization	189
28.5. Port Match	192
28.6. Special Function Registers for Accessing and Configuring Port I/O	194
29. Cyclic Redundancy Check Unit (CRC0).....	211
29.1. 16-bit CRC Algorithm.....	212
29.2. 32-bit CRC Algorithm.....	213
29.3. Preparing for a CRC Calculation	214
29.4. Performing a CRC Calculation	214
29.5. Accessing the CRC0 Result	214
29.6. CRC0 Bit Reverse Feature.....	218
30. SMBus.....	219
30.1. Supporting Documents	220
30.2. SMBus Configuration.....	220
30.3. SMBus Operation	220
30.3.1. Transmitter Vs. Receiver.....	221
30.3.2. Arbitration.....	221
30.3.3. Clock Low Extension.....	221
30.3.4. SCL Low Timeout.....	221
30.3.5. SCL High (SMBus Free) Timeout	222
30.4. Using the SMBus.....	222
30.4.1. SMBus Configuration Register.....	222
30.4.2. SMB0CN Control Register	226
30.4.2.1. Software ACK Generation	226
30.4.2.2. Hardware ACK Generation	226
30.4.3. Hardware Slave Address Recognition	228
30.4.4. Data Register	231
30.5. SMBus Transfer Modes.....	232
30.5.1. Write Sequence (Master)	232
30.5.2. Read Sequence (Master).....	233
30.5.3. Write Sequence (Slave)	234
30.5.4. Read Sequence (Slave).....	235
30.6. SMBus Status Decoding.....	235
31. Enhanced Serial Peripheral Interface (SPI0)	241
31.1. Signal Descriptions.....	242
31.1.1. Master Out, Slave In (MOSI).....	242
31.1.2. Master In, Slave Out (MISO).....	242
31.1.3. Serial Clock (SCK)	242
31.1.4. Slave Select (NSS)	242
31.2. SPI0 Master Mode Operation	242
31.3. SPI0 Slave Mode Operation.....	244
31.4. SPI0 Interrupt Sources	245

31.5. Serial Clock Phase and Polarity	245
31.6. SPI Special Function Registers	247
32. UART0	254
32.1. Enhanced Baud Rate Generation.....	255
32.2. Operational Modes	256
32.2.1. 8-Bit UART	256
32.2.2. 9-Bit UART	257
32.3. Multiprocessor Communications	258
33. Timers	262
33.1. Timer 0 and Timer 1	264
33.1.1. Mode 0: 13-bit Counter/Timer	264
33.1.2. Mode 1: 16-bit Counter/Timer	265
33.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload.....	265
33.1.4. Mode 3: Two 8-bit Counter/Timers (Timer 0 Only).....	266
33.2. Timer 2	272
33.2.1. 16-bit Timer with Auto-Reload.....	272
33.2.2. 8-bit Timers with Auto-Reload.....	273
33.3. Timer 3	278
33.3.1. 16-bit Timer with Auto-Reload.....	278
33.3.2. 8-bit Timers with Auto-Reload.....	279
34. Programmable Counter Array.....	284
34.1. PCA Counter/Timer	285
34.2. PCA0 Interrupt Sources.....	286
34.3. Capture/Compare Modules	286
34.3.1. Edge-triggered Capture Mode.....	288
34.3.2. Software Timer (Compare) Mode.....	289
34.3.3. High-Speed Output Mode	290
34.3.4. Frequency Output Mode	291
34.3.5. 8-bit, 9-bit, 10-bit and 11-bit Pulse Width Modulator Modes	292
34.3.5.1. 8-bit Pulse Width Modulator Mode.....	292
34.3.5.2. 9/10/11-bit Pulse Width Modulator Mode.....	293
34.3.6. 16-Bit Pulse Width Modulator Mode.....	294
34.4. Register Descriptions for PCA0.....	295
35. C2 Interface	301
35.1. C2 Interface Registers.....	301
35.2. C2CK Pin Sharing	304
Document Change List.....	305
Contact Information.....	306

List of Figures

Figure 1.1. C8051F700/1 Block Diagram	18
Figure 1.2. C8051F702/3 Block Diagram	19
Figure 1.3. C8051F704/5 Block Diagram	20
Figure 1.4. C8051F706/07 Block Diagram	21
Figure 1.5. C8051F708/09/10/11 Block Diagram	22
Figure 1.6. C8051F712/13/14/15 Block Diagram	23
Figure 1.7. C8051F716 Block Diagram	24
Figure 1.8. C8051F717 Block Diagram	25
Figure 3.1. C8051F7xx-GQ TQFP64 Pinout Diagram (Top View)	32
Figure 3.2. C8051F7xx-GQ QFP48 Pinout Diagram (Top View)	33
Figure 3.3. C8051F7xx-GM QFN48 Pinout Diagram (Top View)	34
Figure 3.4. C8051F716-GM QFN32 Pinout Diagram (Top View)	35
Figure 3.5. C8051F717-GM QFN24 Pinout Diagram (Top View)	36
Figure 4.1. TQFP-64 Package Drawing	37
Figure 4.2. TQFP-64 PCB Land Pattern	38
Figure 5.1. TQFP-48 Package Drawing	39
Figure 5.2. TQFP-48 PCB Land Pattern	40
Figure 6.1. QFN-48 Package Drawing	41
Figure 6.2. QFN-48 PCB Land Pattern	42
Figure 7.1. QFN-32 Package Drawing	43
Figure 7.2. QFN-32 Recommended PCB Land Pattern	44
Figure 8.1. QFN-24 Package Drawing	45
Figure 8.2. QFN-24 Recommended PCB Land Pattern	46
Figure 10.1. ADC0 Functional Block Diagram	55
Figure 10.2. 10-Bit ADC Track and Conversion Example Timing	57
Figure 10.3. ADC0 Equivalent Input Circuits	58
Figure 10.4. ADC Window Compare Example: Right-Justified Data	64
Figure 10.5. ADC Window Compare Example: Left-Justified Data	64
Figure 10.6. ADC0 Multiplexer Block Diagram	65
Figure 11.1. Temperature Sensor Transfer Function	67
Figure 11.2. Temperature Sensor Error with 1-Point Calibration at 0 Celsius	68
Figure 12.1. Voltage Reference Functional Block Diagram	69
Figure 14.1. Comparator0 Functional Block Diagram	74
Figure 14.2. Comparator Hysteresis Plot	75
Figure 14.3. Comparator Input Multiplexer Block Diagram	78
Figure 15.1. CS0 Block Diagram	80
Figure 15.2. Auto-Scan Example	83
Figure 15.3. CS0 Multiplexer Block Diagram	96
Figure 16.1. CIP-51 Block Diagram	98
Figure 17.1. C8051F70x/71x Memory Map	108
Figure 17.2. Flash Program Memory Map	109
Figure 18.1. Multiplexed Configuration Example	115
Figure 18.2. Non-multiplexed Configuration Example	116

C8051F70x/71x

Figure 18.3. EMIF Operating Modes	117
Figure 18.4. Non-multiplexed 16-bit MOVX Timing	120
Figure 18.5. Non-multiplexed 8-bit MOVX without Bank Select Timing	121
Figure 18.6. Non-Multiplexed 8-Bit MOVX with Bank Select Timing	122
Figure 18.7. Multiplexed 16-bit MOVX Timing	123
Figure 18.8. Multiplexed 8-Bit MOVX without Bank Select Timing	124
Figure 18.9. Multiplexed 8-Bit MOVX with Bank Select Timing	125
Figure 23.1. EEPROM Block Diagram	155
Figure 25.1. Reset Sources	163
Figure 25.2. Power-On and VDD Monitor Reset Timing	164
Figure 27.1. Oscillator Options	171
Figure 27.2. External 32.768 kHz Quartz Crystal Oscillator Connection Diagram	178
Figure 28.1. Port I/O Functional Block Diagram	180
Figure 28.2. Port I/O Cell Block Diagram	181
Figure 28.3. Port I/O Overdrive Current	182
Figure 28.4. Crossbar Priority Decoder—Possible Pin Assignments	186
Figure 28.5. Crossbar Priority Decoder in Example Configuration— No Pins Skipped	187
Figure 28.6. Crossbar Priority Decoder in Example Configuration— 3 Pins Skipped	188
Figure 29.1. CRC0 Block Diagram	211
Figure 30.1. SMBus Block Diagram	219
Figure 30.2. Typical SMBus Configuration	220
Figure 30.3. SMBus Transaction	221
Figure 30.4. Typical SMBus SCL Generation	223
Figure 30.5. Typical Master Write Sequence	232
Figure 30.6. Typical Master Read Sequence	233
Figure 30.7. Typical Slave Write Sequence	234
Figure 30.8. Typical Slave Read Sequence	235
Figure 31.1. SPI Block Diagram	241
Figure 31.2. Multiple-Master Mode Connection Diagram	243
Figure 31.3. 3-Wire Single Master and Single Slave Mode Connection Diagram	243
Figure 31.4. 4-Wire Single Master Mode and Slave Mode Connection Diagram	244
Figure 31.5. Master Mode Data/Clock Timing	246
Figure 31.6. Slave Mode Data/Clock Timing (CKPHA = 0)	246
Figure 31.7. Slave Mode Data/Clock Timing (CKPHA = 1)	247
Figure 31.8. SPI Master Timing (CKPHA = 0)	251
Figure 31.9. SPI Master Timing (CKPHA = 1)	251
Figure 31.10. SPI Slave Timing (CKPHA = 0)	252
Figure 31.11. SPI Slave Timing (CKPHA = 1)	252
Figure 32.1. UART0 Block Diagram	254
Figure 32.2. UART0 Baud Rate Logic	255
Figure 32.3. UART Interconnect Diagram	256
Figure 32.4. 8-Bit UART Timing Diagram	256
Figure 32.5. 9-Bit UART Timing Diagram	257

Figure 32.6. UART Multi-Processor Mode Interconnect Diagram	258
Figure 33.1. T0 Mode 0 Block Diagram	265
Figure 33.2. T0 Mode 2 Block Diagram	266
Figure 33.3. T0 Mode 3 Block Diagram	267
Figure 33.4. Timer 2 16-Bit Mode Block Diagram	272
Figure 33.5. Timer 2 8-Bit Mode Block Diagram	273
Figure 33.7. Timer 3 16-Bit Mode Block Diagram	278
Figure 33.8. Timer 3 8-Bit Mode Block Diagram	279
Figure 33.9. Timer 3 Capture Mode Block Diagram	280
Figure 34.1. PCA Block Diagram	284
Figure 34.2. PCA Counter/Timer Block Diagram	285
Figure 34.3. PCA Interrupt Block Diagram	286
Figure 34.4. PCA Capture Mode Diagram	288
Figure 34.5. PCA Software Timer Mode Diagram	289
Figure 34.6. PCA High-Speed Output Mode Diagram	290
Figure 34.7. PCA Frequency Output Mode	291
Figure 34.8. PCA 8-Bit PWM Mode Diagram	292
Figure 34.9. PCA 9, 10 and 11-Bit PWM Mode Diagram	293
Figure 34.10. PCA 16-Bit PWM Mode	294
Figure 35.1. Typical C2CK Pin Sharing	304

List of Tables

Table 2.1. Product Selection Guide	27
Table 3.1. Pin Definitions for the C8051F70x/71x	28
Table 4.1. TQFP-64 Package Dimensions	37
Table 4.2. TQFP-64 PCB Land Pattern Dimensions	38
Table 5.1. TQFP-48 Package Dimensions	39
Table 5.2. TQFP-48 PCB Land Pattern Dimensions	40
Table 6.1. QFN-48 Package Dimensions	41
Table 6.2. QFN-48 PCB Land Pattern Dimensions	42
Table 7.1. QFN-32 Package Dimensions	43
Table 7.2. QFN-32 PCB Land Pattern Dimensions	44
Table 8.1. QFN-24 Package Dimensions	45
Table 8.2. QFN-24 PCB Land Pattern Dimensions	46
Table 9.1. Absolute Maximum Ratings	47
Table 9.2. Global Electrical Characteristics	48
Table 9.3. Port I/O DC Electrical Characteristics	49
Table 9.4. Reset Electrical Characteristics	49
Table 9.5. Internal Voltage Regulator Electrical Characteristics	50
Table 9.6. Flash Electrical Characteristics	50
Table 9.7. Internal High-Frequency Oscillator Electrical Characteristics	50
Table 9.8. Capacitive Sense Electrical Characteristics	51
Table 9.9. EEPROM Electrical Characteristics	52
Table 9.10. ADC0 Electrical Characteristics	52
Table 9.11. Power Management Electrical Characteristics	53
Table 9.12. Temperature Sensor Electrical Characteristics	53
Table 9.13. Voltage Reference Electrical Characteristics	53
Table 9.14. Comparator Electrical Characteristics	54
Table 15.1. Gain Setting vs. Maximum Capacitance and Conversion Time	81
Table 15.2. Operation with Auto-scan and Accumulate	85
Table 16.1. CIP-51 Instruction Set Summary	100
Table 18.1. AC Parameters for External Memory Interface	126
Table 18.2. EMIF Pinout (C8051F700/1/2/3/8/9 and C8051F710/1)	127
Table 20.1. Special Function Register (SFR) Memory Map	131
Table 20.2. Special Function Registers	132
Table 21.1. Interrupt Summary	139
Table 22.1. Flash Security Summary	150
Table 28.1. Port I/O Assignment for Analog Functions	183
Table 28.2. Port I/O Assignment for Digital Functions	184
Table 28.3. Port I/O Assignment for External Event Trigger Functions	184
Table 29.1. Example 16-bit CRC Outputs	212
Table 29.2. Example 32-bit CRC Outputs	213
Table 30.1. SMBus Clock Source Selection	223
Table 30.2. Minimum SDA Setup and Hold Times	224
Table 30.3. Sources for Hardware Changes to SMB0CN	228

C8051F70x/71x

Table 30.4. Hardware Address Recognition Examples (EHACK = 1)	229
Table 30.5. SMBus Status Decoding: Hardware ACK Disabled (EHACK = 0)	236
Table 30.6. SMBus Status Decoding: Hardware ACK Enabled (EHACK = 1)	238
Table 31.1. SPI Slave Timing Parameters	253
Table 32.1. Timer Settings for Standard Baud Rates Using The Internal 24.5 MHz Oscillator	261
Table 32.2. Timer Settings for Standard Baud Rates Using an External 22.1184 MHz Oscillator	261
Table 34.1. PCA Timebase Input Options	285
Table 34.2. PCA0CPM and PCA0PWM Bit Settings for PCA Modules	287

List of Registers

SFR Definition 10.1. ADC0CF: ADC0 Configuration	59
SFR Definition 10.2. ADC0H: ADC0 Data Word MSB	60
SFR Definition 10.3. ADC0L: ADC0 Data Word LSB	60
SFR Definition 10.4. ADC0CN: ADC0 Control	61
SFR Definition 10.5. ADC0GTH: ADC0 Greater-Than Data High Byte	62
SFR Definition 10.6. ADC0GTL: ADC0 Greater-Than Data Low Byte	62
SFR Definition 10.7. ADC0LTH: ADC0 Less-Than Data High Byte	63
SFR Definition 10.8. ADC0LTL: ADC0 Less-Than Data Low Byte	63
SFR Definition 10.9. ADC0MX: AMUX0 Channel Select	66
SFR Definition 12.1. REF0CN: Voltage Reference Control	71
SFR Definition 13.1. REG0CN: Voltage Regulator Control	73
SFR Definition 14.1. CPT0CN: Comparator0 Control	76
SFR Definition 14.2. CPT0MD: Comparator0 Mode Selection	77
SFR Definition 14.3. CPT0MX: Comparator0 MUX Selection	79
SFR Definition 15.1. CS0CN: Capacitive Sense Control	88
SFR Definition 15.2. CS0CF: Capacitive Sense Configuration	89
SFR Definition 15.3. CS0DH: Capacitive Sense Data High Byte	90
SFR Definition 15.4. CS0DL: Capacitive Sense Data Low Byte	90
SFR Definition 15.5. CS0SS: Capacitive Sense Auto-Scan Start Channel	91
SFR Definition 15.6. CS0SE: Capacitive Sense Auto-Scan End Channel	91
SFR Definition 15.7. CS0THH: Capacitive Sense Comparator Threshold High Byte ...	92
SFR Definition 15.8. CS0THL: Capacitive Sense Comparator Threshold Low Byte	92
SFR Definition 15.9. CS0PM: Capacitive Sense Pin Monitor	93
SFR Definition 15.10. CS0MD1: Capacitive Sense Mode 1	94
SFR Definition 15.11. CS0MD2: Capacitive Sense Mode 2	95
SFR Definition 15.12. CS0MX: Capacitive Sense Mux Channel Select	97
SFR Definition 16.1. DPL: Data Pointer Low Byte	104
SFR Definition 16.2. DPH: Data Pointer High Byte	104
SFR Definition 16.3. SP: Stack Pointer	105
SFR Definition 16.4. ACC: Accumulator	105
SFR Definition 16.5. B: B Register	106
SFR Definition 16.6. PSW: Program Status Word	107
SFR Definition 18.1. EMI0CN: External Memory Interface Control	113
SFR Definition 18.2. EMI0CF: External Memory Configuration	114
SFR Definition 18.3. EMI0TC: External Memory Timing Control	119
SFR Definition 19.1. HWID: Hardware Identification Byte	128
SFR Definition 19.2. DERIVID: Derivative Identification Byte	128
SFR Definition 19.3. REVID: Hardware Revision Identification Byte	129
SFR Definition 20.1. SFRPAGE: SFR Page	132
SFR Definition 21.1. IE: Interrupt Enable	140
SFR Definition 21.2. IP: Interrupt Priority	141
SFR Definition 21.3. EIE1: Extended Interrupt Enable 1	142
SFR Definition 21.4. EIE2: Extended Interrupt Enable 2	143

C8051F70x/71x

SFR Definition 21.5. EIP1: Extended Interrupt Priority 1	144
SFR Definition 21.6. EIP2: Extended Interrupt Priority 2	145
SFR Definition 21.7. IT01CF: INT0/INT1 Configuration	147
SFR Definition 22.1. PSCTL: Program Store R/W Control	153
SFR Definition 22.2. FLKEY: Flash Lock and Key	154
SFR Definition 23.1. EEADDR: EEPROM Byte Address	156
SFR Definition 23.2. EEDATA: EEPROM Byte Data	157
SFR Definition 23.3. EECNTL: EEPROM Control	158
SFR Definition 23.4. EEKEY: EEPROM Protect Key	159
SFR Definition 24.1. PCON: Power Control	162
SFR Definition 25.1. VDM0CN: VDD Monitor Control	166
SFR Definition 25.2. RSTSRC: Reset Source	168
SFR Definition 26.1. WDTCN: Watchdog Timer Control	170
SFR Definition 27.1. CLKSEL: Clock Select	172
SFR Definition 27.2. OSCICL: Internal H-F Oscillator Calibration	173
SFR Definition 27.3. OSCICN: Internal H-F Oscillator Control	174
SFR Definition 27.4. OSCXCN: External Oscillator Control	176
SFR Definition 28.1. XBR0: Port I/O Crossbar Register 0	190
SFR Definition 28.2. XBR1: Port I/O Crossbar Register 1	191
SFR Definition 28.3. P0MASK: Port 0 Mask Register	192
SFR Definition 28.4. P0MAT: Port 0 Match Register	193
SFR Definition 28.5. P1MASK: Port 1 Mask Register	193
SFR Definition 28.6. P1MAT: Port 1 Match Register	194
SFR Definition 28.7. P0: Port 0	195
SFR Definition 28.8. P0MDIN: Port 0 Input Mode	195
SFR Definition 28.9. P0MDOUT: Port 0 Output Mode	196
SFR Definition 28.10. P0SKIP: Port 0 Skip	196
SFR Definition 28.11. P0DRV: Port 0 Drive Strength	197
SFR Definition 28.12. P1: Port 1	197
SFR Definition 28.13. P1MDIN: Port 1 Input Mode	198
SFR Definition 28.14. P1MDOUT: Port 1 Output Mode	198
SFR Definition 28.15. P1SKIP: Port 1 Skip	199
SFR Definition 28.16. P1DRV: Port 1 Drive Strength	199
SFR Definition 28.17. P2: Port 2	200
SFR Definition 28.18. P2MDIN: Port 2 Input Mode	200
SFR Definition 28.19. P2MDOUT: Port 2 Output Mode	201
SFR Definition 28.20. P2SKIP: Port 2 Skip	201
SFR Definition 28.21. P2DRV: Port 2 Drive Strength	202
SFR Definition 28.22. P3: Port 3	202
SFR Definition 28.23. P3MDIN: Port 3 Input Mode	203
SFR Definition 28.24. P3MDOUT: Port 3 Output Mode	203
SFR Definition 28.25. P3DRV: Port 3 Drive Strength	204
SFR Definition 28.26. P4: Port 4	204
SFR Definition 28.27. P4MDIN: Port 4 Input Mode	205
SFR Definition 28.28. P4MDOUT: Port 4 Output Mode	205

SFR Definition 28.29. P4DRV: Port 4 Drive Strength	206
SFR Definition 28.30. P5: Port 5	206
SFR Definition 28.31. P5MDIN: Port 5 Input Mode	207
SFR Definition 28.32. P5MDOUT: Port 5 Output Mode	207
SFR Definition 28.33. P5DRV: Port 5 Drive Strength	208
SFR Definition 28.34. P6: Port 6	208
SFR Definition 28.35. P6MDIN: Port 6 Input Mode	209
SFR Definition 28.36. P6MDOUT: Port 6 Output Mode	209
SFR Definition 28.37. P6DRV: Port 6 Drive Strength	210
SFR Definition 29.1. CRC0CN: CRC0 Control	215
SFR Definition 29.2. CRC0IN: CRC Data Input	216
SFR Definition 29.3. CRC0DATA: CRC Data Output	216
SFR Definition 29.4. CRC0AUTO: CRC Automatic Control	217
SFR Definition 29.5. CRC0CNT: CRC Automatic Flash Sector Count	217
SFR Definition 29.6. CRC0FLIP: CRC Bit Flip	218
SFR Definition 30.1. SMB0CF: SMBus Clock/Configuration	225
SFR Definition 30.2. SMB0CN: SMBus Control	227
SFR Definition 30.3. SMB0ADR: SMBus Slave Address	229
SFR Definition 30.4. SMB0ADM: SMBus Slave Address Mask	230
SFR Definition 30.5. SMB0DAT: SMBus Data	231
SFR Definition 31.1. SPI0CFG: SPI0 Configuration	248
SFR Definition 31.2. SPI0CN: SPI0 Control	249
SFR Definition 31.3. SPI0CKR: SPI0 Clock Rate	250
SFR Definition 31.4. SPI0DAT: SPI0 Data	250
SFR Definition 32.1. SCON0: Serial Port 0 Control	259
SFR Definition 32.2. SBUF0: Serial (UART0) Port Data Buffer	260
SFR Definition 33.1. CKCON: Clock Control	263
SFR Definition 33.2. TCON: Timer Control	268
SFR Definition 33.3. TMOD: Timer Mode	269
SFR Definition 33.4. TL0: Timer 0 Low Byte	270
SFR Definition 33.5. TL1: Timer 1 Low Byte	270
SFR Definition 33.6. TH0: Timer 0 High Byte	271
SFR Definition 33.7. TH1: Timer 1 High Byte	271
SFR Definition 33.8. TMR2CN: Timer 2 Control	275
SFR Definition 33.9. TMR2RLL: Timer 2 Reload Register Low Byte	276
SFR Definition 33.10. TMR2RLH: Timer 2 Reload Register High Byte	276
SFR Definition 33.11. TMR2L: Timer 2 Low Byte	277
SFR Definition 33.12. TMR2H: Timer 2 High Byte	277
SFR Definition 33.13. TMR3CN: Timer 3 Control	281
SFR Definition 33.14. TMR3RLL: Timer 3 Reload Register Low Byte	282
SFR Definition 33.15. TMR3RLH: Timer 3 Reload Register High Byte	282
SFR Definition 33.16. TMR3L: Timer 3 Low Byte	283
SFR Definition 33.17. TMR3H: Timer 3 High Byte	283
SFR Definition 34.1. PCA0CN: PCA Control	295
SFR Definition 34.2. PCA0MD: PCA Mode	296

C8051F70x/71x

SFR Definition 34.3. PCA0PWM: PCA PWM Configuration	297
SFR Definition 34.4. PCA0CPMn: PCA Capture/Compare Mode	298
SFR Definition 34.5. PCA0L: PCA Counter/Timer Low Byte	299
SFR Definition 34.6. PCA0H: PCA Counter/Timer High Byte	299
SFR Definition 34.7. PCA0CPLn: PCA Capture Module Low Byte	300
SFR Definition 34.8. PCA0CPHn: PCA Capture Module High Byte	300
C2 Register Definition 35.1. C2ADD: C2 Address	301
C2 Register Definition 35.2. DEVICEID: C2 Device ID	302
C2 Register Definition 35.3. REVID: C2 Revision ID	302
C2 Register Definition 35.4. FPCTL: C2 Flash Programming Control	303
C2 Register Definition 35.5. FPDAT: C2 Flash Programming Data	303

1. System Overview

C8051F70x/71x devices are fully integrated, system-on-a-chip, capacitive sensing mixed-signal MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- Capacitive Sense interface with 38 input channels
- 10-bit 500 ksp/s single-ended ADC with 16 external channels and integrated temperature sensor
- Precision calibrated 24.5 MHz internal oscillator
- 16 kB of on-chip Flash memory
- 512 bytes of on-chip RAM
- SMBus/I²C, Enhanced UART, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with three capture/compare modules
- On-chip internal voltage reference
- On-chip Watchdog timer
- On-chip Power-On Reset and Supply Monitor
- On-chip Voltage Comparator
- 54 general purpose I/O

With on-chip power-on reset, V_{DD} monitor, watchdog timer, and clock oscillator, the C8051F70x/71x devices are truly stand-alone, system-on-a-chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The C8051F70x/71x processors include Silicon Laboratories' 2-Wire C2 Debug and Programming interface, which allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection of memory, viewing and modification of special function registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 1.8–3.6 V operation over the industrial temperature range (-45 to $+85$ °C). An internal LDO is used to supply the processor core voltage at 1.8 V. The Port I/O and \overline{RST} pins are tolerant of input signals up to 2 V above the V_{DD} supply, with the exception of P0.3. See Table 2.1 for ordering information. Block diagrams of the devices in the C8051F70x/71x family are shown in Figure 1.1.

C8051F70x/71x

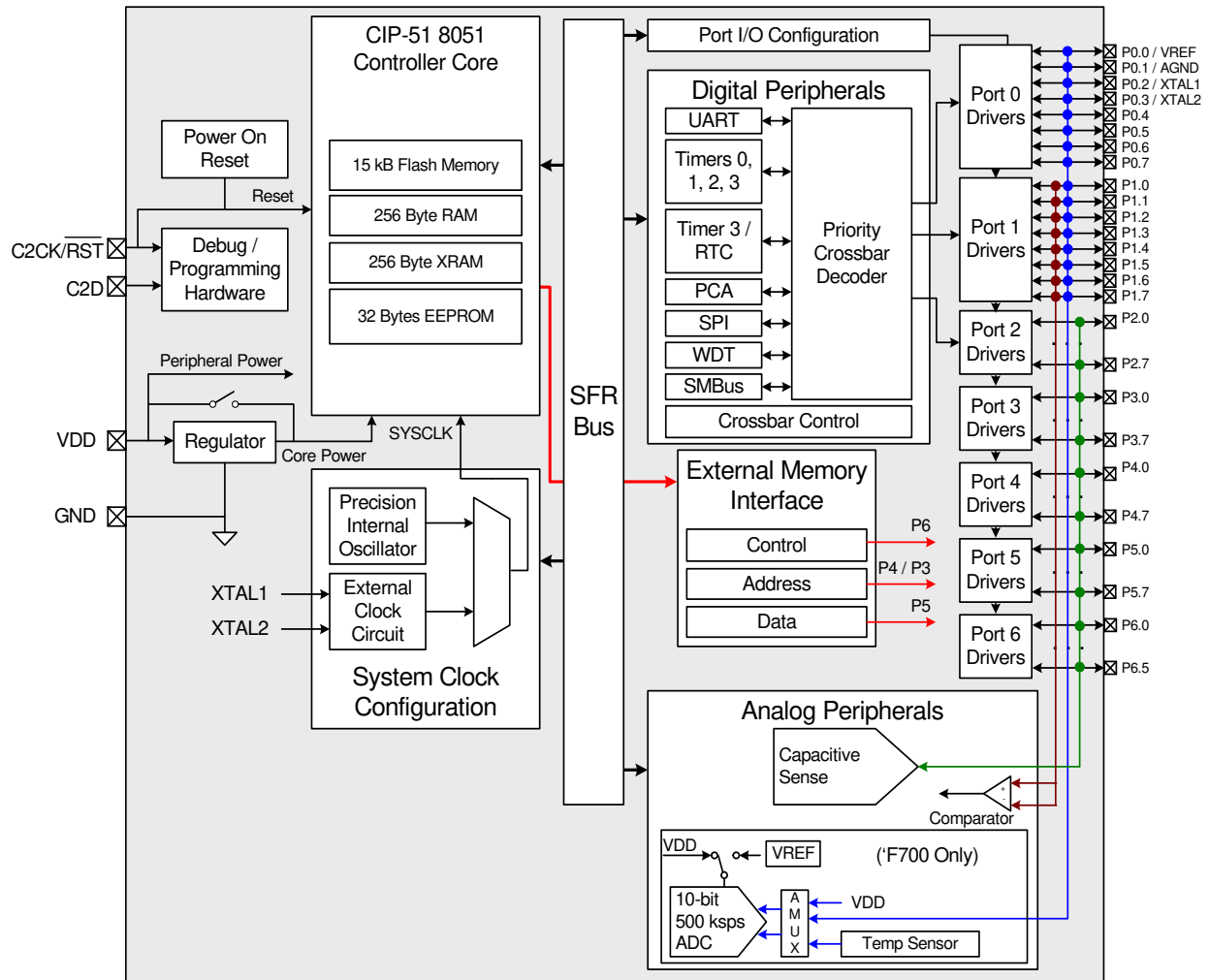


Figure 1.1. C8051F700/1 Block Diagram

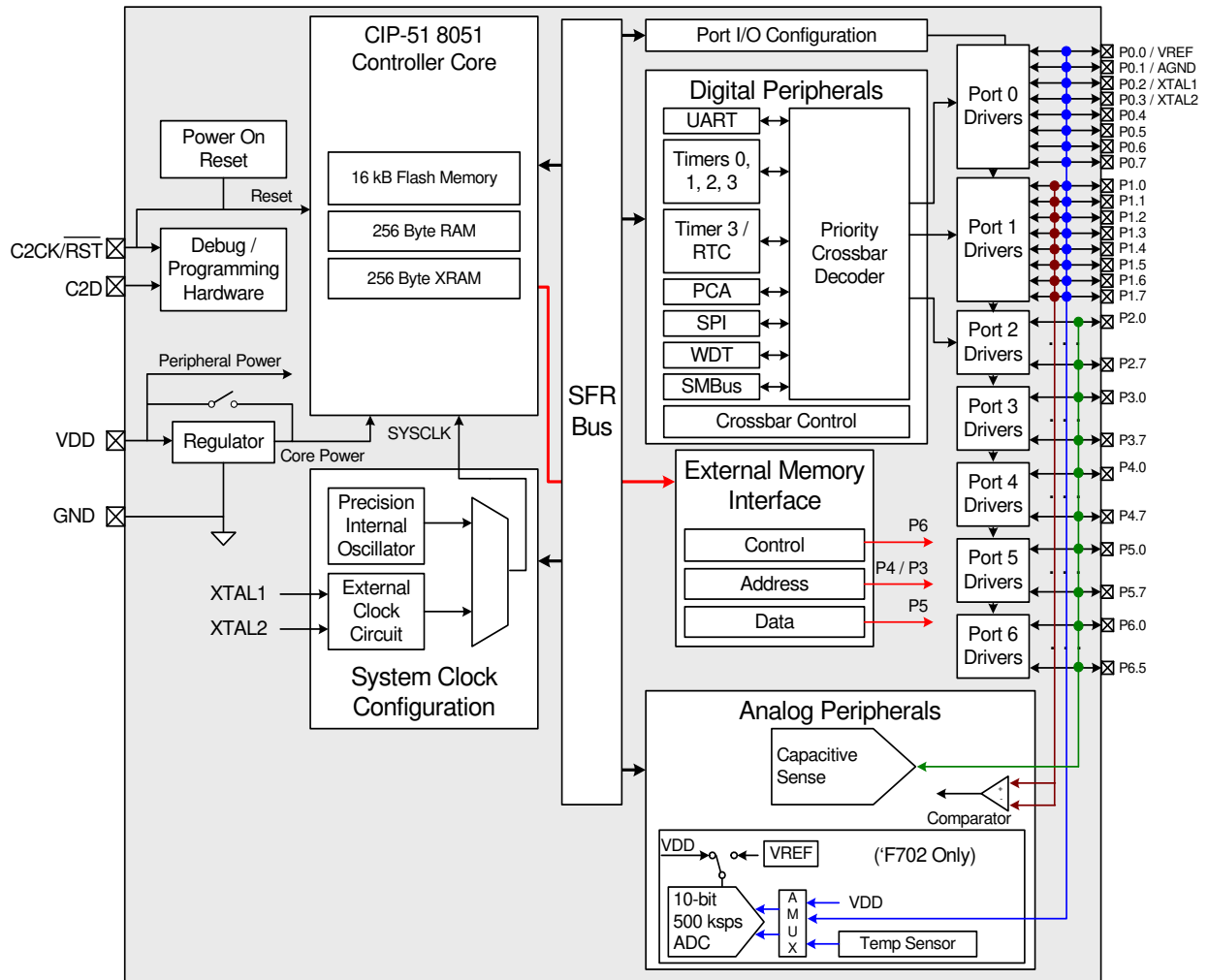


Figure 1.2. C8051F702/3 Block Diagram

C8051F70x/71x

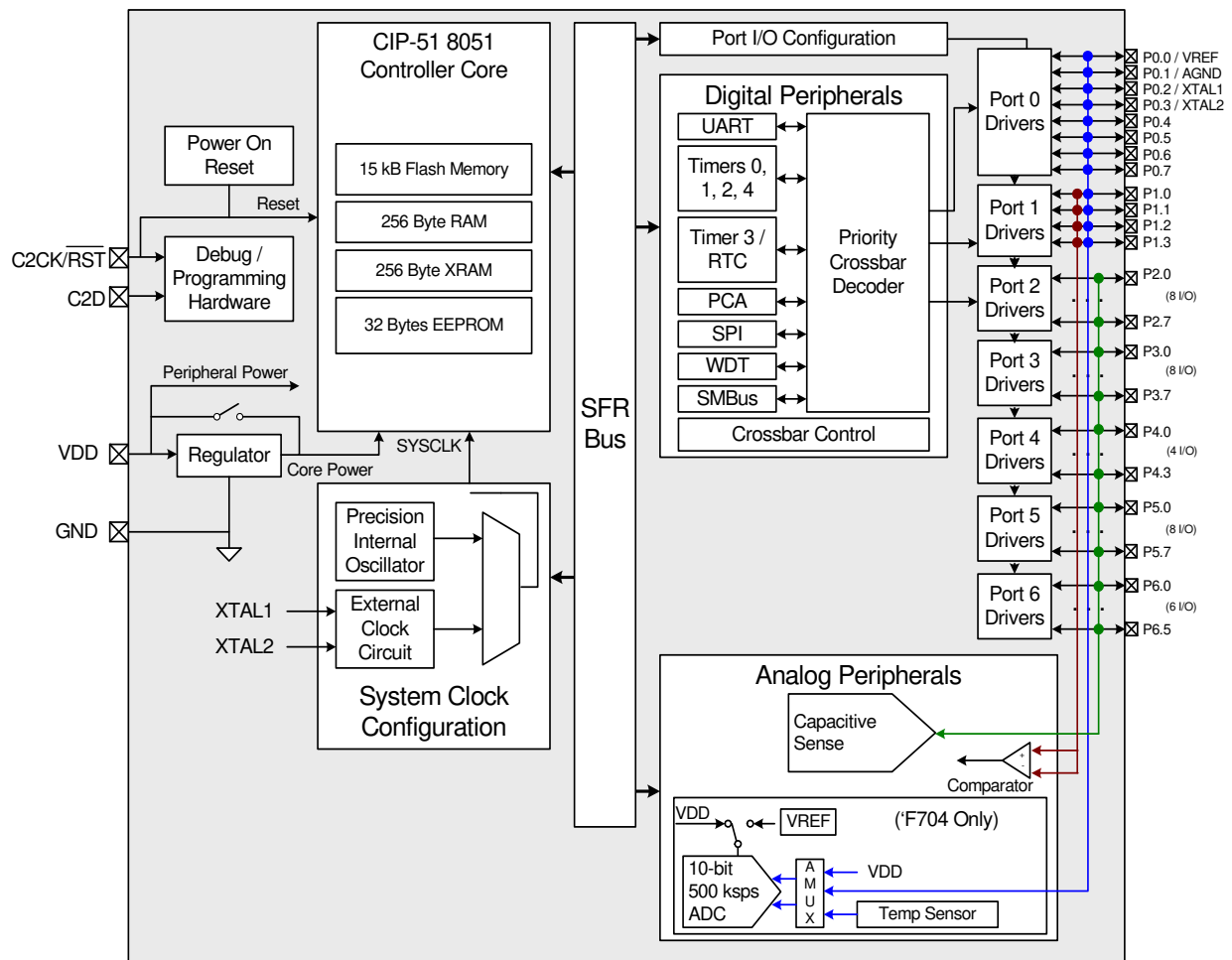


Figure 1.3. C8051F704/5 Block Diagram

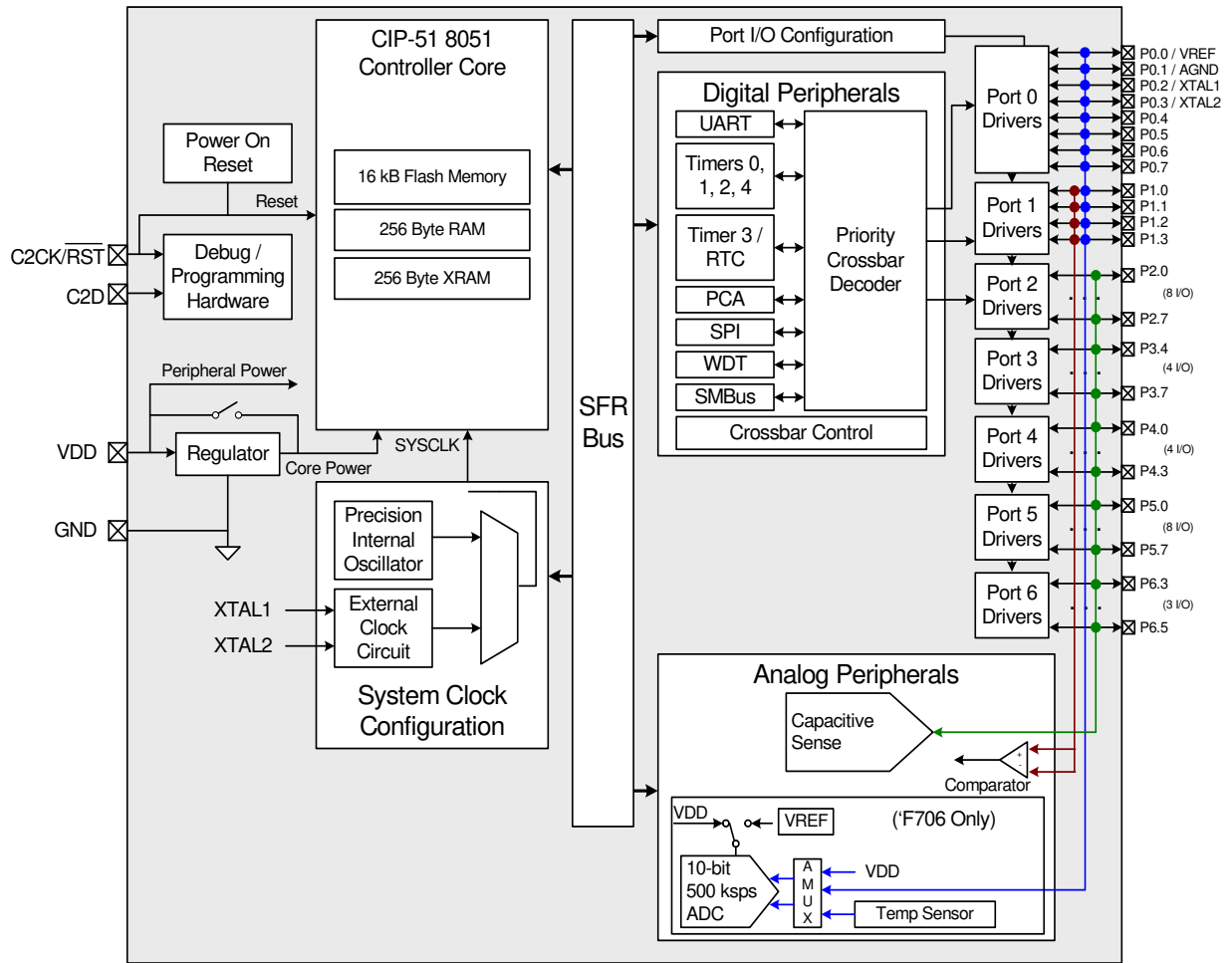


Figure 1.4. C8051F706/07 Block Diagram

C8051F70x/71x

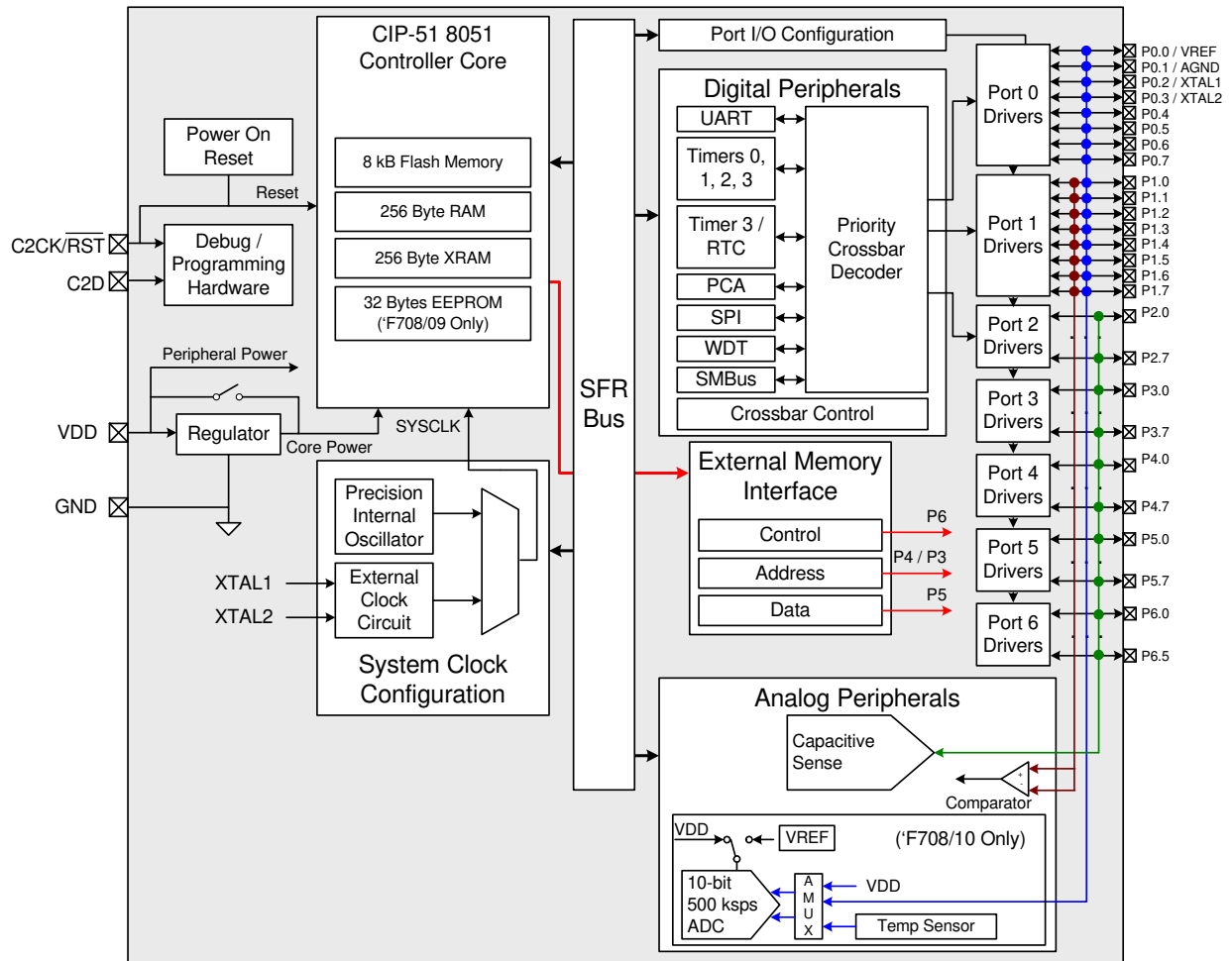


Figure 1.5. C8051F708/09/10/11 Block Diagram

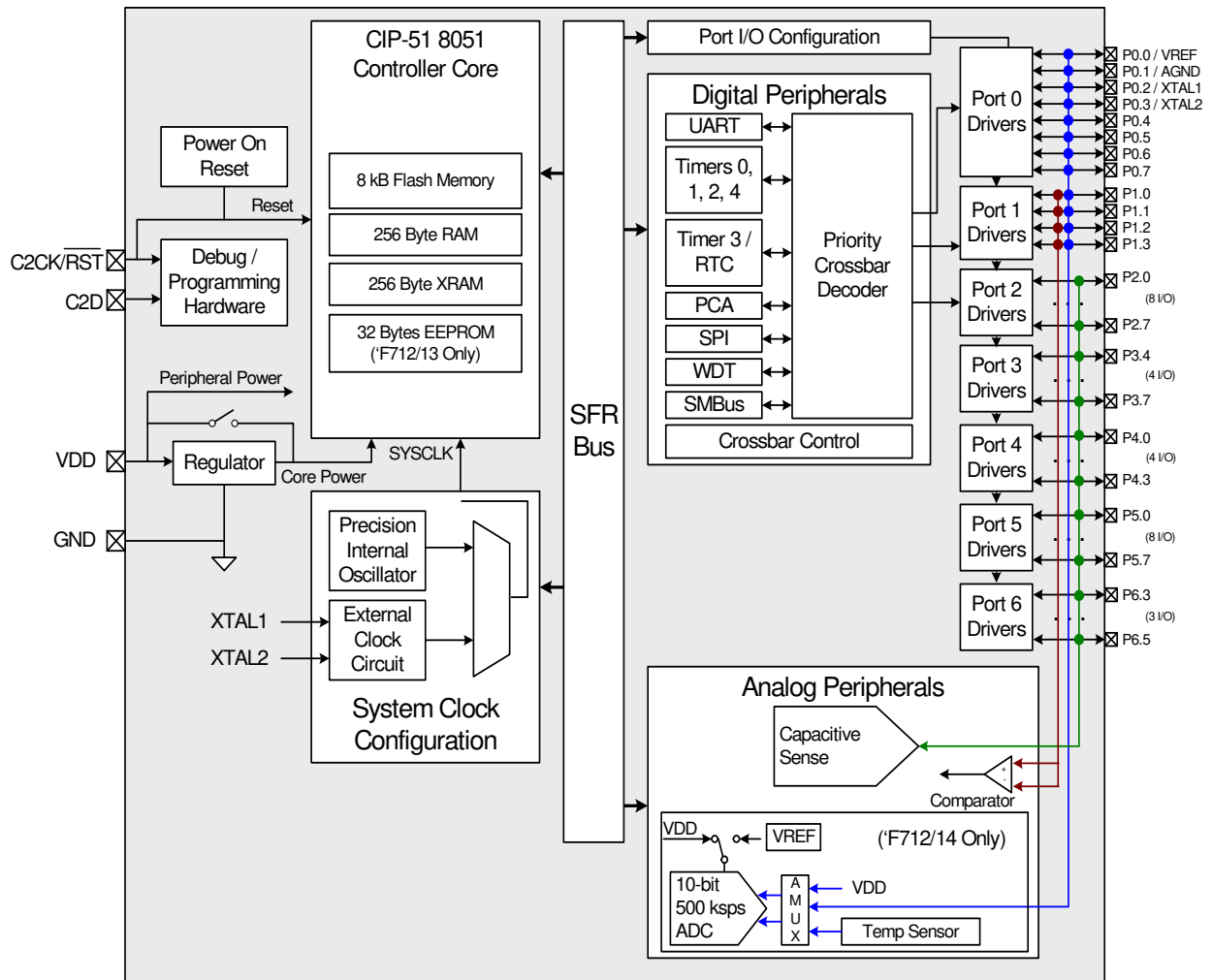


Figure 1.6. C8051F712/13/14/15 Block Diagram

C8051F70x/71x

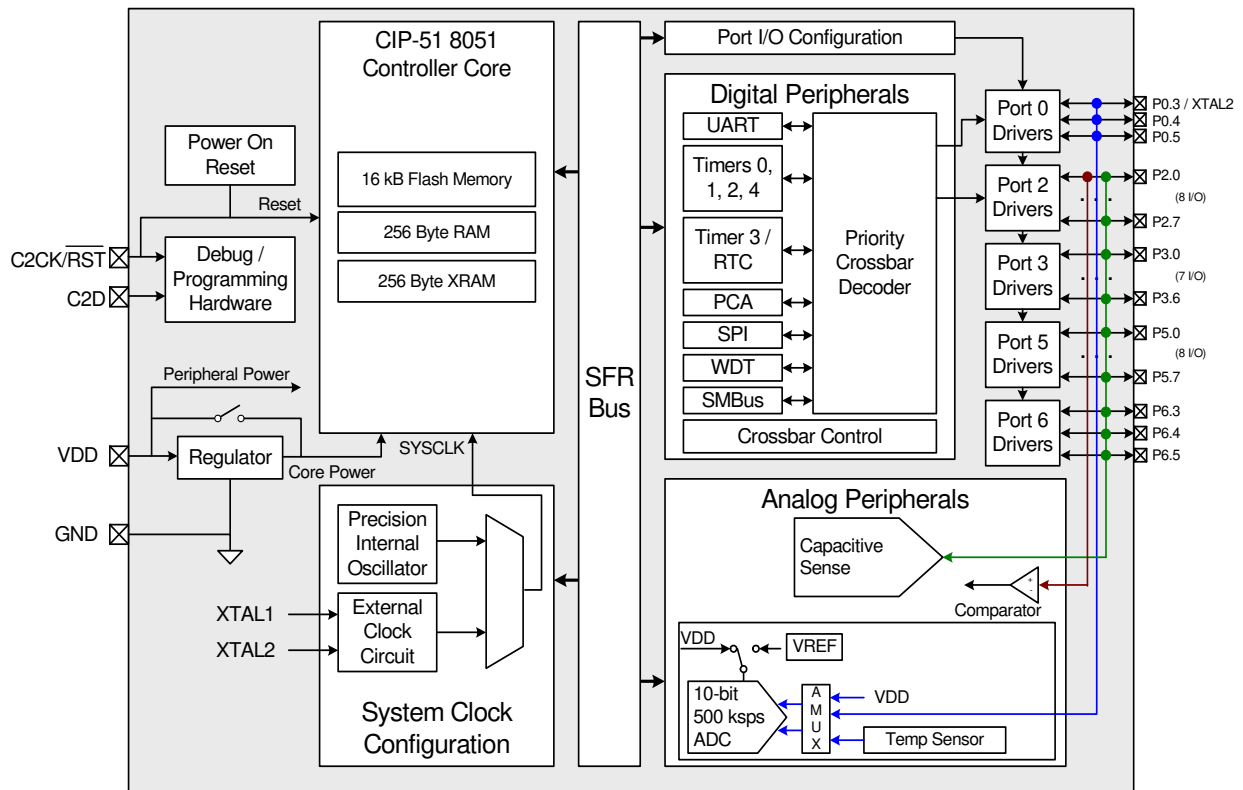


Figure 1.7. C8051F716 Block Diagram

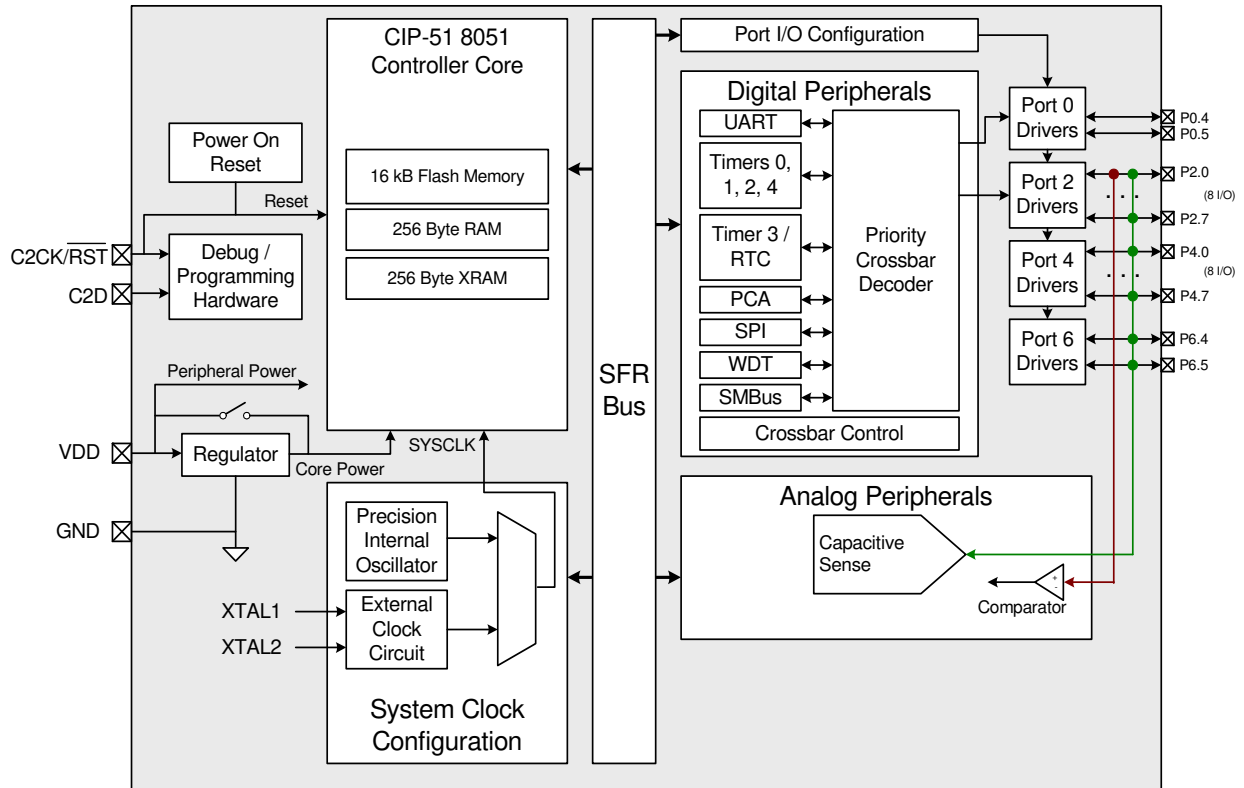


Figure 1.8. C8051F717 Block Diagram