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C8051F80x-83x

Mixed Signal ISP Flash MCU Family

Capacitance to Digital Converter
- Supports buttons, sliders, wheels, and capacitive proximity sensing
- Fast 40 µs per channel conversion time
- 16-bit resolution
- Up to 16 input channels
- Auto-scan and wake-on-touch
- Auto-accumulate 4x, 8x, 16, 32x, and 64x samples

Analog Peripherals
- **10-Bit ADC**
  - Up to 500 ksps
  - Up to 16 external single-ended inputs
  - VREF from on-chip VREF, external pin or V_{DD}
  - Internal or external start of conversion source
  - Built-in temperature sensor
- **Comparator**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source

On-Chip Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Low cost, **complete** development kit

High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

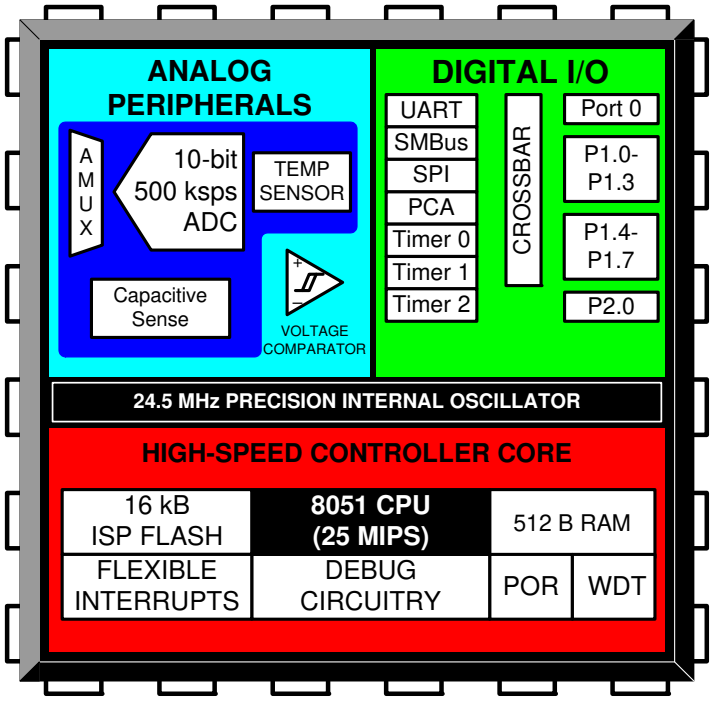
Memory
- Up to 512 bytes internal data RAM (256 + 256)
- Up to 16 kB Flash; In-system programmable in 512-byte sectors

Digital Peripherals
- 17 or 13 Port I/O with high sink current
- Hardware enhanced UART, SMBus™ (I^2C compatible), and enhanced SPI™ serial ports
- Three general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with 3 capture/compare modules and enhanced PWM functionality
- Real time clock mode using timer and crystal

Clock Sources
- 24.5 MHz ±2% Oscillator
  - Supports crystal-less UART operation
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly; useful in power saving modes

Supply Voltage 1.8 to 3.6 V
- Built-in voltage supply monitor

24-Pin QSOP, 20-Pin QFN, 16-Pin SOIC
Temperature Range: –40 to +85 °C



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1. System Overview

C8051F80x-83x devices are fully integrated, mixed-signal, system-on-a-chip capacitive sensing MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- Capacitive sense interface with 16 input channels
- 10-bit 500 ksps single-ended ADC with 16-channel analog multiplexer and integrated temperature sensor
- Precision calibrated 24.5 MHz internal oscillator
- 16 kb of on-chip Flash memory
- 512 bytes of on-chip RAM
- SMBus/I^2C, Enhanced UART, and Enhanced SPI serial interfaces implemented in hardware
- Three general-purpose 16-bit timers
- Programmable counter/timer array (PCA) with three capture/compare modules
- On-chip internal voltage reference
- On-chip Watchdog timer
- On-chip power-on reset and supply monitor
- On-chip voltage comparator
- 17 general purpose I/O

With on-chip power-on reset, V_{DD} monitor, watchdog timer, and clock oscillator, the C8051F80x-83x devices are truly stand-alone, system-on-a-chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The C8051F80x-83x processors include Silicon Laboratories' 2-Wire C2 Debug and Programming interface, which allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection of memory, viewing and modification of special function registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 1.8–3.6 V operation over the industrial temperature range (–45 to +85 °C). An internal LDO regulator is used to supply the processor core voltage at 1.8 V. The Port I/O and $\overline{\text{RST}}$ pins are tolerant of input signals up to 5 V. See Table 2.1 for ordering information. Block diagrams of the devices in the C8051F80x-83x family are shown in Figure 1.1 through Figure 1.9.

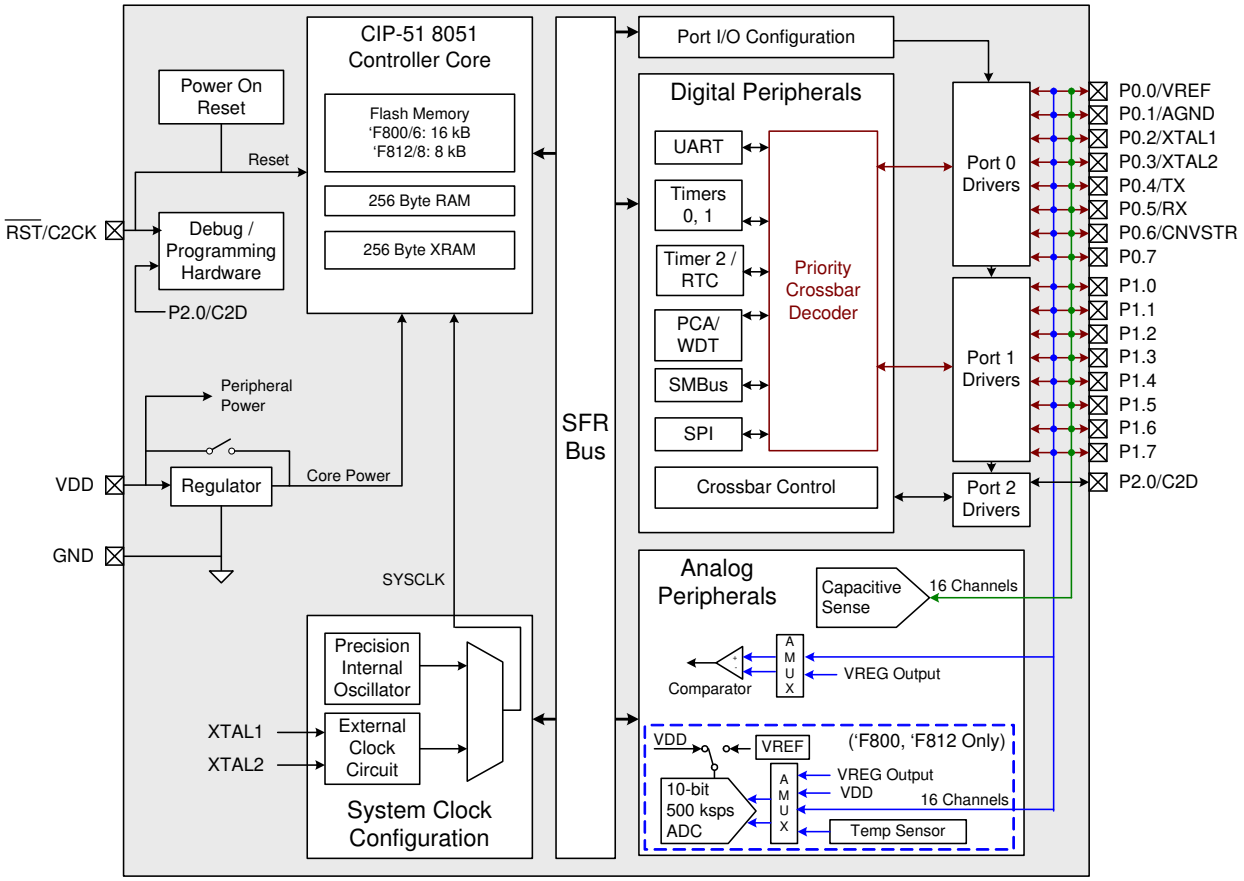

Figure 1.1. C8051F800, C8051F806, C8051F812, C8051F818 Block Diagram

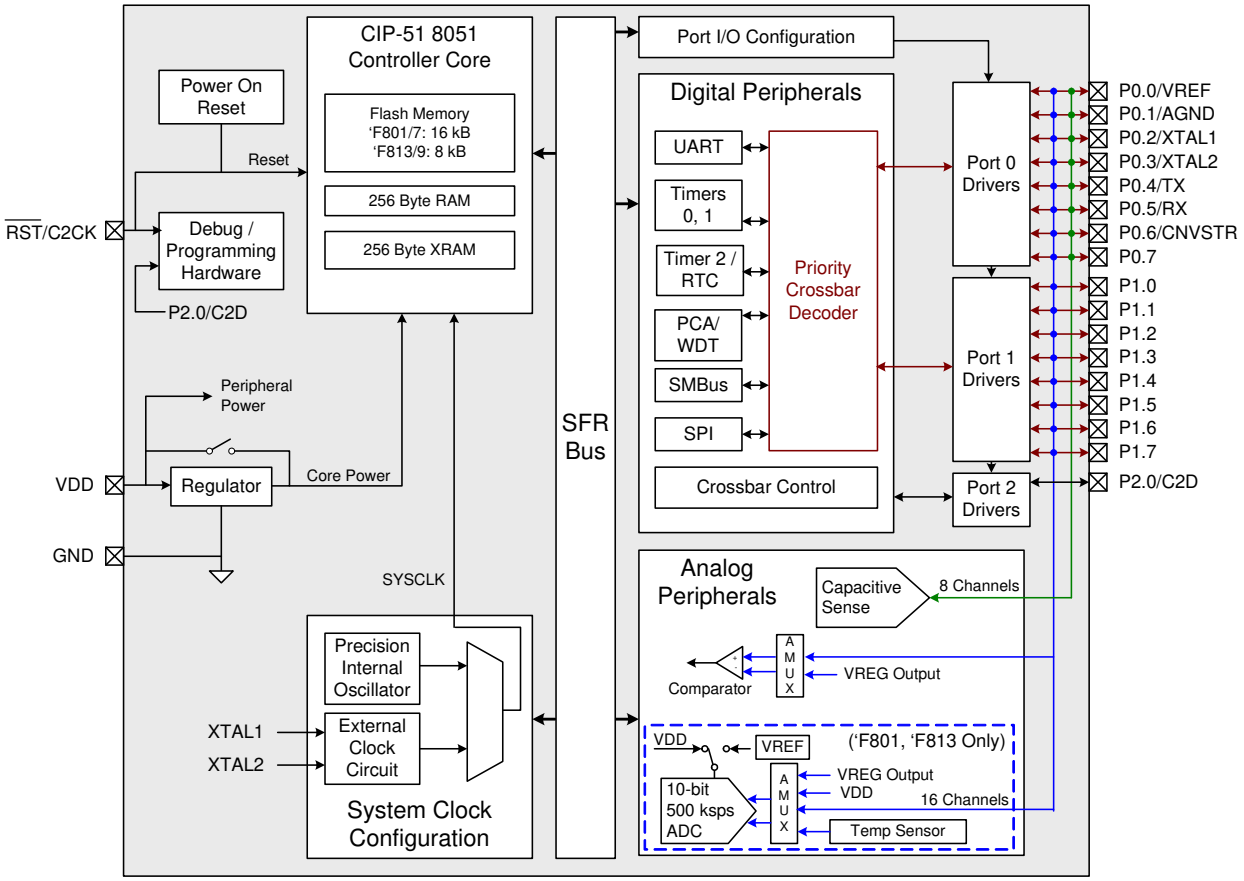

Figure 1.2. C8051F801, C8051F807, C8051F813, C8051F819 Block Diagram

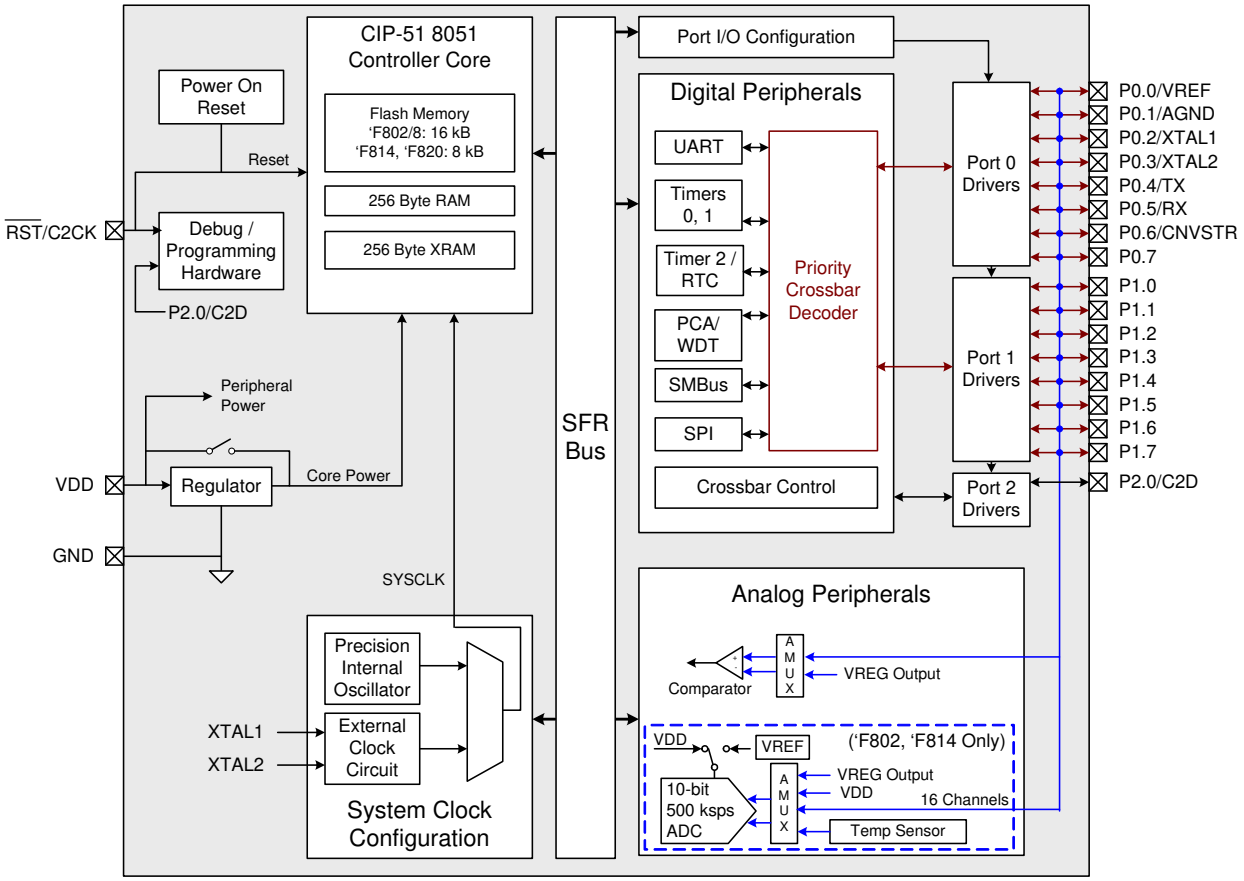

Figure 1.3. C8051F802, C8051F808, C8051F814, C8051F820 Block Diagram

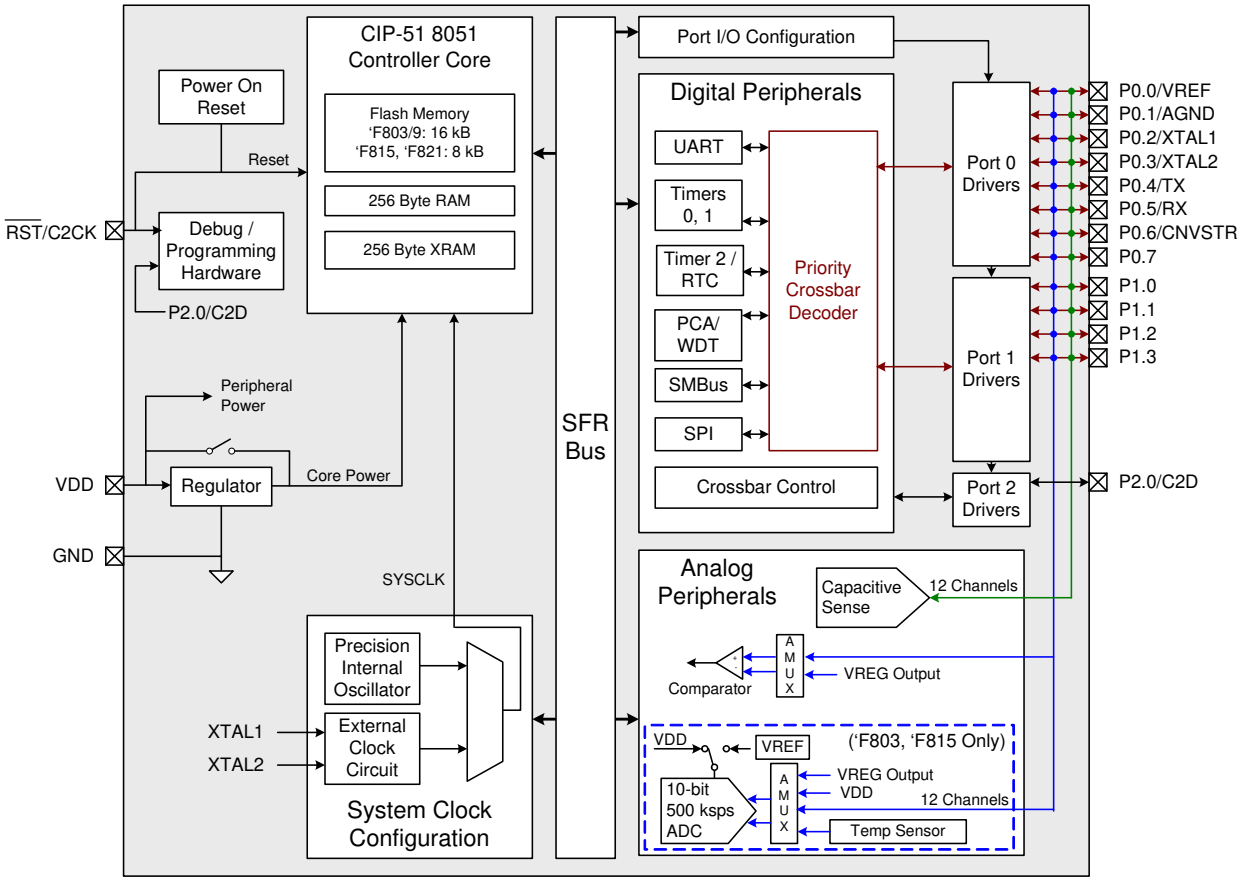

Figure 1.4. C8051F803, C8051F809, C8051F815, C8051F821 Block Diagram

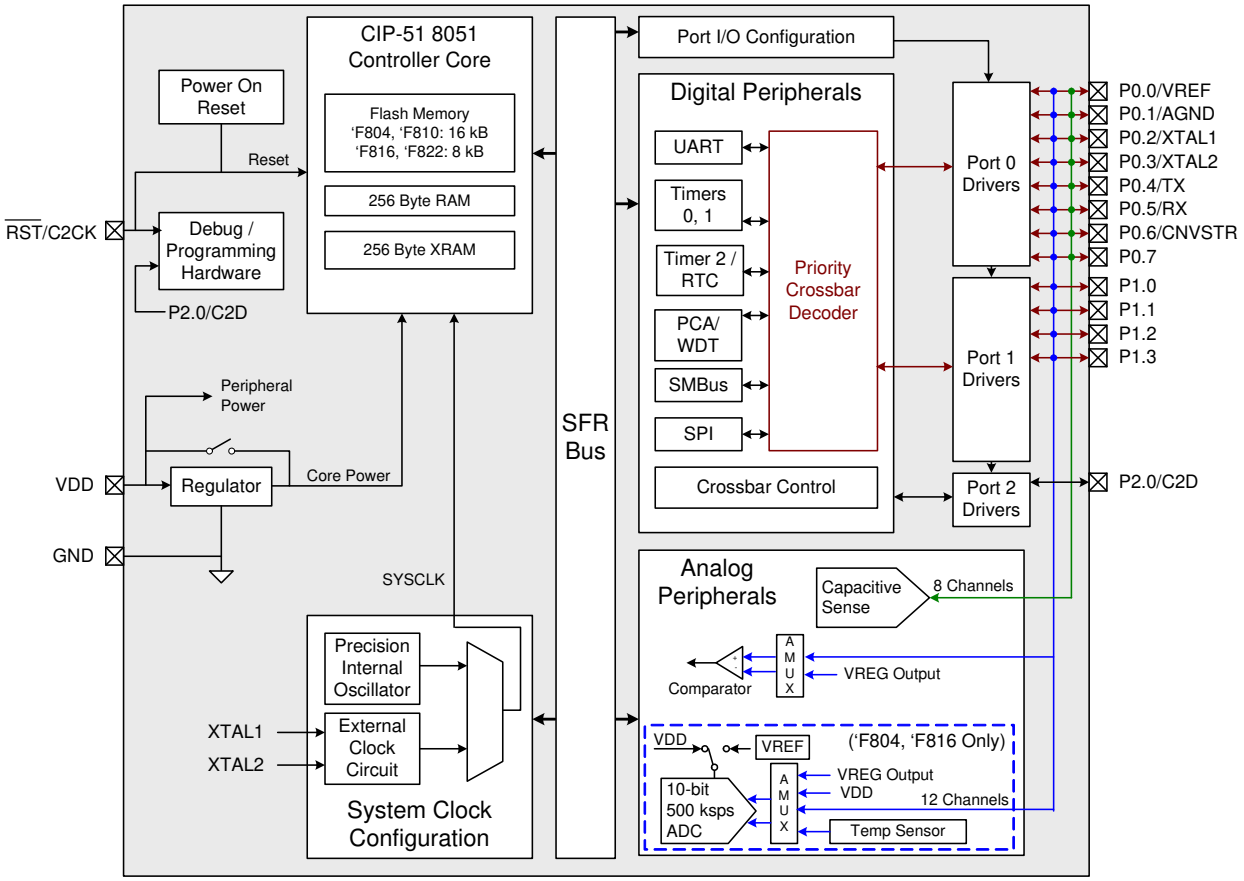

Figure 1.5. C8051F804, C8051F810, C8051F816, C8051F822 Block Diagram

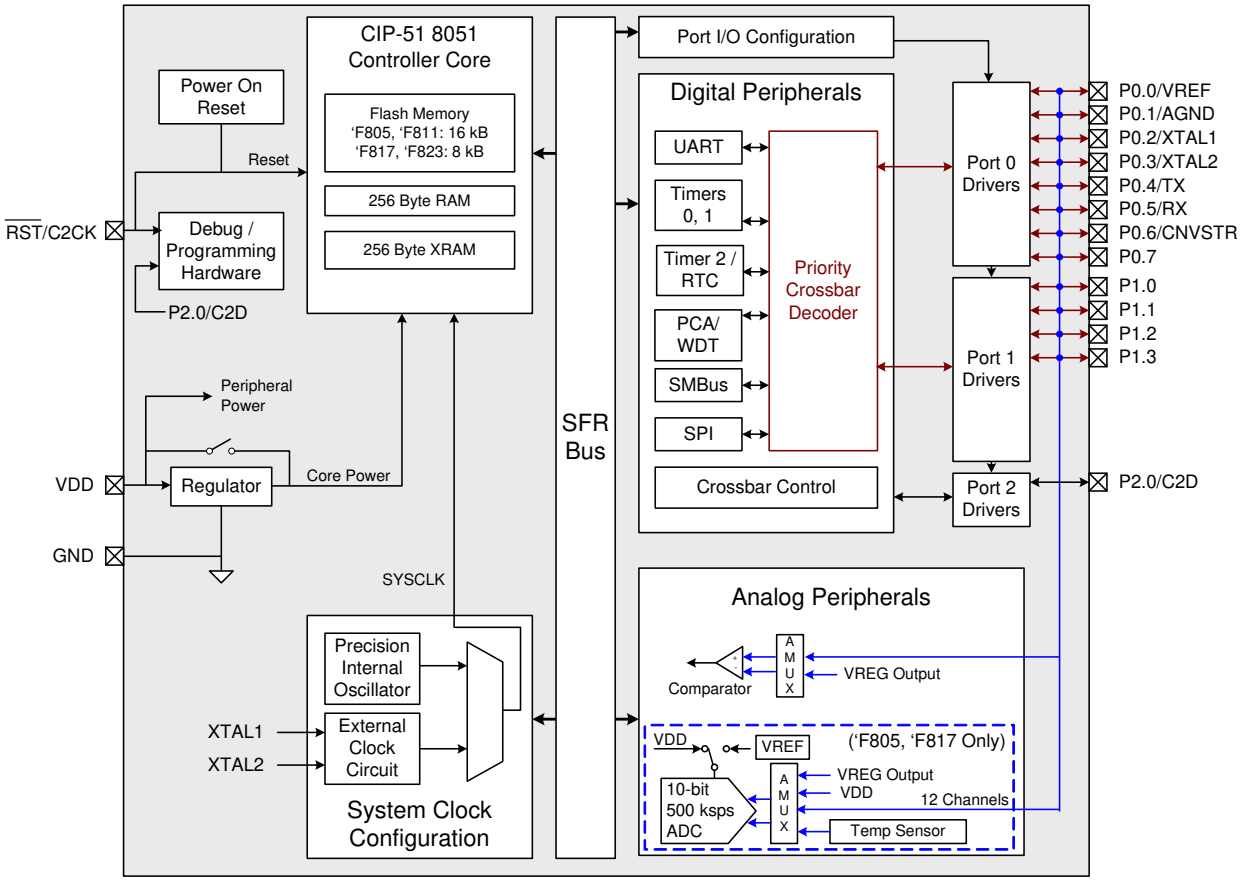

Figure 1.6. C8051F805, C8051F811, C8051F817, C8051F823 Block Diagram

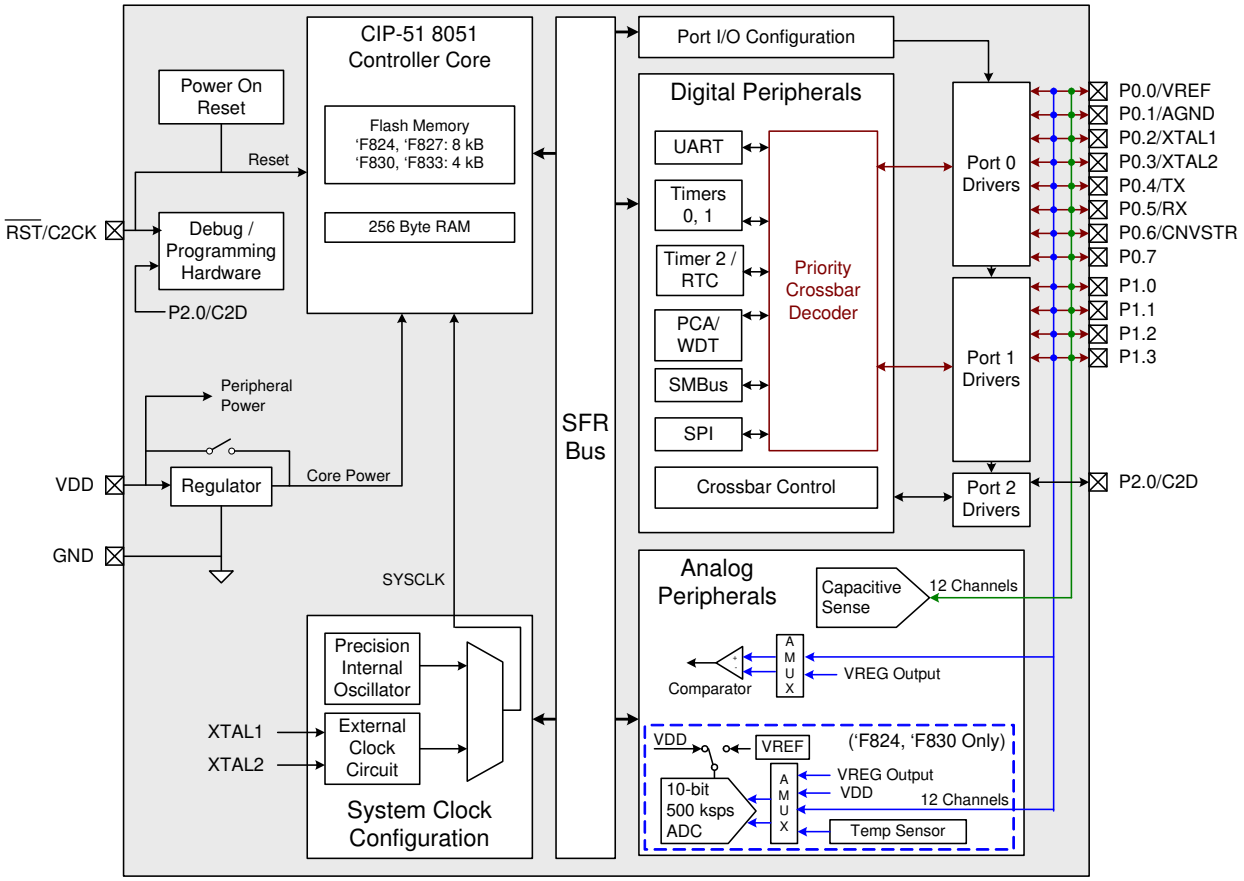

Figure 1.7. C8051F824, C8051F827, C8051F830, C8051F833 Block Diagram

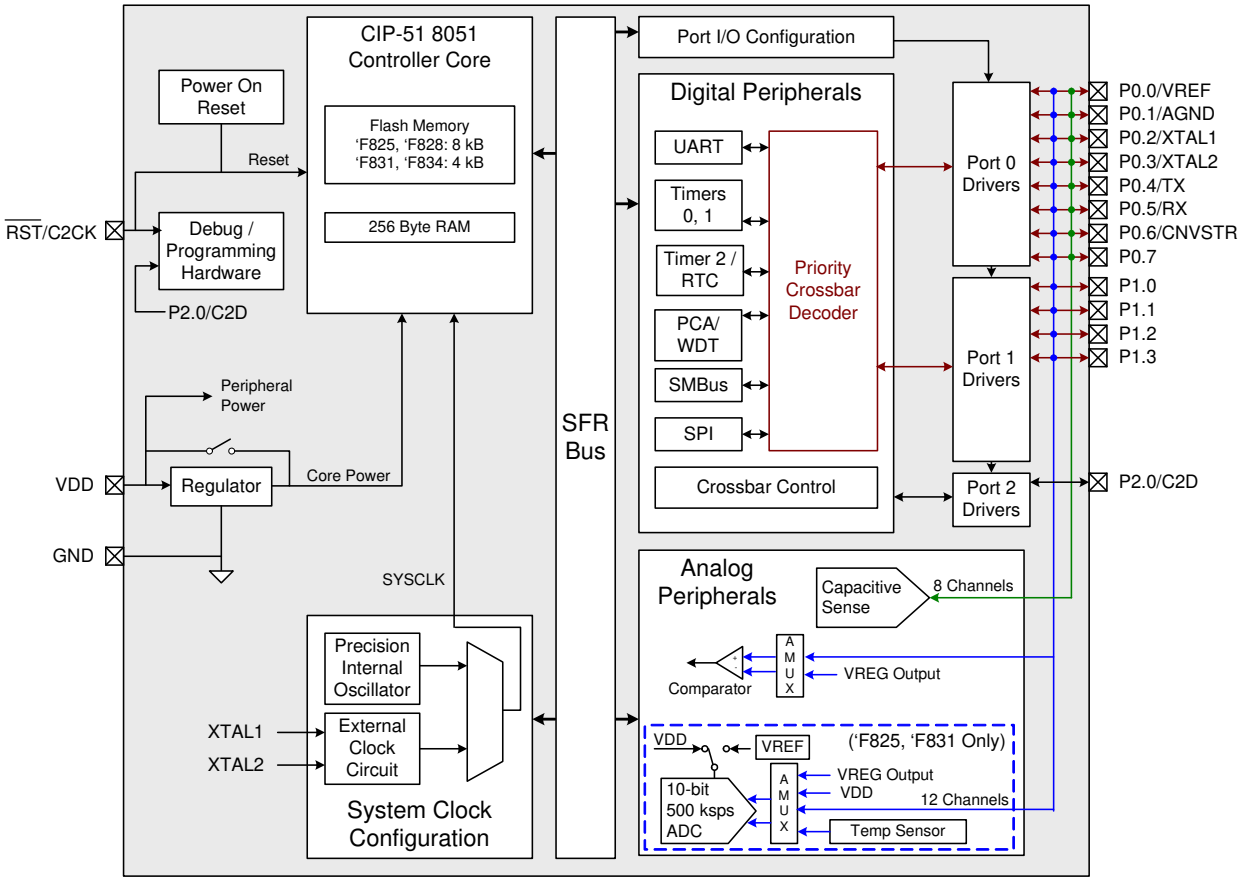

Figure 1.8. C8051F825, C8051F828, C8051F831, C8051F834 Block Diagram

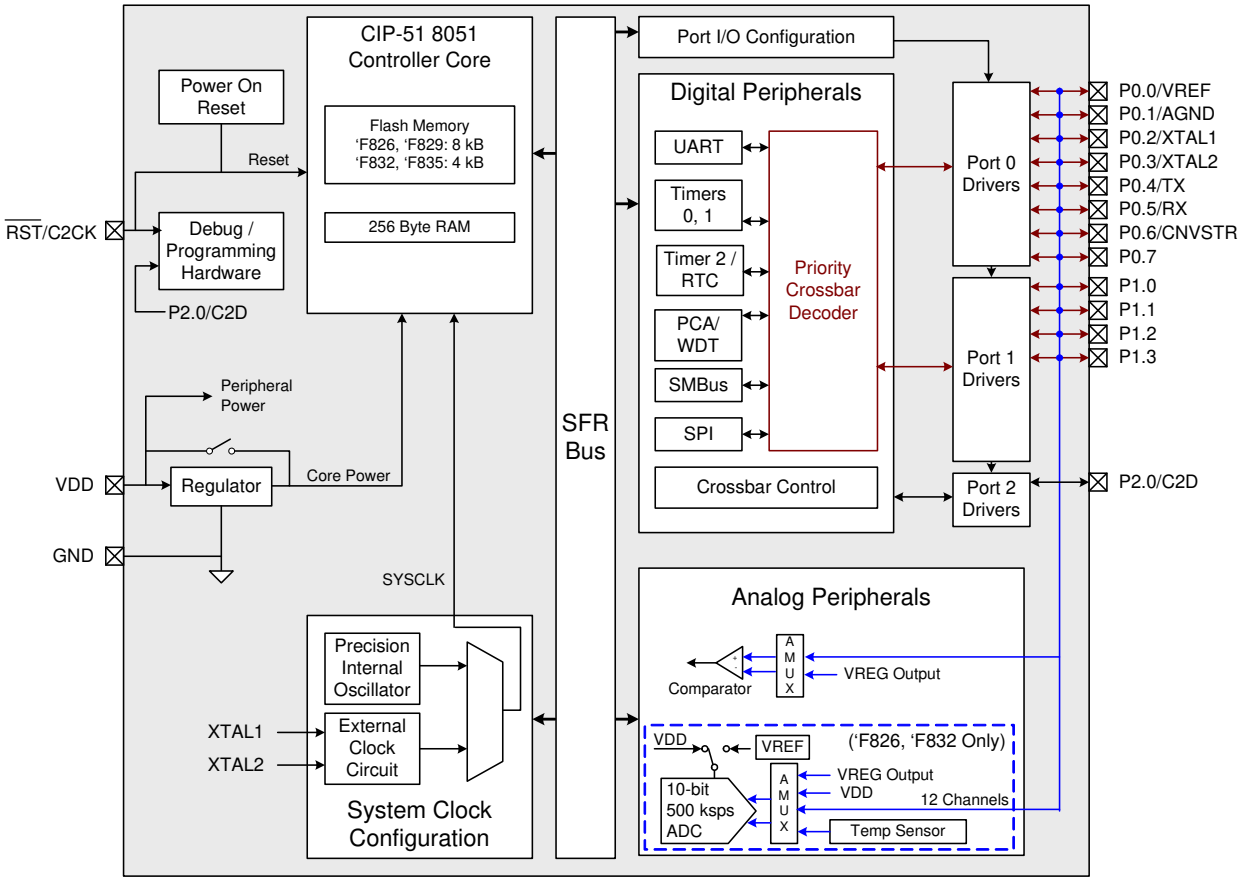

Figure 1.9. C8051F826, C8051F829, C8051F832, C8051F835 Block Diagram

2. Ordering Information

All C8051F80x-83x devices have the following features:

- 25 MIPS (Peak)
- Calibrated Internal Oscillator
- SMBus/I2C
- Enhanced SPI
- UART
- Programmable counter array (3 channels)
- 3 Timers (16-bit)
- 1 Comparator
- Pb-Free (RoHS compliant) package

In addition to the features listed above, each device in the C8051F80x-83x family has a set of features that vary across the product line. See Table 2.1 for a complete list of the unique feature sets for each device in the family.