



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



### Capacitance to Digital Converter

- Supports buttons, sliders, wheels, and capacitive proximity sensing
- Fast 40  $\mu$ s per channel conversion time
- 16-bit resolution
- Up to 16 input channels
- Auto-scan and wake-on-touch
- Auto-accumulate 4x, 8x, 16, 32x, and 64x samples

### Analog Peripherals

- **10-Bit ADC**
  - Up to 500 ksps
  - Up to 16 external single-ended inputs
  - VREF from on-chip VREF, external pin or  $V_{DD}$
  - Internal or external start of conversion source
  - Built-in temperature sensor
- **Comparator**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Low cost, **complete** development kit

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- Up to 512 bytes internal data RAM (256 + 256)
- Up to 16 kB Flash; In-system programmable in 512-byte sectors

### Digital Peripherals

- 17 or 13 Port I/O with high sink current
- Hardware enhanced UART, SMBus™ (I<sup>2</sup>C compatible), and enhanced SPI™ serial ports
- Three general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with 3 capture/compare modules and enhanced PWM functionality
- Real time clock mode using timer and crystal

### Clock Sources

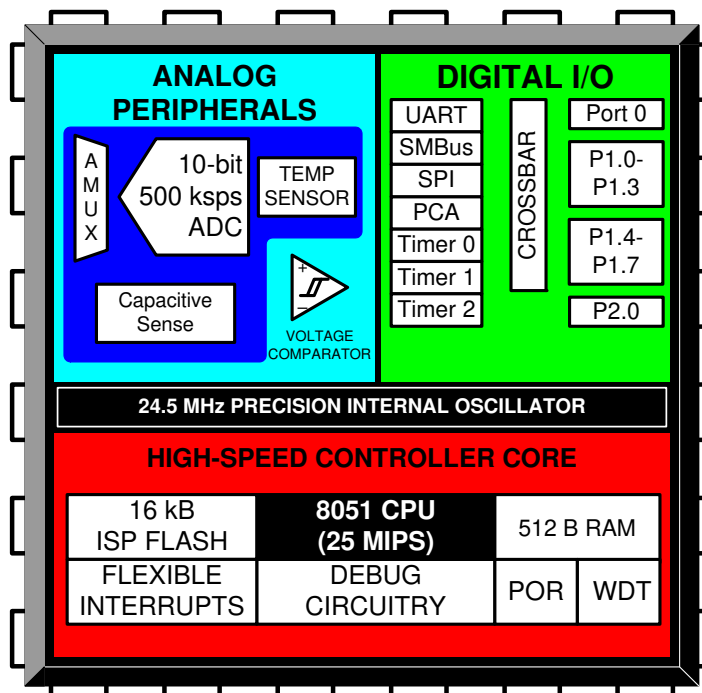
- 24.5 MHz  $\pm$ 2% Oscillator
  - Supports crystal-less UART operation
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly; useful in power saving modes

### Supply Voltage 1.8 to 3.6 V

- Built-in voltage supply monitor

**24-Pin QSOP, 20-Pin QFN, 16-Pin SOIC**

**Temperature Range: -40 to +85 °C**



# C8051F80x-83x

---



---

## Table of Contents

<b>1. System Overview</b> .....	<b>15</b>
<b>2. Ordering Information</b> .....	<b>25</b>
<b>3. Pin Definitions</b> .....	<b>28</b>
<b>4. QFN-20 Package Specifications</b> .....	<b>33</b>
<b>5. QSOP-24 Package Specifications</b> .....	<b>35</b>
<b>6. SOIC-16 Package Specifications</b> .....	<b>37</b>
<b>7. Electrical Characteristics</b> .....	<b>39</b>
7.1. Absolute Maximum Specifications.....	39
7.2. Electrical Characteristics .....	40
<b>8. 10-Bit ADC (ADC0)</b> .....	<b>46</b>
8.1. Output Code Formatting .....	47
8.2. 8-Bit Mode .....	47
8.3. Modes of Operation .....	47
8.3.1. Starting a Conversion.....	47
8.3.2. Tracking Modes.....	48
8.3.3. Settling Time Requirements.....	49
8.4. Programmable Window Detector.....	53
8.4.1. Window Detector Example.....	55
8.5. ADC0 Analog Multiplexer .....	56
<b>9. Temperature Sensor</b> .....	<b>58</b>
9.1. Calibration .....	58
<b>10. Voltage and Ground Reference Options</b> .....	<b>60</b>
10.1. External Voltage References.....	61
10.2. Internal Voltage Reference Options .....	61
10.3. Analog Ground Reference.....	61
10.4. Temperature Sensor Enable .....	61
<b>11. Voltage Regulator (REG0)</b> .....	<b>63</b>
<b>12. Comparator0</b> .....	<b>65</b>
12.1. Comparator Multiplexer .....	69
<b>13. Capacitive Sense (CS0)</b> .....	<b>71</b>
13.1. Configuring Port Pins as Capacitive Sense Inputs.....	72
13.2. Capacitive Sense Start-Of-Conversion Sources .....	72
13.3. Automatic Scanning.....	72
13.4. CS0 Comparator.....	73
13.5. CS0 Conversion Accumulator .....	74
13.6. Capacitive Sense Multiplexer .....	80
<b>14. CIP-51 Microcontroller</b> .....	<b>82</b>
14.1. Instruction Set.....	83
14.1.1. Instruction and CPU Timing .....	83
14.2. CIP-51 Register Descriptions .....	88
<b>15. Memory Organization</b> .....	<b>92</b>
15.1. Program Memory.....	93
15.1.1. MOVX Instruction and Program Memory .....	93

# C8051F80x-83x

---

15.2. Data Memory .....	93
15.2.1. Internal RAM .....	93
15.2.1.1. General Purpose Registers .....	94
15.2.1.2. Bit Addressable Locations .....	94
15.2.1.3. Stack .....	94
<b>16. In-System Device Identification .....</b>	<b>95</b>
<b>17. Special Function Registers .....</b>	<b>97</b>
<b>18. Interrupts .....</b>	<b>102</b>
18.1. MCU Interrupt Sources and Vectors .....	103
18.1.1. Interrupt Priorities .....	103
18.1.2. Interrupt Latency .....	103
18.2. <u>Interrupt Register</u> Descriptions .....	104
18.3. INT0 and INT1 External Interrupts .....	111
<b>19. Flash Memory .....</b>	<b>113</b>
19.1. Programming The Flash Memory .....	113
19.1.1. Flash Lock and Key Functions .....	113
19.1.2. Flash Erase Procedure .....	113
19.1.3. Flash Write Procedure .....	114
19.2. Non-volatile Data Storage .....	114
19.3. Security Options .....	114
19.4. Flash Write and Erase Guidelines .....	115
19.4.1. VDD Maintenance and the VDD Monitor .....	116
19.4.2. PSWE Maintenance .....	116
19.4.3. System Clock .....	117
<b>20. Power Management Modes .....</b>	<b>120</b>
20.1. Idle Mode .....	120
20.2. Stop Mode .....	121
20.3. Suspend Mode .....	121
<b>21. Reset Sources .....</b>	<b>123</b>
21.1. Power-On Reset .....	124
21.2. Power-Fail Reset / VDD Monitor .....	125
21.3. External Reset .....	126
21.4. Missing Clock Detector Reset .....	126
21.5. Comparator0 Reset .....	127
21.6. PCA Watchdog Timer Reset .....	127
21.7. Flash Error Reset .....	127
21.8. Software Reset .....	127
<b>22. Oscillators and Clock Selection .....</b>	<b>129</b>
22.1. System Clock Selection .....	129
22.2. Programmable Internal High-Frequency (H-F) Oscillator .....	131
22.3. External Oscillator Drive Circuit .....	133
22.3.1. External Crystal Example .....	135
22.3.2. External RC Example .....	136
22.3.3. External Capacitor Example .....	137
<b>23. Port Input/Output .....</b>	<b>138</b>

---

---

23.1. Port I/O Modes of Operation.....	139
23.1.1. Port Pins Configured for Analog I/O.....	139
23.1.2. Port Pins Configured For Digital I/O.....	139
23.1.3. Interfacing Port I/O to 5 V Logic.....	140
23.2. Assigning Port I/O Pins to Analog and Digital Functions.....	140
23.2.1. Assigning Port I/O Pins to Analog Functions.....	140
23.2.2. Assigning Port I/O Pins to Digital Functions.....	141
23.2.3. Assigning Port I/O Pins to External Digital Event Capture Functions ...	142
23.3. Priority Crossbar Decoder.....	143
23.4. Port I/O Initialization.....	147
23.5. Port Match.....	150
23.6. Special Function Registers for Accessing and Configuring Port I/O.....	152
<b>24. Cyclic Redundancy Check Unit (CRC0).....</b>	<b>159</b>
24.1. 16-bit CRC Algorithm.....	160
24.2. 32-bit CRC Algorithm.....	161
24.3. Preparing for a CRC Calculation.....	162
24.4. Performing a CRC Calculation.....	162
24.5. Accessing the CRC0 Result.....	162
24.6. CRC0 Bit Reverse Feature.....	166
<b>25. Enhanced Serial Peripheral Interface (SPI0).....</b>	<b>167</b>
25.1. Signal Descriptions.....	168
25.1.1. Master Out, Slave In (MOSI).....	168
25.1.2. Master In, Slave Out (MISO).....	168
25.1.3. Serial Clock (SCK).....	168
25.1.4. Slave Select (NSS).....	168
25.2. SPI0 Master Mode Operation.....	168
25.3. SPI0 Slave Mode Operation.....	170
25.4. SPI0 Interrupt Sources.....	171
25.5. Serial Clock Phase and Polarity.....	171
25.6. SPI Special Function Registers.....	173
<b>26. SMBus.....</b>	<b>180</b>
26.1. Supporting Documents.....	181
26.2. SMBus Configuration.....	181
26.3. SMBus Operation.....	181
26.3.1. Transmitter Vs. Receiver.....	182
26.3.2. Arbitration.....	182
26.3.3. Clock Low Extension.....	182
26.3.4. SCL Low Timeout.....	182
26.3.5. SCL High (SMBus Free) Timeout.....	183
26.4. Using the SMBus.....	183
26.4.1. SMBus Configuration Register.....	183
26.4.2. SMB0CN Control Register.....	187
26.4.2.1. Software ACK Generation.....	187
26.4.2.2. Hardware ACK Generation.....	187
26.4.3. Hardware Slave Address Recognition.....	189

---

# C8051F80x-83x

---

26.4.4. Data Register .....	192
26.5. SMBus Transfer Modes.....	193
26.5.1. Write Sequence (Master) .....	193
26.5.2. Read Sequence (Master) .....	194
26.5.3. Write Sequence (Slave) .....	195
26.5.4. Read Sequence (Slave).....	196
26.6. SMBus Status Decoding.....	196
<b>27. UART0 .....</b>	<b>201</b>
27.1. Enhanced Baud Rate Generation.....	202
27.2. Operational Modes .....	203
27.2.1. 8-Bit UART .....	203
27.2.2. 9-Bit UART .....	204
27.3. Multiprocessor Communications .....	205
<b>28. Timers .....</b>	<b>209</b>
28.1. Timer 0 and Timer 1 .....	211
28.1.1. Mode 0: 13-bit Counter/Timer .....	211
28.1.2. Mode 1: 16-bit Counter/Timer .....	212
28.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload.....	212
28.1.4. Mode 3: Two 8-bit Counter/Timers (Timer 0 Only).....	213
28.2. Timer 2 .....	219
28.2.1. 16-bit Timer with Auto-Reload.....	219
28.2.2. 8-bit Timers with Auto-Reload.....	220
<b>29. Programmable Counter Array.....</b>	<b>225</b>
29.1. PCA Counter/Timer .....	226
29.2. PCA0 Interrupt Sources.....	227
29.3. Capture/Compare Modules .....	228
29.3.1. Edge-Triggered Capture Mode .....	229
29.3.2. Software Timer (Compare) Mode.....	230
29.3.3. High-Speed Output Mode .....	231
29.3.4. Frequency Output Mode .....	232
29.3.5. 8-bit through 15-bit Pulse Width Modulator Modes .....	232
29.3.5.1. 8-bit Pulse Width Modulator Mode.....	233
29.3.5.2. 9-bit through 15-bit Pulse Width Modulator Mode .....	234
29.3.6. 16-Bit Pulse Width Modulator Mode.....	235
29.4. Watchdog Timer Mode .....	236
29.4.1. Watchdog Timer Operation .....	236
29.4.2. Watchdog Timer Usage .....	237
29.5. Register Descriptions for PCA0.....	237
<b>30. C2 Interface .....</b>	<b>244</b>
30.1. C2 Interface Registers.....	244
30.2. C2CK Pin Sharing .....	247
<b>Document Change List.....</b>	<b>248</b>
<b>Contact Information.....</b>	<b>250</b>

---

---

## List of Tables

<b>1. System Overview</b>	
<b>2. Ordering Information</b>	
Table 2.1. Product Selection Guide .....	26
<b>3. Pin Definitions</b>	
Table 3.1. Pin Definitions for the C8051F80x-83x .....	28
<b>4. QFN-20 Package Specifications</b>	
Table 4.1. QFN-20 Package Dimensions .....	33
Table 4.2. QFN-20 PCB Land Pattern Dimensions .....	34
<b>5. QSOP-24 Package Specifications</b>	
Table 5.1. QSOP-24 Package Dimensions .....	35
Table 5.2. QSOP-24 PCB Land Pattern Dimensions .....	36
<b>6. SOIC-16 Package Specifications</b>	
Table 6.1. SOIC-16 Package Dimensions .....	37
Table 6.2. SOIC-16 PCB Land Pattern Dimensions .....	38
<b>7. Electrical Characteristics</b>	
Table 7.1. Absolute Maximum Ratings .....	39
Table 7.2. Global Electrical Characteristics .....	40
Table 7.3. Port I/O DC Electrical Characteristics .....	41
Table 7.4. Reset Electrical Characteristics .....	41
Table 7.5. Internal Voltage Regulator Electrical Characteristics .....	41
Table 7.6. Flash Electrical Characteristics .....	42
Table 7.7. Internal High-Frequency Oscillator Electrical Characteristics .....	42
Table 7.8. Capacitive Sense Electrical Characteristics .....	42
Table 7.9. ADC0 Electrical Characteristics .....	43
Table 7.10. Power Management Electrical Characteristics .....	44
Table 7.11. Temperature Sensor Electrical Characteristics .....	44
Table 7.12. Voltage Reference Electrical Characteristics .....	44
Table 7.13. Comparator Electrical Characteristics .....	45
<b>8. 10-Bit ADC (ADC0)</b>	
<b>9. Temperature Sensor</b>	
<b>10. Voltage and Ground Reference Options</b>	
<b>11. Voltage Regulator (REG0)</b>	
<b>12. Comparator0</b>	
<b>13. Capacitive Sense (CS0)</b>	
Table 13.1. Operation with Auto-scan and Accumulate .....	74
<b>14. CIP-51 Microcontroller</b>	
Table 14.1. CIP-51 Instruction Set Summary .....	84
<b>15. Memory Organization</b>	
<b>16. In-System Device Identification</b>	
<b>17. Special Function Registers</b>	
Table 17.1. Special Function Register (SFR) Memory Map .....	97
Table 17.2. Special Function Registers .....	98
<b>18. Interrupts</b>	



# C8051F80x-83x

---

Table 18.1. Interrupt Summary .....	104
<b>19. Flash Memory</b>	
Table 19.1. Flash Security Summary .....	115
<b>20. Power Management Modes</b>	
<b>21. Reset Sources</b>	
<b>22. Oscillators and Clock Selection</b>	
<b>23. Port Input/Output</b>	
Table 23.1. Port I/O Assignment for Analog Functions .....	141
Table 23.2. Port I/O Assignment for Digital Functions .....	142
Table 23.3. Port I/O Assignment for External Digital Event Capture Functions ....	142
<b>24. Cyclic Redundancy Check Unit (CRC0)</b>	
Table 24.1. Example 16-bit CRC Outputs .....	160
Table 24.2. Example 32-bit CRC Outputs .....	161
<b>25. Enhanced Serial Peripheral Interface (SPI0)</b>	
Table 25.1. SPI Slave Timing Parameters .....	179
<b>26. SMBus</b>	
Table 26.1. SMBus Clock Source Selection .....	184
Table 26.2. Minimum SDA Setup and Hold Times .....	185
Table 26.3. Sources for Hardware Changes to SMB0CN .....	189
Table 26.4. Hardware Address Recognition Examples (EHACK = 1) .....	190
Table 26.5. SMBus Status Decoding With Hardware ACK Generation Disabled (EHACK = 0) .....	197
Table 26.6. SMBus Status Decoding With Hardware ACK Generation Enabled (EHACK = 1) .....	199
<b>27. UART0</b>	
Table 27.1. Timer Settings for Standard Baud Rates Using The Internal 24.5 MHz Oscillator .....	208
Table 27.2. Timer Settings for Standard Baud Rates Using an External 22.1184 MHz Oscillator .....	208
<b>28. Timers</b>	
<b>29. Programmable Counter Array</b>	
Table 29.1. PCA Timebase Input Options .....	226
Table 29.2. PCA0CPM and PCA0PWM Bit Settings for PCA Capture/Compare Mod- ules <sup>1,2,3,4,5,6</sup> .....	228
Table 29.3. Watchdog Timer Timeout Intervals <sup>1</sup> .....	237
<b>30. C2 Interface</b>	

---

## List of Figures

### 1. System Overview

Figure 1.1. C8051F800, C8051F806, C8051F812, C8051F818 Block Diagram .....	16
Figure 1.2. C8051F801, C8051F807, C8051F813, C8051F819 Block Diagram .....	17
Figure 1.3. C8051F802, C8051F808, C8051F814, C8051F820 Block Diagram .....	18
Figure 1.4. C8051F803, C8051F809, C8051F815, C8051F821 Block Diagram .....	19
Figure 1.5. C8051F804, C8051F810, C8051F816, C8051F822 Block Diagram .....	20
Figure 1.6. C8051F805, C8051F811, C8051F817, C8051F823 Block Diagram .....	21
Figure 1.7. C8051F824, C8051F827, C8051F830, C8051F833 Block Diagram .....	22
Figure 1.8. C8051F825, C8051F828, C8051F831, C8051F834 Block Diagram .....	23
Figure 1.9. C8051F826, C8051F829, C8051F832, C8051F835 Block Diagram .....	24

### 2. Ordering Information

### 3. Pin Definitions

Figure 3.1. QFN-20 Pinout Diagram (Top View) .....	30
Figure 3.2. QSOP-24 Pinout Diagram (Top View) .....	31
Figure 3.3. SOIC-16 Pinout Diagram (Top View) .....	32

### 4. QFN-20 Package Specifications

Figure 4.1. QFN-20 Package Drawing .....	33
Figure 4.2. QFN-20 Recommended PCB Land Pattern .....	34

### 5. QSOP-24 Package Specifications

Figure 5.1. QSOP-24 Package Drawing .....	35
Figure 5.2. QSOP-24 PCB Land Pattern .....	36

### 6. SOIC-16 Package Specifications

Figure 6.1. SOIC-16 Package Drawing .....	37
Figure 6.2. SOIC-16 PCB Land Pattern .....	38

### 7. Electrical Characteristics

### 8. 10-Bit ADC (ADC0)

Figure 8.1. ADC0 Functional Block Diagram .....	46
Figure 8.2. 10-Bit ADC Track and Conversion Example Timing .....	48
Figure 8.3. ADC0 Equivalent Input Circuits .....	49
Figure 8.4. ADC Window Compare Example: Right-Justified Data .....	55
Figure 8.5. ADC Window Compare Example: Left-Justified Data .....	55
Figure 8.6. ADC0 Multiplexer Block Diagram .....	56

### 9. Temperature Sensor

Figure 9.1. Temperature Sensor Transfer Function .....	58
Figure 9.2. Temperature Sensor Error with 1-Point Calibration at 0 °C .....	59

### 10. Voltage and Ground Reference Options

Figure 10.1. Voltage Reference Functional Block Diagram .....	60
---	----

### 11. Voltage Regulator (REG0)

### 12. Comparator0

Figure 12.1. Comparator0 Functional Block Diagram .....	65
Figure 12.2. Comparator Hysteresis Plot .....	66
Figure 12.3. Comparator Input Multiplexer Block Diagram .....	69

### 13. Capacitive Sense (CS0)

# C8051F80x-83x

---

Figure 13.1. CS0 Block Diagram .....	71
Figure 13.2. Auto-Scan Example .....	73
Figure 13.3. CS0 Multiplexer Block Diagram .....	80
<b>14. CIP-51 Microcontroller</b>	
Figure 14.1. CIP-51 Block Diagram .....	82
<b>15. Memory Organization</b>	
Figure 15.1. C8051F80x-83x Memory Map .....	92
Figure 15.2. Flash Program Memory Map .....	93
<b>16. In-System Device Identification</b>	
<b>17. Special Function Registers</b>	
<b>18. Interrupts</b>	
<b>19. Flash Memory</b>	
<b>20. Power Management Modes</b>	
<b>21. Reset Sources</b>	
Figure 21.1. Reset Sources .....	123
Figure 21.2. Power-On and VDD Monitor Reset Timing .....	124
<b>22. Oscillators and Clock Selection</b>	
Figure 22.1. Oscillator Options .....	129
Figure 22.2. External 32.768 kHz Quartz Crystal Oscillator Connection Diagram	136
<b>23. Port Input/Output</b>	
Figure 23.1. Port I/O Functional Block Diagram .....	138
Figure 23.2. Port I/O Cell Block Diagram .....	139
Figure 23.3. Port I/O Overdrive Current .....	140
Figure 23.4. Priority Crossbar Decoder Potential Pin Assignments .....	144
Figure 23.5. Priority Crossbar Decoder Example 1—No Skipped Pins .....	145
Figure 23.6. Priority Crossbar Decoder Example 2—Skipping Pins .....	146
<b>24. Cyclic Redundancy Check Unit (CRC0)</b>	
Figure 24.1. CRC0 Block Diagram .....	159
<b>25. Enhanced Serial Peripheral Interface (SPI0)</b>	
Figure 25.1. SPI Block Diagram .....	167
Figure 25.2. Multiple-Master Mode Connection Diagram .....	169
Figure 25.3. 3-Wire Single Master and 3-Wire Single Slave Mode Connection Diagram	169
Figure 25.4. 4-Wire Single Master Mode and 4-Wire Slave Mode Connection Diagram	170
Figure 25.5. Master Mode Data/Clock Timing .....	172
Figure 25.6. Slave Mode Data/Clock Timing (CKPHA = 0) .....	172
Figure 25.7. Slave Mode Data/Clock Timing (CKPHA = 1) .....	173
Figure 25.8. SPI Master Timing (CKPHA = 0) .....	177
Figure 25.9. SPI Master Timing (CKPHA = 1) .....	177
Figure 25.10. SPI Slave Timing (CKPHA = 0) .....	178
Figure 25.11. SPI Slave Timing (CKPHA = 1) .....	178
<b>26. SMBus</b>	
Figure 26.1. SMBus Block Diagram .....	180
Figure 26.2. Typical SMBus Configuration .....	181

---

---

Figure 26.3. SMBus Transaction .....	182
Figure 26.4. Typical SMBus SCL Generation .....	184
Figure 26.5. Typical Master Write Sequence .....	193
Figure 26.6. Typical Master Read Sequence .....	194
Figure 26.7. Typical Slave Write Sequence .....	195
Figure 26.8. Typical Slave Read Sequence .....	196
<b>27. UART0</b>	
Figure 27.1. UART0 Block Diagram .....	201
Figure 27.2. UART0 Baud Rate Logic .....	202
Figure 27.3. UART Interconnect Diagram .....	203
Figure 27.4. 8-Bit UART Timing Diagram .....	203
Figure 27.5. 9-Bit UART Timing Diagram .....	204
Figure 27.6. UART Multi-Processor Mode Interconnect Diagram .....	205
<b>28. Timers</b>	
Figure 28.1. T0 Mode 0 Block Diagram .....	212
Figure 28.2. T0 Mode 2 Block Diagram .....	213
Figure 28.3. T0 Mode 3 Block Diagram .....	214
Figure 28.4. Timer 2 16-Bit Mode Block Diagram .....	219
Figure 28.5. Timer 2 8-Bit Mode Block Diagram .....	220
<b>29. Programmable Counter Array</b>	
Figure 29.1. PCA Block Diagram .....	225
Figure 29.2. PCA Counter/Timer Block Diagram .....	226
Figure 29.3. PCA Interrupt Block Diagram .....	227
Figure 29.4. PCA Capture Mode Diagram .....	229
Figure 29.5. PCA Software Timer Mode Diagram .....	230
Figure 29.6. PCA High-Speed Output Mode Diagram .....	231
Figure 29.7. PCA Frequency Output Mode .....	232
Figure 29.8. PCA 8-Bit PWM Mode Diagram .....	233
Figure 29.9. PCA 9-bit through 15-Bit PWM Mode Diagram .....	234
Figure 29.10. PCA 16-Bit PWM Mode .....	235
Figure 29.11. PCA Module 2 with Watchdog Timer Enabled .....	236
<b>30. C2 Interface</b>	
Figure 30.1. Typical C2 Pin Sharing .....	247

## List of Registers

SFR Definition 8.1. ADC0CF: ADC0 Configuration .....	50
SFR Definition 8.2. ADC0H: ADC0 Data Word MSB .....	51
SFR Definition 8.3. ADC0L: ADC0 Data Word LSB .....	51
SFR Definition 8.4. ADC0CN: ADC0 Control .....	52
SFR Definition 8.5. ADC0GTH: ADC0 Greater-Than Data High Byte .....	53
SFR Definition 8.6. ADC0GTL: ADC0 Greater-Than Data Low Byte .....	53
SFR Definition 8.7. ADC0LTH: ADC0 Less-Than Data High Byte .....	54
SFR Definition 8.8. ADC0LTL: ADC0 Less-Than Data Low Byte .....	54
SFR Definition 8.9. ADC0MX: AMUX0 Channel Select .....	57
SFR Definition 10.1. REF0CN: Voltage Reference Control .....	62
SFR Definition 11.1. REG0CN: Voltage Regulator Control .....	64
SFR Definition 12.1. CPT0CN: Comparator0 Control .....	67
SFR Definition 12.2. CPT0MD: Comparator0 Mode Selection .....	68
SFR Definition 12.3. CPT0MX: Comparator0 MUX Selection .....	70
SFR Definition 13.1. CS0CN: Capacitive Sense Control .....	75
SFR Definition 13.2. CS0CF: Capacitive Sense Configuration .....	76
SFR Definition 13.3. CS0DH: Capacitive Sense Data High Byte .....	77
SFR Definition 13.4. CS0DL: Capacitive Sense Data Low Byte .....	77
SFR Definition 13.5. CS0SS: Capacitive Sense Auto-Scan Start Channel .....	78
SFR Definition 13.6. CS0SE: Capacitive Sense Auto-Scan End Channel .....	78
SFR Definition 13.7. CS0THH: Capacitive Sense Comparator Threshold High Byte ...	79
SFR Definition 13.8. CS0THL: Capacitive Sense Comparator Threshold Low Byte ....	79
SFR Definition 13.9. CS0MX: Capacitive Sense Mux Channel Select .....	81
SFR Definition 14.1. DPL: Data Pointer Low Byte .....	88
SFR Definition 14.2. DPH: Data Pointer High Byte .....	88
SFR Definition 14.3. SP: Stack Pointer .....	89
SFR Definition 14.4. ACC: Accumulator .....	89
SFR Definition 14.5. B: B Register .....	90
SFR Definition 14.6. PSW: Program Status Word .....	91
SFR Definition 16.1. HWID: Hardware Identification Byte .....	95
SFR Definition 16.2. DERIVID: Derivative Identification Byte .....	96
SFR Definition 16.3. REVID: Hardware Revision Identification Byte .....	96
SFR Definition 18.1. IE: Interrupt Enable .....	105
SFR Definition 18.2. IP: Interrupt Priority .....	106
SFR Definition 18.3. EIE1: Extended Interrupt Enable 1 .....	107
SFR Definition 18.4. EIE2: Extended Interrupt Enable 2 .....	108
SFR Definition 18.5. EIP1: Extended Interrupt Priority 1 .....	109
SFR Definition 18.6. EIP2: Extended Interrupt Priority 2 .....	110
SFR Definition 18.7. IT01CF: INT0/INT1 Configuration .....	112
SFR Definition 19.1. PSCTL: Program Store R/W Control .....	118
SFR Definition 19.2. FLKEY: Flash Lock and Key .....	119
SFR Definition 20.1. PCON: Power Control .....	122
SFR Definition 21.1. VDM0CN: VDD Monitor Control .....	126

# C8051F80x-83x

---

SFR Definition 21.2. RSTSRC: Reset Source .....	128
SFR Definition 22.1. CLKSEL: Clock Select .....	130
SFR Definition 22.2. OSCICL: Internal H-F Oscillator Calibration .....	131
SFR Definition 22.3. OSCICN: Internal H-F Oscillator Control .....	132
SFR Definition 22.4. OSCXCN: External Oscillator Control .....	134
SFR Definition 23.1. XBR0: Port I/O Crossbar Register 0 .....	148
SFR Definition 23.2. XBR1: Port I/O Crossbar Register 1 .....	149
SFR Definition 23.3. P0MASK: Port 0 Mask Register .....	151
SFR Definition 23.4. P0MAT: Port 0 Match Register .....	151
SFR Definition 23.5. P1MASK: Port 1 Mask Register .....	152
SFR Definition 23.6. P1MAT: Port 1 Match Register .....	152
SFR Definition 23.7. P0: Port 0 .....	153
SFR Definition 23.8. P0MDIN: Port 0 Input Mode .....	154
SFR Definition 23.9. P0MDOUT: Port 0 Output Mode .....	154
SFR Definition 23.10. P0SKIP: Port 0 Skip .....	155
SFR Definition 23.11. P1: Port 1 .....	155
SFR Definition 23.12. P1MDIN: Port 1 Input Mode .....	156
SFR Definition 23.13. P1MDOUT: Port 1 Output Mode .....	156
SFR Definition 23.14. P1SKIP: Port 1 Skip .....	157
SFR Definition 23.15. P2: Port 2 .....	157
SFR Definition 23.16. P2MDOUT: Port 2 Output Mode .....	158
SFR Definition 24.1. CRC0CN: CRC0 Control .....	163
SFR Definition 24.2. CRC0IN: CRC Data Input .....	164
SFR Definition 24.3. CRC0DATA: CRC Data Output .....	164
SFR Definition 24.4. CRC0AUTO: CRC Automatic Control .....	165
SFR Definition 24.5. CRC0CNT: CRC Automatic Flash Sector Count .....	165
SFR Definition 24.6. CRC0FLIP: CRC Bit Flip .....	166
SFR Definition 25.1. SPI0CFG: SPI0 Configuration .....	174
SFR Definition 25.2. SPI0CN: SPI0 Control .....	175
SFR Definition 25.3. SPI0CKR: SPI0 Clock Rate .....	176
SFR Definition 25.4. SPI0DAT: SPI0 Data .....	176
SFR Definition 26.1. SMB0CF: SMBus Clock/Configuration .....	186
SFR Definition 26.2. SMB0CN: SMBus Control .....	188
SFR Definition 26.3. SMB0ADR: SMBus Slave Address .....	191
SFR Definition 26.4. SMB0ADM: SMBus Slave Address Mask .....	191
SFR Definition 26.5. SMB0DAT: SMBus Data .....	192
SFR Definition 27.1. SCON0: Serial Port 0 Control .....	206
SFR Definition 27.2. SBUF0: Serial (UART0) Port Data Buffer .....	207
SFR Definition 28.1. CKCON: Clock Control .....	210
SFR Definition 28.2. TCON: Timer Control .....	215
SFR Definition 28.3. TMOD: Timer Mode .....	216
SFR Definition 28.4. TL0: Timer 0 Low Byte .....	217
SFR Definition 28.5. TL1: Timer 1 Low Byte .....	217
SFR Definition 28.6. TH0: Timer 0 High Byte .....	218
SFR Definition 28.7. TH1: Timer 1 High Byte .....	218

---

---

SFR Definition 28.8. TMR2CN: Timer 2 Control .....	222
SFR Definition 28.9. TMR2RLL: Timer 2 Reload Register Low Byte .....	223
SFR Definition 28.10. TMR2RLH: Timer 2 Reload Register High Byte .....	223
SFR Definition 28.11. TMR2L: Timer 2 Low Byte .....	224
SFR Definition 28.12. TMR2H: Timer 2 High Byte .....	224
SFR Definition 29.1. PCA0CN: PCA0 Control .....	238
SFR Definition 29.2. PCA0MD: PCA0 Mode .....	239
SFR Definition 29.3. PCA0PWM: PCA0 PWM Configuration .....	240
SFR Definition 29.4. PCA0CPMn: PCA0 Capture/Compare Mode .....	241
SFR Definition 29.5. PCA0L: PCA0 Counter/Timer Low Byte .....	242
SFR Definition 29.6. PCA0H: PCA0 Counter/Timer High Byte .....	242
SFR Definition 29.7. PCA0CPLn: PCA0 Capture Module Low Byte .....	243
SFR Definition 29.8. PCA0CPHn: PCA0 Capture Module High Byte .....	243
C2 Register Definition 30.1. C2ADD: C2 Address .....	244
C2 Register Definition 30.3. REVID: C2 Revision ID .....	245
C2 Register Definition 30.2. DEVICEID: C2 Device ID .....	245
C2 Register Definition 30.4. FPCTL: C2 Flash Programming Control .....	246
C2 Register Definition 30.5. FPDAT: C2 Flash Programming Data .....	246

---

## 1. System Overview

C8051F80x-83x devices are fully integrated, mixed-signal, system-on-a-chip capacitive sensing MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- Capacitive sense interface with 16 input channels
- 10-bit 500 ksps single-ended ADC with 16-channel analog multiplexer and integrated temperature sensor
- Precision calibrated 24.5 MHz internal oscillator
- 16 kb of on-chip Flash memory
- 512 bytes of on-chip RAM
- SMBus/I<sup>2</sup>C, Enhanced UART, and Enhanced SPI serial interfaces implemented in hardware
- Three general-purpose 16-bit timers
- Programmable counter/timer array (PCA) with three capture/compare modules
- On-chip internal voltage reference
- On-chip Watchdog timer
- On-chip power-on reset and supply monitor
- On-chip voltage comparator
- 17 general purpose I/O

With on-chip power-on reset,  $V_{DD}$  monitor, watchdog timer, and clock oscillator, the C8051F80x-83x devices are truly stand-alone, system-on-a-chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The C8051F80x-83x processors include Silicon Laboratories' 2-Wire C2 Debug and Programming interface, which allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection of memory, viewing and modification of special function registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 1.8–3.6 V operation over the industrial temperature range (–45 to +85 °C). An internal LDO regulator is used to supply the processor core voltage at 1.8 V. The Port I/O and  $\overline{RST}$  pins are tolerant of input signals up to 5 V. See Table 2.1 for ordering information. Block diagrams of the devices in the C8051F80x-83x family are shown in Figure 1.1 through Figure 1.9.



# C8051F80x-83x

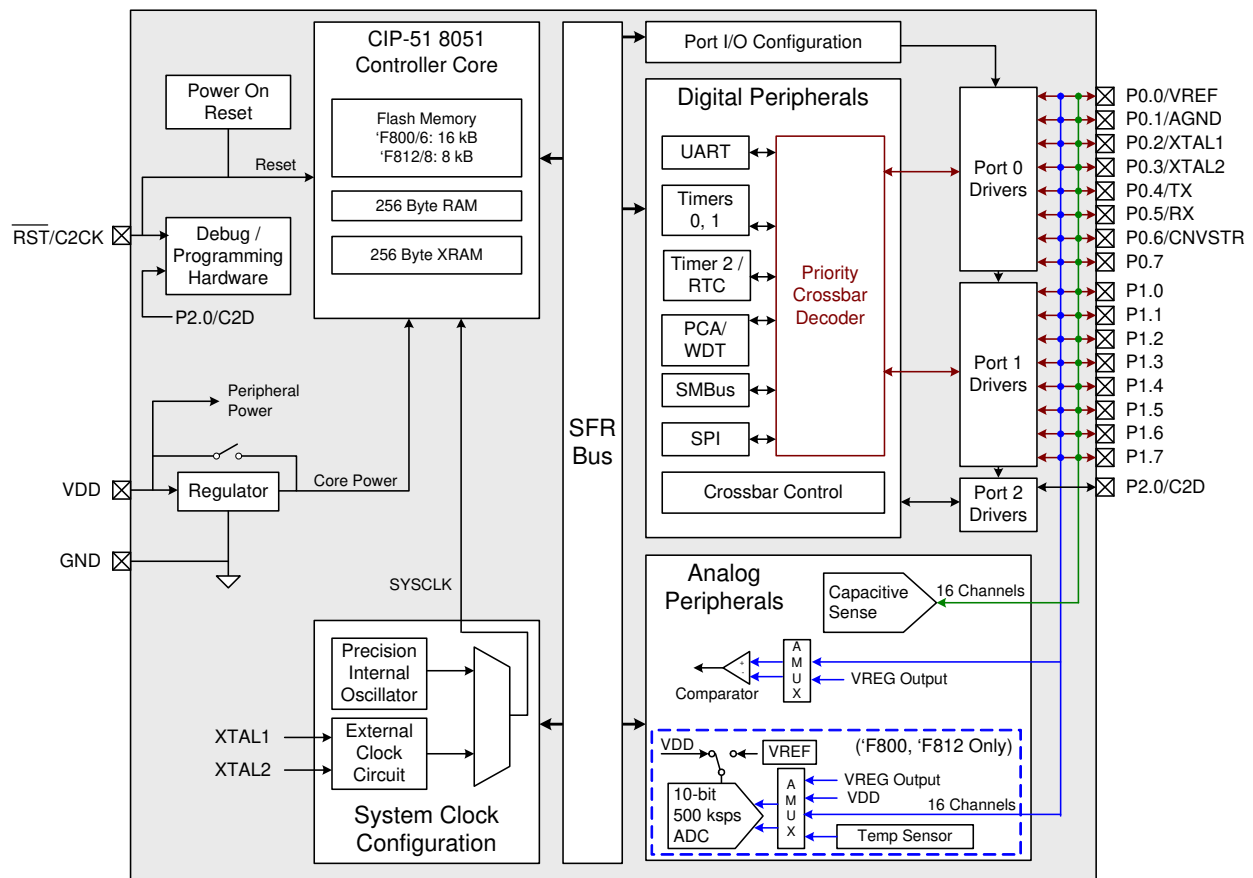


Figure 1.1. C8051F800, C8051F806, C8051F812, C8051F818 Block Diagram

# C8051F80x-83x

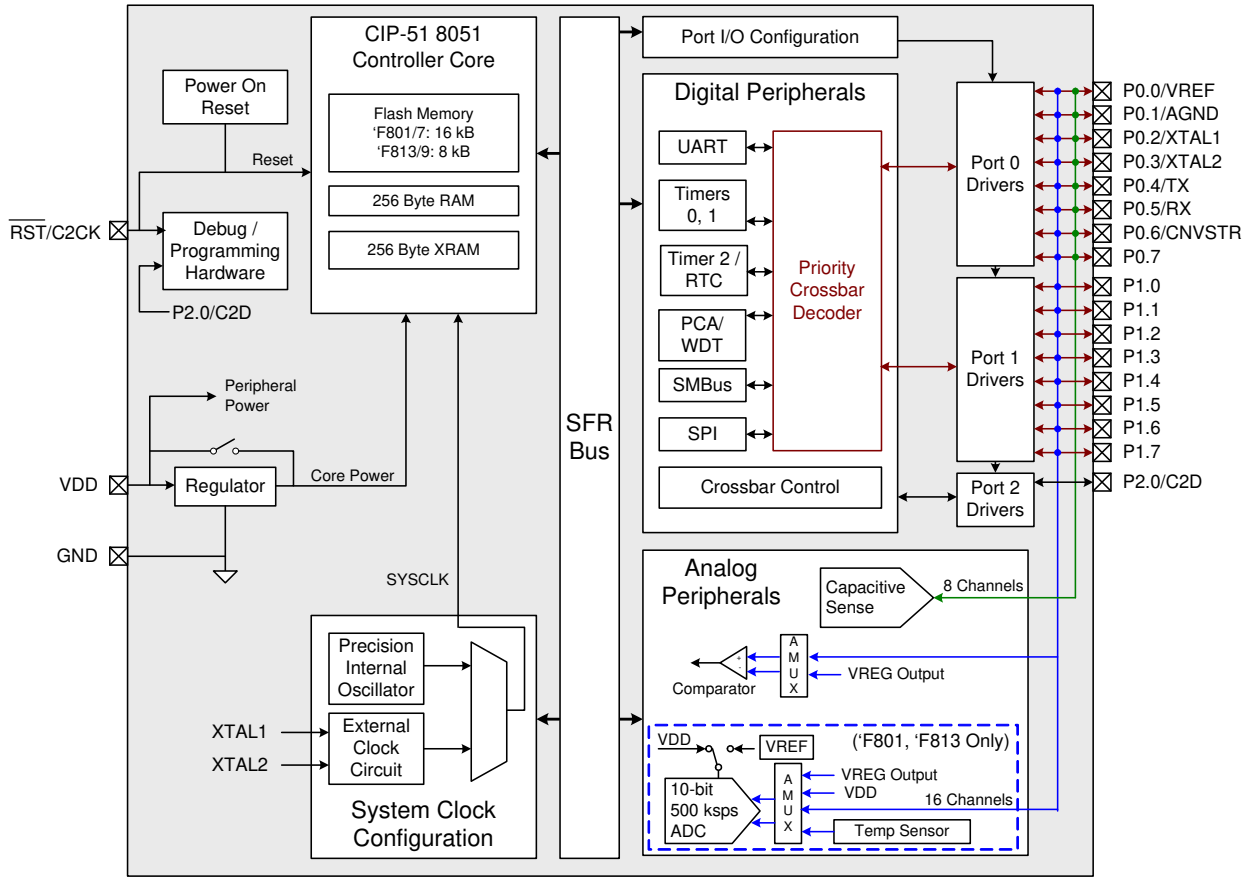


Figure 1.2. C8051F801, C8051F807, C8051F813, C8051F819 Block Diagram

# C8051F80x-83x

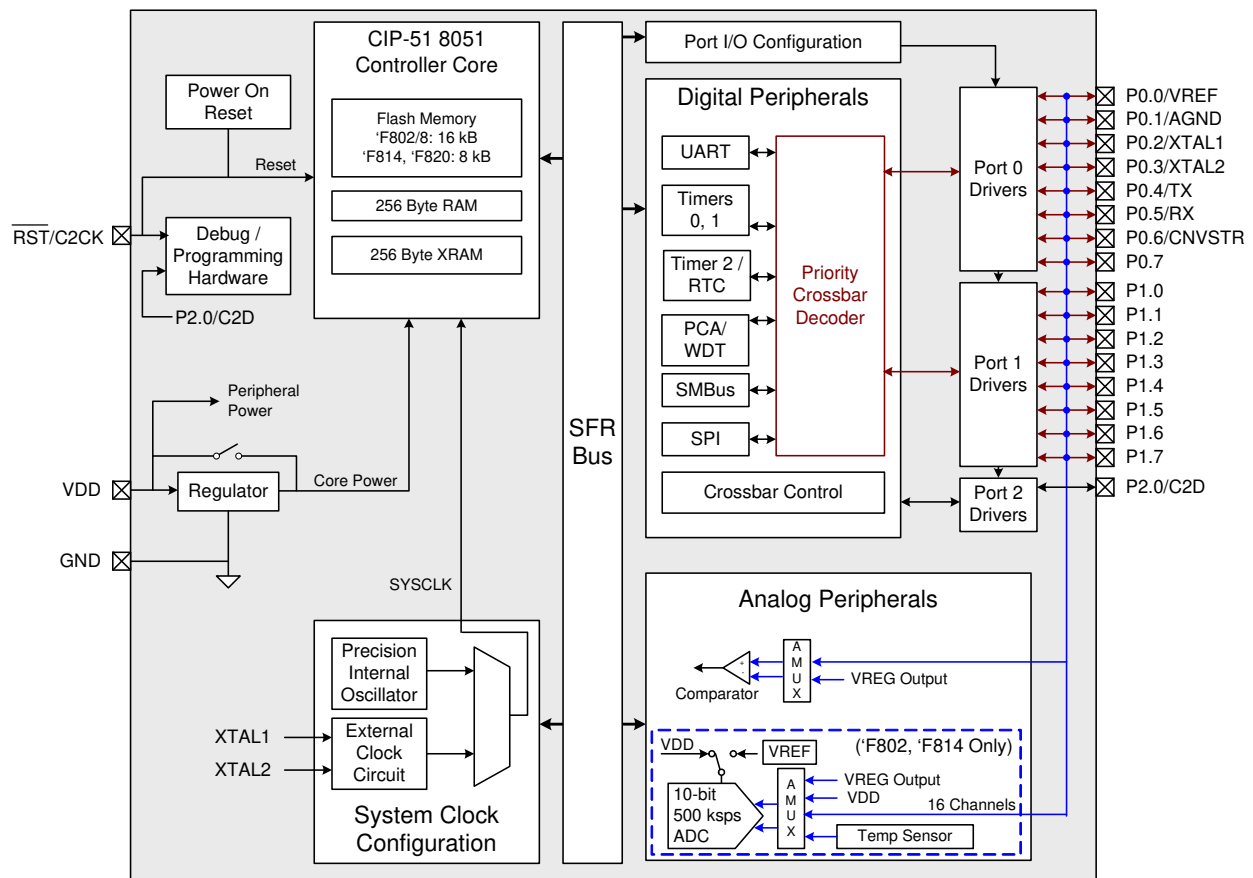


Figure 1.3. C8051F802, C8051F808, C8051F814, C8051F820 Block Diagram

# C8051F80x-83x

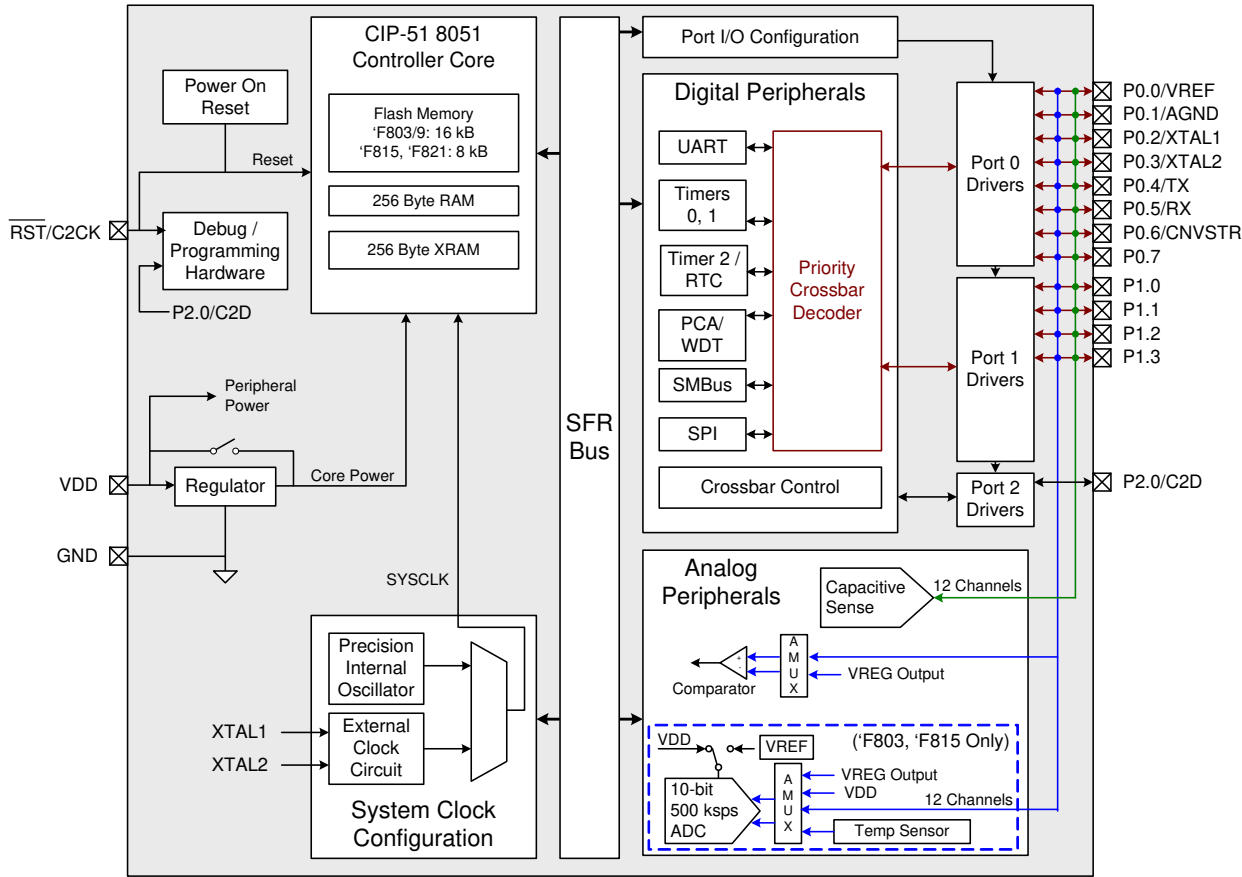


Figure 1.4. C8051F803, C8051F809, C8051F815, C8051F821 Block Diagram

# C8051F80x-83x

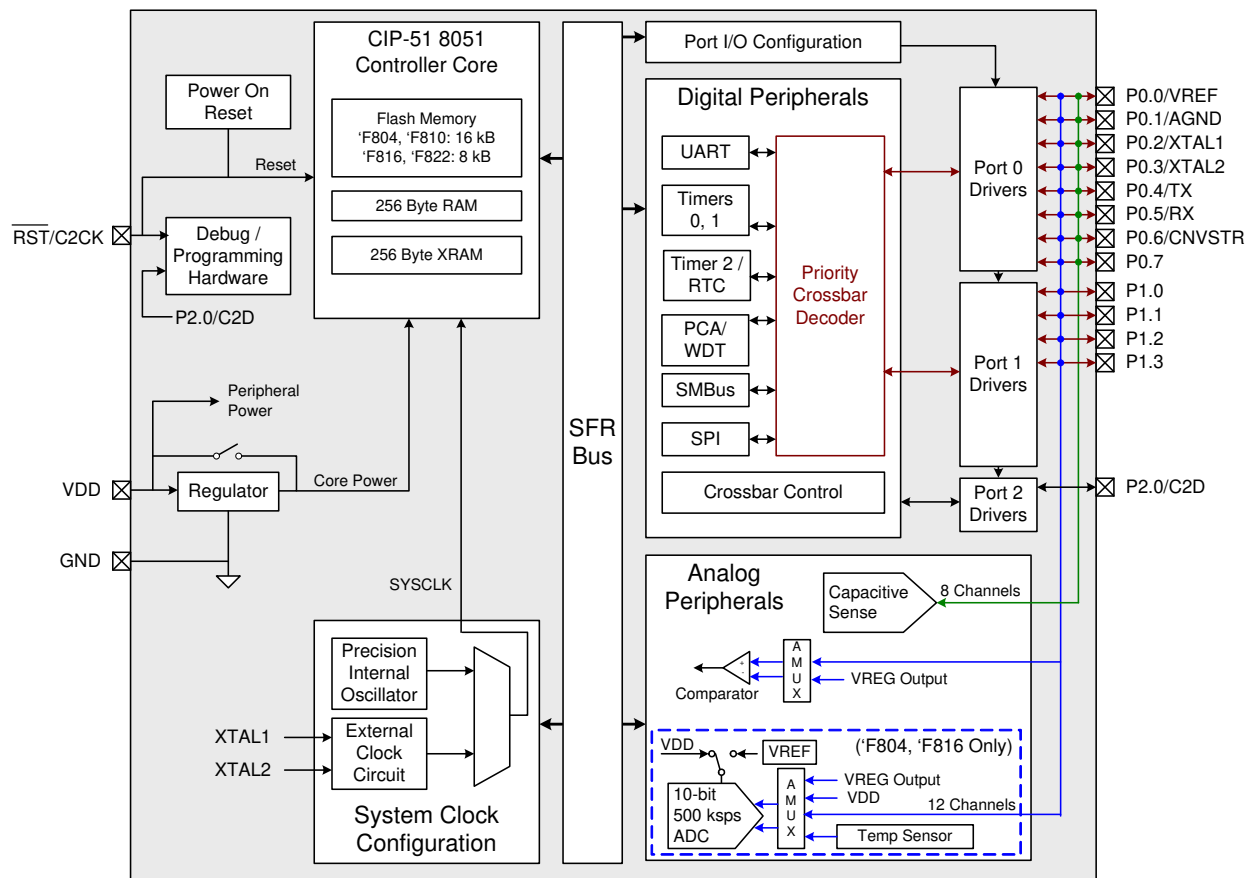


Figure 1.5. C8051F804, C8051F810, C8051F816, C8051F822 Block Diagram

# C8051F80x-83x

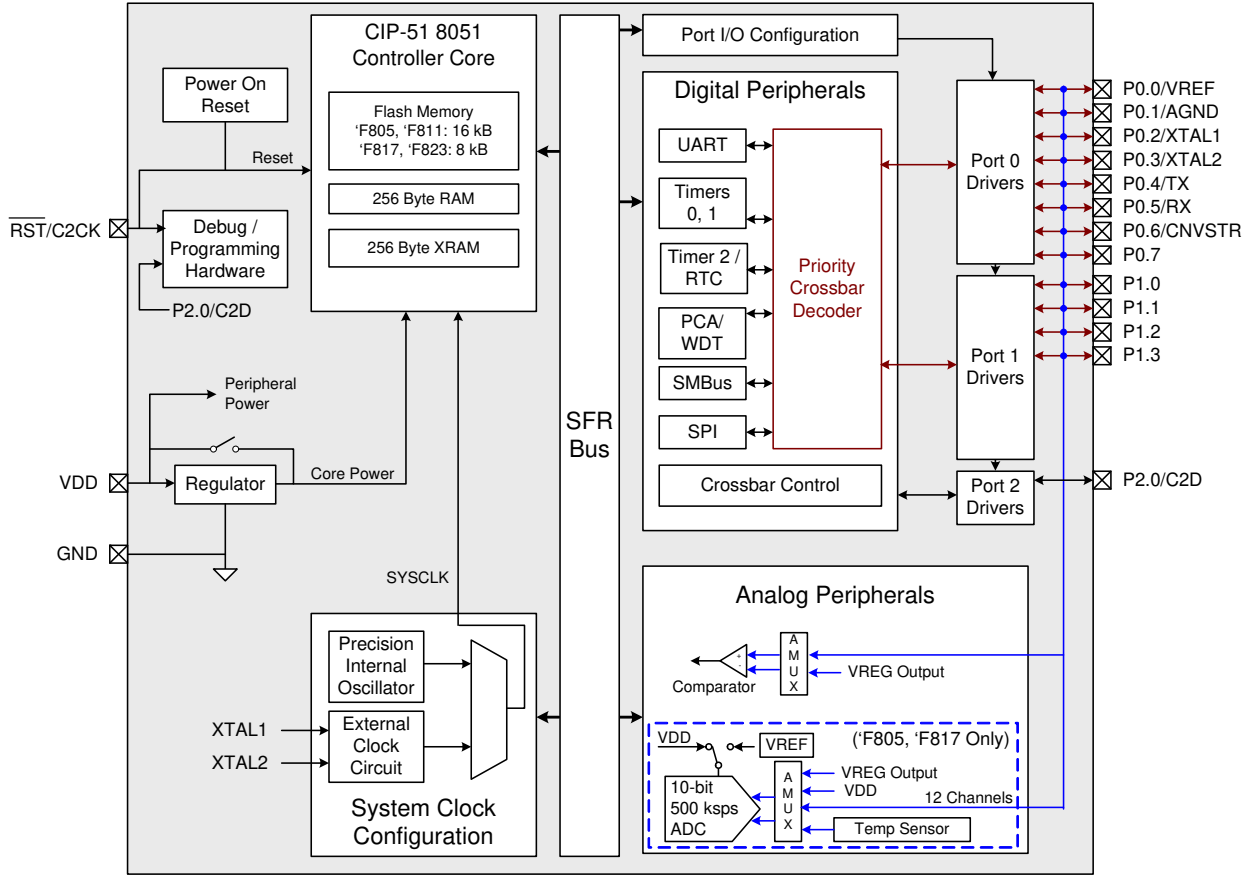


Figure 1.6. C8051F805, C8051F811, C8051F817, C8051F823 Block Diagram

# C8051F80x-83x

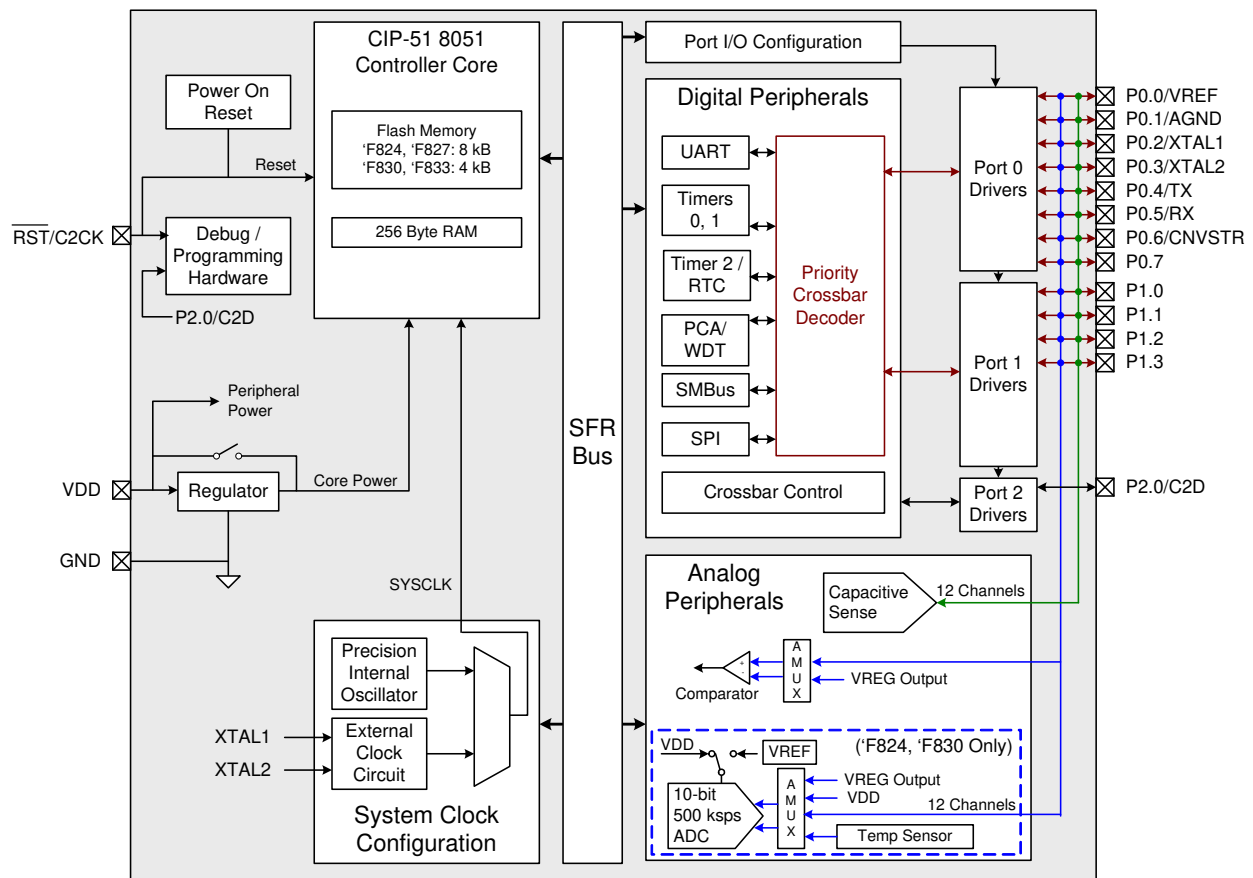


Figure 1.7. C8051F824, C8051F827, C8051F830, C8051F833 Block Diagram

# C8051F80x-83x

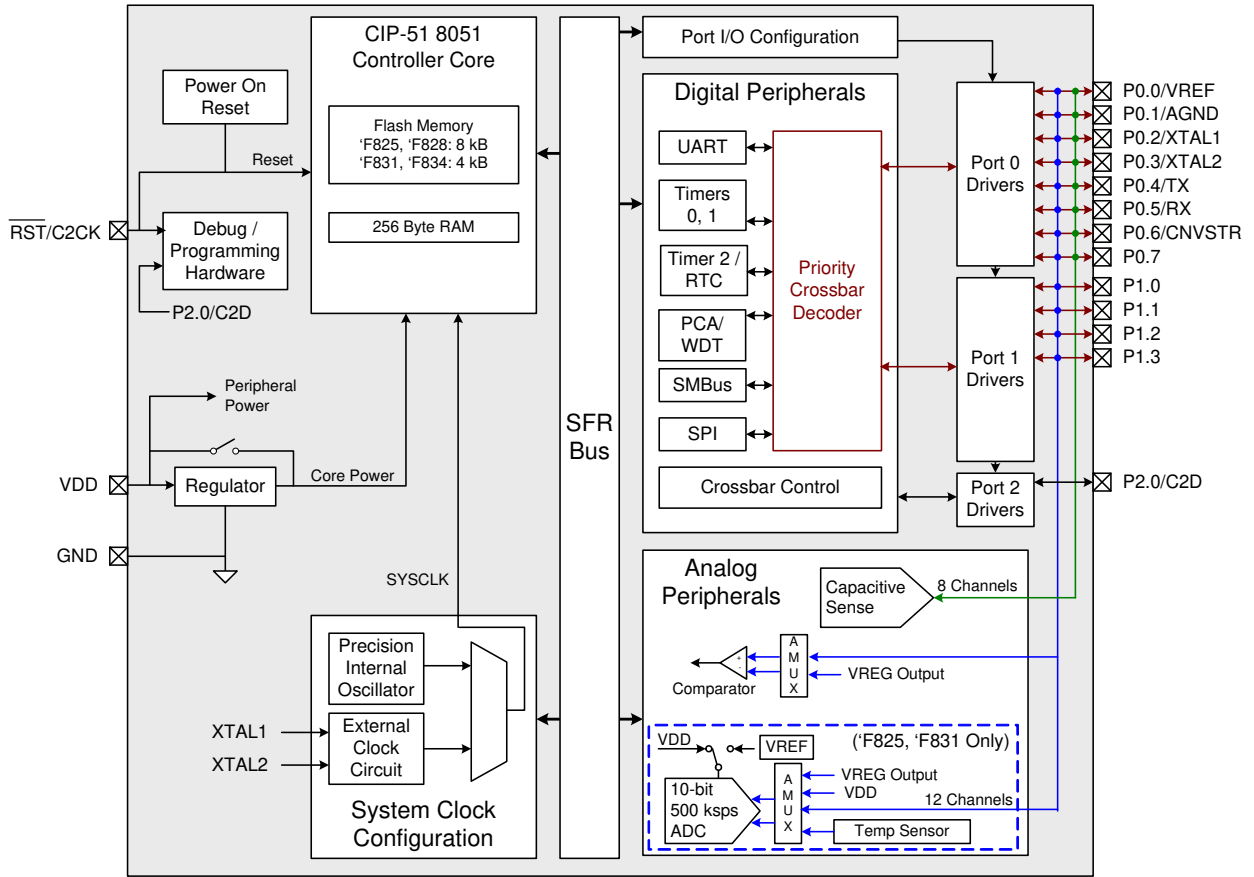


Figure 1.8. C8051F825, C8051F828, C8051F831, C8051F834 Block Diagram



# C8051F80x-83x

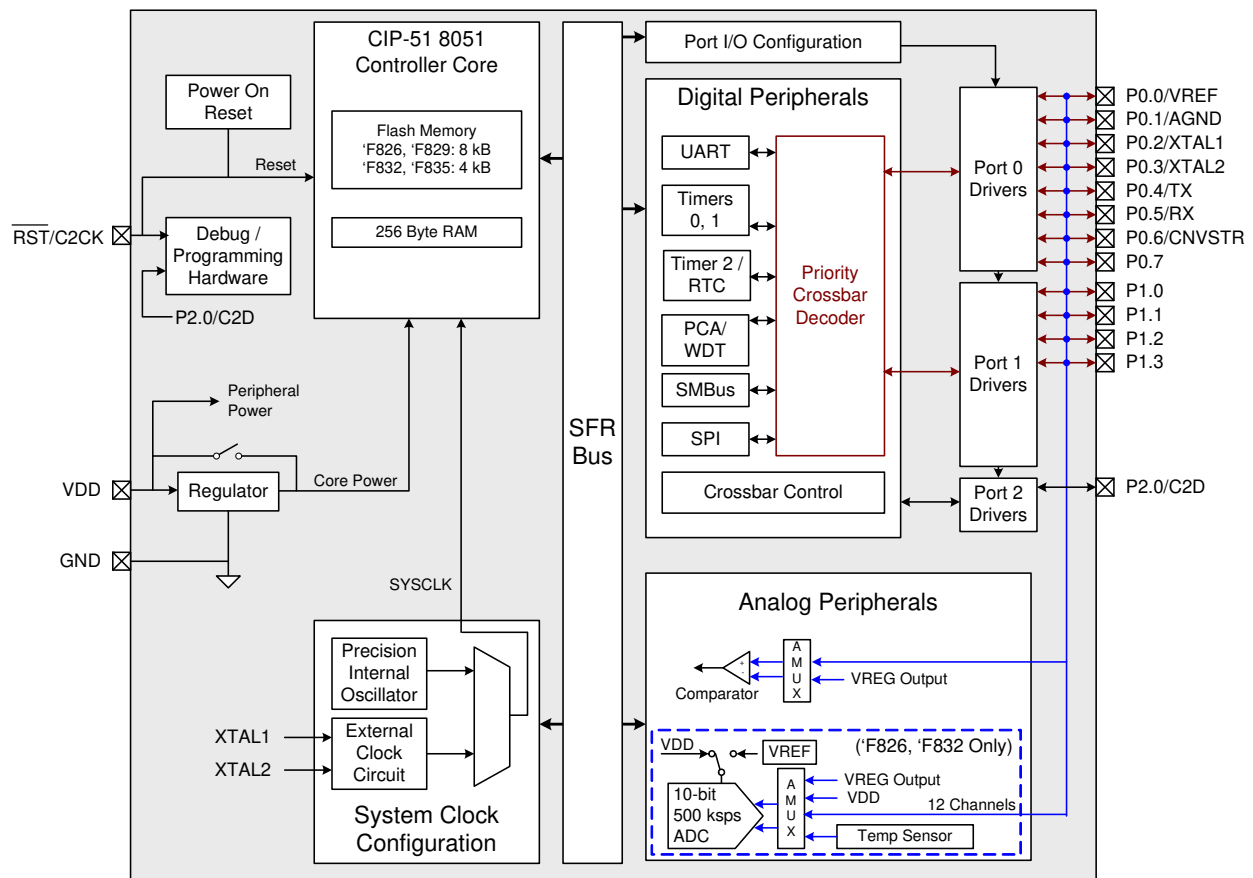


Figure 1.9. C8051F826, C8051F829, C8051F832, C8051F835 Block Diagram

## 2. Ordering Information

All C8051F80x-83x devices have the following features:

- 25 MIPS (Peak)
- Calibrated Internal Oscillator
- SMBus/I2C
- Enhanced SPI
- UART
- Programmable counter array (3 channels)
- 3 Timers (16-bit)
- 1 Comparator
- Pb-Free (RoHS compliant) package

In addition to the features listed above, each device in the C8051F80x-83x family has a set of features that vary across the product line. See Table 2.1 for a complete list of the unique feature sets for each device in the family.