Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

C8051F85x/86x

Low-Cost 8-bit MCU Family with up to 8 kB of Flash

Memory
- Up to 8 kB flash
- Flash is in-system programmable in 512-Byte sectors
- Up to 512 Bytes RAM (256 + 256)

On-Chip Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers

12-Bit Analog-to-Digital Converter
- Up to 16 input channels
- Up to 200 ksps 12-bit mode or 800 ksps 10-bit mode
- Internal VREF or external VREF supported

Internal Low-Power Oscillator
- Calibrated to 24.5 MHz
- Low supply current
- ±2% accuracy over supply and temperature

Internal Low-Frequency Oscillator
- 80 kHz nominal operation
- Low supply current
- Independent clock source for watchdog timer

2 Analog Comparators
- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current

General-Purpose I/O
- Up to 18 pins
- 5 V-Tolerant
- Crossbar-enabled

High-Speed CIP-51 µC Core
- Efficient, pipelined instruction architecture
- Up to 25 MIPS throughput with 25 MHz clock
- Uses standard 8051 instruction set
- Expanded interrupt handler

Communication Peripherals
- UART
- I^2C / SMBus™
- SPI™

Timer/Counters and PWM
- 4 General-Purpose 16-bit Timer/Counters
- 16-bit Programmable Counter Array (PCA) with three channels of PWM, capture/compare, or frequency output capability, and hardware kill/safe state capability

Additional Support Peripherals
- Independent watchdog timer clocked from LFO
- 16-bit CRC engine

Unique Identifier
- 32-bit unique key for each device

Supply Voltage
- 2.2 to 3.6 V

Package Options
- 16-pin SOIC
- 20-pin QFN, 3 x 3 mm
- 24-pin QSOP
- Available in die form
- Qualified to AEC-Q100 Standards

Temperature Ranges:
- –40 to +125 °C (-Ix) and –40 to +85 °C (-Gx)

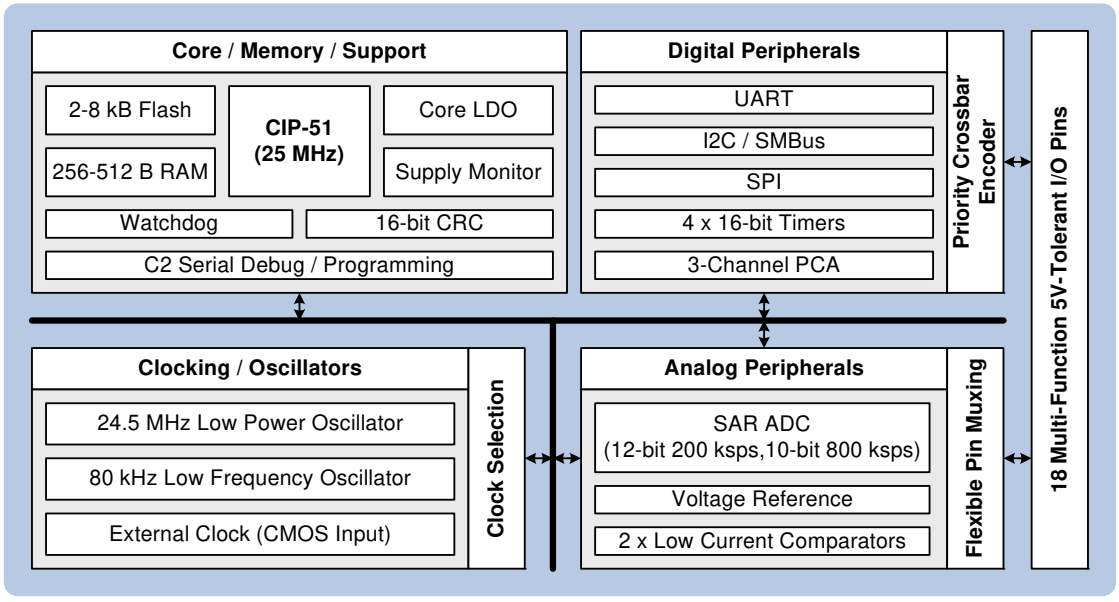

Table of Contents

1. Electrical Specifications 8
1.1. Electrical Characteristics 8
1.2. Typical Performance Curves 19
1.2.1. Operating Supply Current 19
1.2.2. ADC Supply Current 20
1.2.3. Port I/O Output Drive 21
1.3. Thermal Conditions 21
1.4. Absolute Maximum Ratings 22
2. System Overview 23
2.1. Power 25
2.1.1. LDO 25
2.1.2. Voltage Supply Monitor (VMON0) 25
2.1.3. Device Power Modes 25
2.2. I/O 26
2.2.1. General Features 26
2.2.2. Crossbar 26
2.3. Clocking 27
2.4. Counters/Timers and PWM 27
2.4.1. Programmable Counter Array (PCA0) 27
2.4.2. Timers (Timer 0, Timer 1, Timer 2 and Timer 3) 27
2.4.3. Watchdog Timer (WDT0) 27
2.5. Communications and other Digital Peripherals 28
2.5.1. Universal Asynchronous Receiver/Transmitter (UART0) 28
2.5.2. Serial Peripheral Interface (SPI0) 28
2.5.3. System Management Bus / I2C (SMBus0) 28
2.5.4. 16/32-bit CRC (CRC0) 28
2.6. Analog Peripherals 30
2.6.1. 12-Bit Analog-to-Digital Converter (ADC0) 30
2.6.2. Low Current Comparators (CMP0, CMP1) 30
2.7. Reset Sources 31
2.8. On-Chip Debugging 31
3. Pin Definitions 32
3.1. C8051F850/1/2/3/4/5 QSOP24 Pin Definitions 32
3.2. C8051F850/1/2/3/4/5 QFN20 Pin Definitions 36
3.3. C8051F860/1/2/3/4/5 SOIC16 Pin Definitions 39
4. Ordering Information 42
5. QSOP-24 Package Specifications 45
6. QFN-20 Package Specifications 47
7. SOIC-16 Package Specifications 50
8. Memory Organization 52
8.1. Program Memory 53
8.1.1. MOVX Instruction and Program Memory 53
8.2. Data Memory 53

8.2.1. Internal RAM 53
8.2.2. External RAM 54
8.2.3. Special Function Registers 55
9. Special Function Register Memory Map 56
10. Flash Memory 61
10.1. Security Options 61
10.2. Programming the Flash Memory 63
10.2.1. Flash Lock and Key Functions 63
10.2.2. Flash Erase Procedure 63
10.2.3. Flash Write Procedure 63
10.3. Non-Volatile Data Storage 64
10.4. Flash Write and Erase Guidelines 64
10.4.1. Voltage Supply Maintenance and the Supply Monitor 64
10.4.2. PSWE Maintenance 65
10.4.3. System Clock 65
10.5. Flash Control Registers 66
11. Device Identification and Unique Identifier 68
11.1. Device Identification Registers 69
12. Interrupts 72
12.1. MCU Interrupt Sources and Vectors 72
12.1.1. Interrupt Priorities 72
12.1.2. Interrupt Latency 72
12.2. Interrupt Control Registers 75
13. Power Management and Internal Regulator 82
13.1. Power Modes 82
13.1.1. Idle Mode 82
13.1.2. Stop Mode 83
13.2. LDO Regulator 83
13.3. Power Control Registers 83
13.4. LDO Control Registers 84
14. Analog-to-Digital Converter (ADC0) 85
14.1. ADC0 Analog Multiplexer 86
14.2. ADC Operation 88
14.2.1. Starting a Conversion 88
14.2.2. Tracking Modes 88
14.2.3. Burst Mode 89
14.2.4. Settling Time Requirements 90
14.2.5. Gain Setting 91
14.3. 8-Bit Mode 91
14.4. 12-Bit Mode 91
14.5. Power Considerations 92
14.6. Output Code Formatting 94
14.7. Programmable Window Detector 95
14.7.1. Window Detector In Single-Ended Mode 95
14.8. Voltage and Ground Reference Options 97

14.8.1. External Voltage Reference 97
14.8.2. Internal Voltage Reference 97
14.8.3. Analog Ground Reference 97
14.9. Temperature Sensor 98
14.9.1. Calibration 98
14.10. ADC Control Registers 99
15. CIP-51 Microcontroller Core 113
15.1. Performance 113
15.2. Programming and Debugging Support 114
15.3. Instruction Set 114
15.3.1. Instruction and CPU Timing 114
15.4. CPU Core Registers 119
16. Clock Sources and Selection (HFOSC0, LFOSC0, and EXTCLK) 125
16.1. Programmable High-Frequency Oscillator 125
16.2. Programmable Low-Frequency Oscillator 125
16.2.1. Calibrating the Internal L-F Oscillator 125
16.3. External Clock 126
16.4. Clock Selection 126
16.5. High Frequency Oscillator Control Registers 127
16.6. Low Frequency Oscillator Control Registers 128
16.7. Clock Selection Control Registers 129
17. Comparators (CMP0 and CMP1) 130
17.1. System Connectivity 130
17.2. Functional Description 133
17.3. Comparator Control Registers 134
18. Cyclic Redundancy Check Unit (CRC0) 140
18.1. CRC Algorithm 140
18.2. Preparing for a CRC Calculation 142
18.3. Performing a CRC Calculation 142
18.4. Accessing the CRC0 Result 142
18.5. CRC0 Bit Reverse Feature 142
18.6. CRC Control Registers 143
19. External Interrupts (INT0 and INT1) 149
19.1. External Interrupt Control Registers 150
20. Programmable Counter Array (PCA0) 152
20.1. PCA Counter/Timer 153
20.2. PCA0 Interrupt Sources 153
20.3. Capture/Compare Modules 154
20.3.1. Output Polarity 154
20.3.2. Edge-Triggered Capture Mode 155
20.3.3. Software Timer (Compare) Mode 156
20.3.4. High-Speed Output Mode 157
20.3.5. Frequency Output Mode 158
20.4. PWM Waveform Generation 159
20.4.1. Edge Aligned PWM 159

20.4.2. Center Aligned PWM 161
20.4.3. 8 to11-bit Pulse Width Modulator Modes 163
20.4.4. 16-Bit Pulse Width Modulator Mode 164
20.5. Comparator Clear Function 165
20.6. PCA Control Registers 167
21. Port I/O (Port 0, Port 1, Port 2, Crossbar, and Port Match) 184
21.1. General Port I/O Initialization 185
21.2. Assigning Port I/O Pins to Analog and Digital Functions 186
21.2.1. Assigning Port I/O Pins to Analog Functions 186
21.2.2. Assigning Port I/O Pins to Digital Functions 186
21.2.3. Assigning Port I/O Pins to Fixed Digital Functions 187
21.3. Priority Crossbar Decoder 188
21.4. Port I/O Modes of Operation 191
21.4.1. Configuring Port Pins For Analog Modes 191
21.4.2. Configuring Port Pins For Digital Modes 191
21.4.3. Port Drive Strength 192
21.5. Port Match 192
21.6. Direct Read/Write Access to Port I/O Pins 192
21.7. Port I/O and Pin Configuration Control Registers 193
22. Reset Sources and Supply Monitor 211
22.1. Power-On Reset 212
22.2. Power-Fail Reset / Supply Monitor 213
22.3. Enabling the VDD Monitor 213
22.4. External Reset 214
22.5. Missing Clock Detector Reset 214
22.6. Comparator0 Reset 214
22.7. Watchdog Timer Reset 214
22.8. Flash Error Reset 214
22.9. Software Reset 214
22.10. Reset Sources Control Registers 215
22.11. Supply Monitor Control Registers 216
23. Serial Peripheral Interface (SPI0) 217
23.1. Signal Descriptions 218
23.1.1. Master Out, Slave In (MOSI) 218
23.1.2. Master In, Slave Out (MISO) 218
23.1.3. Serial Clock (SCK) 218
23.1.4. Slave Select (NSS) 218
23.2. SPI0 Master Mode Operation 219
23.3. SPI0 Slave Mode Operation 221
23.4. SPI0 Interrupt Sources 221
23.5. Serial Clock Phase and Polarity 221
23.6. SPI Special Function Registers 223
23.7. SPI Control Registers 227
24. System Management Bus / I2C (SMBus0) 233
24.1. Supporting Documents 234

24.2. SMBus Configuration 234
24.3. SMBus Operation 234
24.3.1. Transmitter vs. Receiver 235
24.3.2. Arbitration 235
24.3.3. Clock Low Extension 235
24.3.4. SCL Low Timeout 235
24.3.5. SCL High (SMBus Free) Timeout 236
24.4. Using the SMBus 236
24.4.1. SMBus Configuration Register 236
24.4.2. SMBus Pin Swap 238
24.4.3. SMBus Timing Control 238
24.4.4. SMB0CN Control Register 238
24.4.5. Hardware Slave Address Recognition 240
24.4.6. Data Register 241
24.5. SMBus Transfer Modes 242
24.5.1. Write Sequence (Master) 242
24.5.2. Read Sequence (Master) 243
24.5.3. Write Sequence (Slave) 244
24.5.4. Read Sequence (Slave) 245
24.6. SMBus Status Decoding 245
24.7. I2C / SMBus Control Registers 251
25. Timers (Timer0, Timer1, Timer2 and Timer3) 259
25.1. Timer 0 and Timer 1 261
25.1.1. Mode 0: 13-bit Counter/Timer 262
25.1.2. Mode 1: 16-bit Counter/Timer 263
25.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload 264
25.1.4. Mode 3: Two 8-bit Counter/Timers (Timer 0 Only) 265
25.2. Timer 2 and Timer 3 266
25.2.1. 16-bit Timer with Auto-Reload 266
25.2.2. 8-bit Timers with Auto-Reload 267
25.2.3. Capture Mode 268
25.3. Timer Control Registers 269
26. Universal Asynchronous Receiver/Transmitter (UART0) 289
26.1. Enhanced Baud Rate Generation 289
26.2. Operational Modes 291
26.2.1. 8-Bit UART 291
26.2.2. 9-Bit UART 292
26.3. Multiprocessor Communications 293
26.4. UART Control Registers 295
27. Watchdog Timer (WDT0) 298
27.1. Enabling / Resetting the WDT 299
27.2. Disabling the WDT 299
27.3. Disabling the WDT Lockout 299
27.4. Setting the WDT Interval 299
27.5. Watchdog Timer Control Registers 300

28. Revision-Specific Behavior 301
28.1. Revision Identification 301
28.2. Temperature Sensor Offset and Slope 303
28.3. Flash Endurance 303
28.4. Latch-Up Performance 303
28.5. Unique Identifier 303
29. C2 Interface 304
29.1. C2 Pin Sharing 304
29.2. C2 Interface Registers 305
Document Change List 310
Contact Information 311

1. Electrical Specifications

1.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 1.1, unless stated otherwise.

Table 1.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		2.2	—	3.6	V
System Clock Frequency	f_{SYSCLK}		0	—	25	MHz
Operating Ambient Temperature	T_A	Commercial Grade Devices (-GM, -GS, -GU)	–40	—	85	°C
		Industrial Grade Devices (-IM, -IS, -IU)	–40	—	125	°C
Note: All voltages with respect to GND						

Table 1.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current (–Gx Devices, -40°C to +85°C)						
Normal Mode—Full speed with code executing from flash	I_{DD}	F_{SYSCLK} = 24.5 MHz[2]	—	4.45	4.85	mA
		F_{SYSCLK} = 1.53 MHz[2]	—	915	1150	µA
		F_{SYSCLK} = 80 kHz[3], T_A = 25 °C	—	250	290	µA
		F_{SYSCLK} = 80 kHz[3]	—	250	380	µA
Idle Mode—Core halted with peripherals running	I_{DD}	F_{SYSCLK} = 24.5 MHz[2]	—	2.05	2.3	mA
		F_{SYSCLK} = 1.53 MHz[2]	—	550	700	µA
		F_{SYSCLK} = 80 kHz[3], T_A = 25 °C	—	125	130	µA
		F_{SYSCLK} = 80 kHz[3]	—	125	200	µA
Stop Mode—Core halted and all clocks stopped, Supply monitor off.	I_{DD}	Internal LDO ON, T_A = 25 °C	—	105	120	µA
		Internal LDO ON	—	105	170	µA
		Internal LDO OFF	—	0.2	—	µA

Notes:
1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

Table 1.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current (–Ix Devices, -40°C to +125°C)						
Normal Mode—Full speed with code executing from flash	I_{DD}	F_{SYSCLK} = 24.5 MHz[2]	—	4.45	5.25	mA
		F_{SYSCLK} = 1.53 MHz[2]	—	915	1600	µA
		F_{SYSCLK} = 80 kHz[3], T_A = 25 °C	—	250	290	µA
		F_{SYSCLK} = 80 kHz[3]	—	250	725	µA
Idle Mode—Core halted with peripherals running	I_{DD}	F_{SYSCLK} = 24.5 MHz[2]	—	2.05	2.6	mA
		F_{SYSCLK} = 1.53 MHz[2]	—	550	1000	µA
		F_{SYSCLK} = 80 kHz[3], T_A = 25 °C	—	125	130	µA
		F_{SYSCLK} = 80 kHz[3]	—	125	550	µA
Stop Mode—Core halted and all clocks stopped, Supply monitor off.	I_{DD}	Internal LDO ON, T_A = 25 °C	—	105	120	µA
		Internal LDO ON	—	105	270	µA
		Internal LDO OFF	—	0.2	—	µA
Analog Peripheral Supply Currents (Both –Gx and –Ix Devices)						
High-Frequency Oscillator	I_{HFOSC}	Operating at 24.5 MHz, T_A = 25 °C	—	155	—	µA
Low-Frequency Oscillator	I_{LFOSC}	Operating at 80 kHz, T_A = 25 °C	—	3.5	—	µA
ADC0 Always-on[4]	I_{ADC}	800 ksps, 10-bit conversions or 200 ksps, 12-bit conversions Normal bias settings V_{DD} = 3.0 V	—	845	1200	µA
		250 ksps, 10-bit conversions or 62.5 ksps 12-bit conversions Low power bias settings V_{DD} = 3.0 V	—	425	580	µA
ADC0 Burst Mode, 10-bit single conversions, external reference	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	370	—	µA
		100 ksps, V_{DD} = 3.0 V	—	185	—	µA
		10 ksps, V_{DD} = 3.0 V	—	19	—	µA

Notes:
1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

Table 1.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	490	—	µA
		100 ksps, V_{DD} = 3.0 V	—	245	—	µA
		10 ksps, V_{DD} = 3.0 V	—	23	—	µA
ADC0 Burst Mode, 12-bit single conversions, external reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V	—	530	—	µA
		50 ksps, V_{DD} = 3.0 V	—	265	—	µA
		10 ksps, V_{DD} = 3.0 V	—	53	—	µA
ADC0 Burst Mode, 12-bit single conversions, internal reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V, Normal bias	—	950	—	µA
		50 ksps, V_{DD} = 3.0 V, Low power bias	—	420	—	µA
		10 ksps, V_{DD} = 3.0 V, Low power bias	—	85	—	µA
Internal ADC0 Reference, Always-on[5]	I_{IREF}	Normal Power Mode	—	680	790	µA
		Low Power Mode	—	160	210	µA
Temperature Sensor	I_{TSENSE}		—	75	120	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CPnMD = 11	—	0.5	—	µA
		CPnMD = 10	—	3	—	µA
		CPnMD = 01	—	10	—	µA
		CPnMD = 00	—	25	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	20	µA

Notes:
1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

Table 1.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD} Supply Monitor Threshold	V_{VDDM}		1.85	1.95	2.1	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on V_{DD}	—	1.4	—	V
		Falling Voltage on V_{DD}	0.75	—	1.36	V
V_{DD} Ramp Time	t_{RMP}	Time to $V_{DD} \geq 2.2$ V	10	—	—	µs
Reset Delay from POR	t_{POR}	Relative to $V_{DD} \geq V_{POR}$	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	39	—	µs
$\overline{RST}$ Low Time to Generate Reset	t_{RSTL}		15	—	—	µs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{SYSCLK} > 1$ MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7.5	13.5	kHz
V_{DD} Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

Table 1.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time[1,2]	t_{WRITE}	One Byte, F_{SYSCLK} = 24.5 MHz	19	20	21	µs
Erase Time[1,2]	t_{ERASE}	One Page, F_{SYSCLK} = 24.5 MHz	5.2	5.35	5.5	ms
V_{DD} Voltage During Programming[3]	V_{PROG}		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles

Notes:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. The internal High-Frequency Oscillator has a programmable output frequency using the OSCICL register, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the OSCICL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

Table 1.5. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator (24.5 MHz)						
Oscillator Frequency	f_{HFOSC}	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	PSS_{HFOSC}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{HFOSC}	V_{DD} = 3.0 V	—	40	—	ppm/°C
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	0.05	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{DD} = 3.0 V	—	65	—	ppm/°C

Table 1.6. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	25	MHz
External Input CMOS Clock High Time	t_{CMOSH}		18	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		18	—	—	ns

Table 1.7. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	200	ksps
		10 Bit Mode	—	—	800	ksps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t_{PWR}		1.2	—	—	µs
SAR Clock Frequency	f_{SAR}	High Speed Mode, Reference is 2.4 V internal	—	—	6.25	MHz
		High Speed Mode, Reference is not 2.4 V internal	—	—	12.5	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 12.25 MHz, System Clock = 24.5 MHz.		1.1		µs
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}		—	20	—	pF
Input Mux Impedance	R_{MUX}		—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range*	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±2.3	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	–1	±0.7	1.9	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB

***Note:** Absolute input pin voltage is limited by the V_{DD} supply.

Table 1.7. ADC (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset Error	E_{OFF}	12 Bit Mode, VREF = 1.65 V	–3	0	3	LSB
		10 Bit Mode, VREF = 1.65 V	–2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error	E_M	12 Bit Mode	—	±0.02	±0.1	%
		10 Bit Mode	—	±0.06	±0.24	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput, using AGND pin						
Signal-to-Noise	SNR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	71	—	dB
		10 Bit Mode	—	70	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	–79	—	dB
		10 Bit Mode	—	–74	—	dB

***Note:** Absolute input pin voltage is limited by the V_{DD} supply.

Table 1.8. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}	1.65 V Setting	1.62	1.65	1.68	V
		2.4 V Setting, $V_{DD} \geq 2.6$ V	2.35	2.4	2.45	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 800 ksps; VREF = 3.0 V	—	5	—	µA

Table 1.9. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	757	—	mV
Offset Error*	E_{OFF}	T_A = 0 °C	—	17	—	mV
Slope	M		—	2.85	—	mV/°C
Slope Error*	E_M		—	70	—	µV/°C
Linearity			—	0.5	—	°C
Turn-on Time			—	1.8	—	µs
***Note:** Represents one standard deviation from the mean.						

Table 1.10. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPnMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		–100 mV Differential	—	150	—	ns
Response Time, CPnMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.5	—	µs
		–100 mV Differential	—	3.5	—	µs
Positive Hysterisis Mode 0 (CPnMD = 00)	HYS_{CP+}	CPnHYP = 00	—	0.4	—	mV
		CPnHYP = 01	—	8	—	mV
		CPnHYP = 10	—	16	—	mV
		CPnHYP = 11	—	32	—	mV
Negative Hysterisis Mode 0 (CPnMD = 00)	HYS_{CP-}	CPnHYN = 00	—	-0.4	—	mV
		CPnHYN = 01	—	–8	—	mV
		CPnHYN = 10	—	–16	—	mV
		CPnHYN = 11	—	–32	—	mV
Positive Hysterisis Mode 1 (CPnMD = 01)	HYS_{CP+}	CPnHYP = 00	—	0.5	—	mV
		CPnHYP = 01	—	6	—	mV
		CPnHYP = 10	—	12	—	mV
		CPnHYP = 11	—	24	—	mV
Negative Hysterisis Mode 1 (CPnMD = 01)	HYS_{CP-}	CPnHYN = 00	—	-0.5	—	mV
		CPnHYN = 01	—	–6	—	mV
		CPnHYN = 10	—	–12	—	mV
		CPnHYN = 11	—	–24	—	mV
Positive Hysterisis Mode 2 (CPnMD = 10)	HYS_{CP+}	CPnHYP = 00	—	0.7	—	mV
		CPnHYP = 01	—	4.5	—	mV
		CPnHYP = 10	—	9	—	mV
		CPnHYP = 11	—	18	—	mV
Negative Hysterisis Mode 2 (CPnMD = 10)	HYS_{CP-}	CPnHYN = 00	—	-0.6	—	mV
		CPnHYN = 01	—	–4.5	—	mV
		CPnHYN = 10	—	–9	—	mV
		CPnHYN = 11	—	–18	—	mV

Table 1.10. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPnMD = 11)	HYS_{CP+}	CPnHYP = 00	—	1.5	—	mV
		CPnHYP = 01	—	4	—	mV
		CPnHYP = 10	—	8	—	mV
		CPnHYP = 11	—	16	—	mV
Negative Hysteresis Mode 3 (CPnMD = 11)	HYS_{CP-}	CPnHYN = 00	—	-1.5	—	mV
		CPnHYN = 01	—	–4	—	mV
		CPnHYN = 10	—	–8	—	mV
		CPnHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		-0.25	—	V_{DD}+0.25	V
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	70	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C

Table 1.11. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	V_{OH}	I_{OH} = –3 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (High Drive)	V_{OL}	I_{OL} = 8.5 mA	—	—	0.6	V
Output High Voltage (Low Drive)	V_{OH}	I_{OH} = –1 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (Low Drive)	V_{OL}	I_{OL} = 1.4 mA	—	—	0.6	V
Input High Voltage	V_{IH}		V_{DD} – 0.6	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current (V_{IN} = 0 V)	I_{PU}	V_{DD} = 3.6	–30	–20	–10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	GND ≤ V_{IN} ≤ V_{DD}	–1.1	—	1.1	µA
Input Leakage Current with V_{IN} above V_{DD}	I_{LK}	V_{DD} < V_{IN} < V_{DD}+2.0 V	0	5	150	µA

1.2. Typical Performance Curves

1.2.1. Operating Supply Current

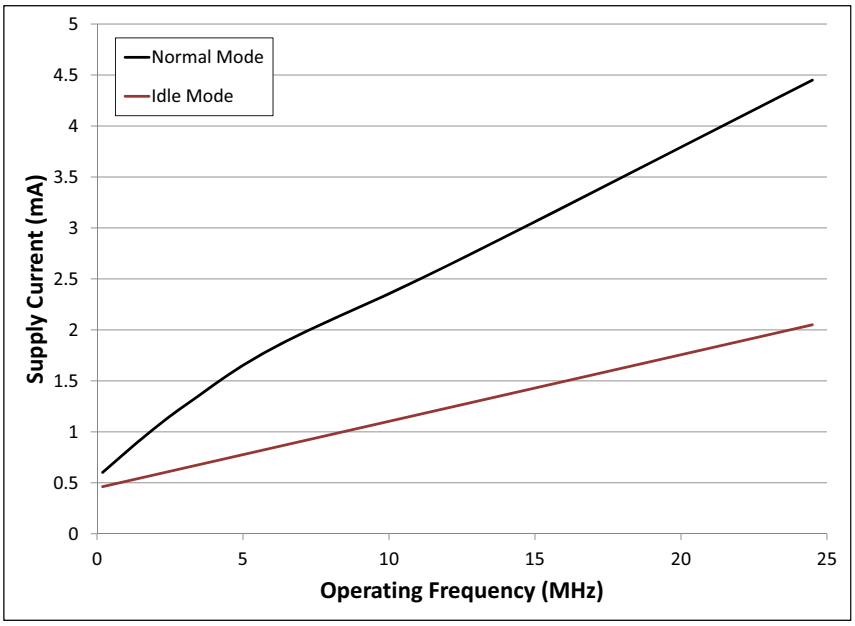

Figure 1.1. Typical Operating Current Running From 24.5 MHz Internal Oscillator

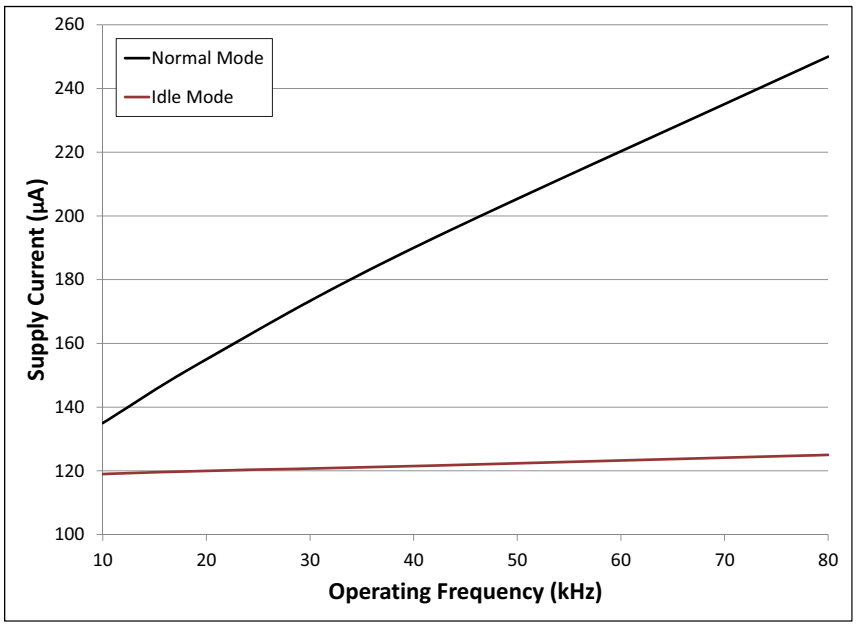

Figure 1.2. Typical Operating Current Running From 80 kHz Internal Oscillator

1.2.2. ADC Supply Current

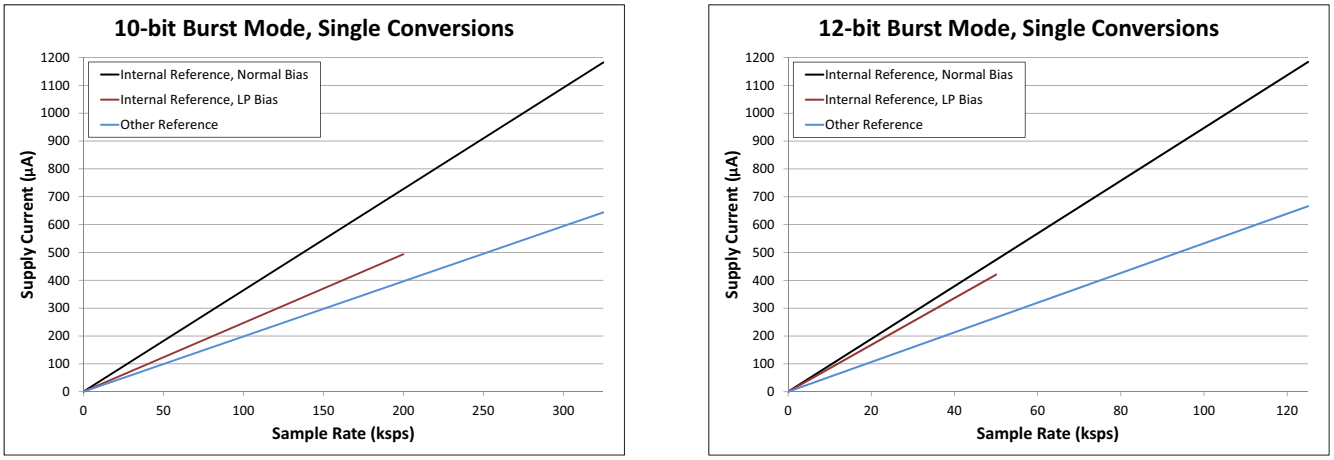

Figure 1.3. Typical ADC and Internal Reference Power Consumption in Burst Mode

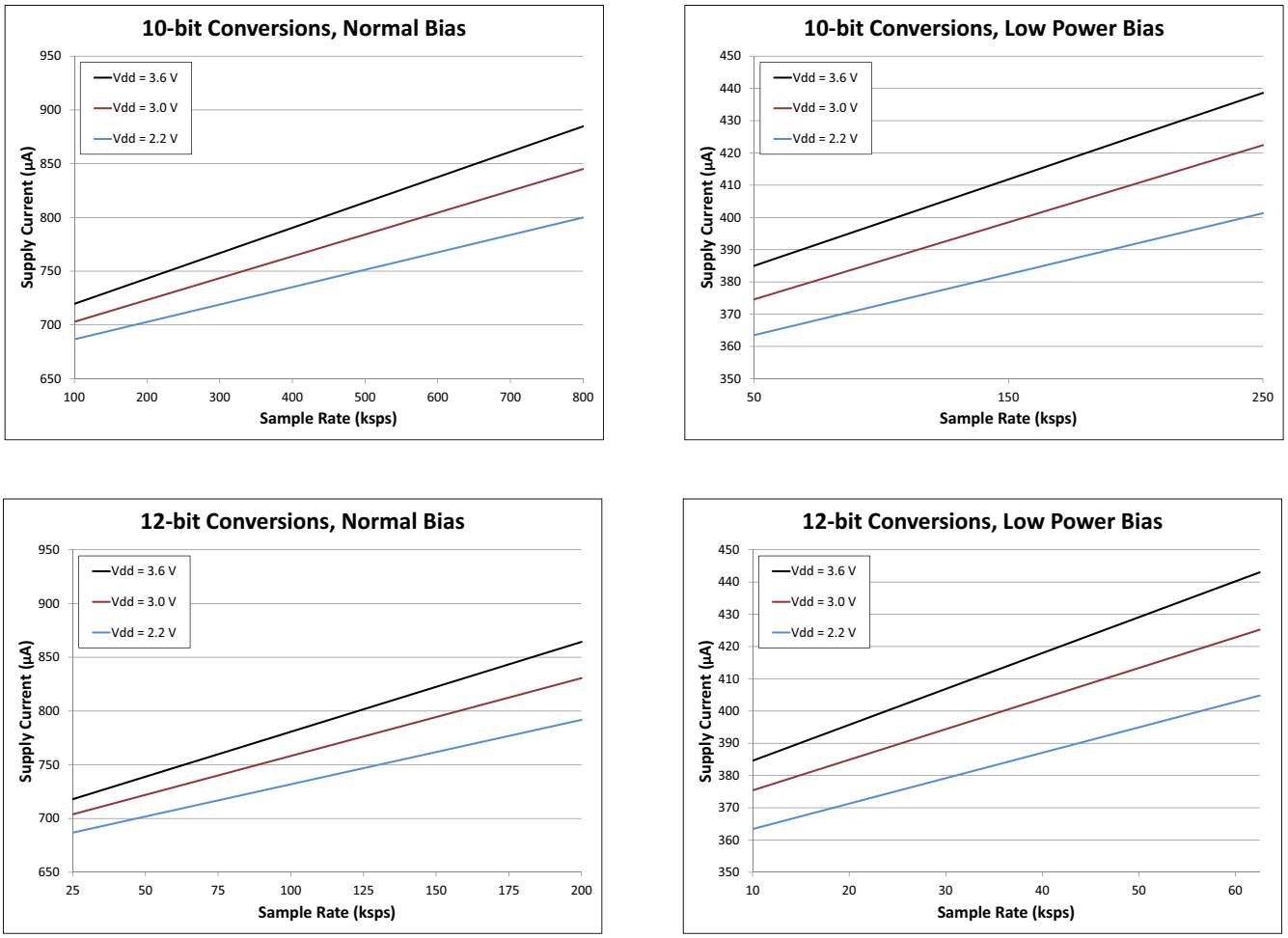

Figure 1.4. Typical ADC Power Consumption in Normal (Always-On) Mode

1.2.3. Port I/O Output Drive

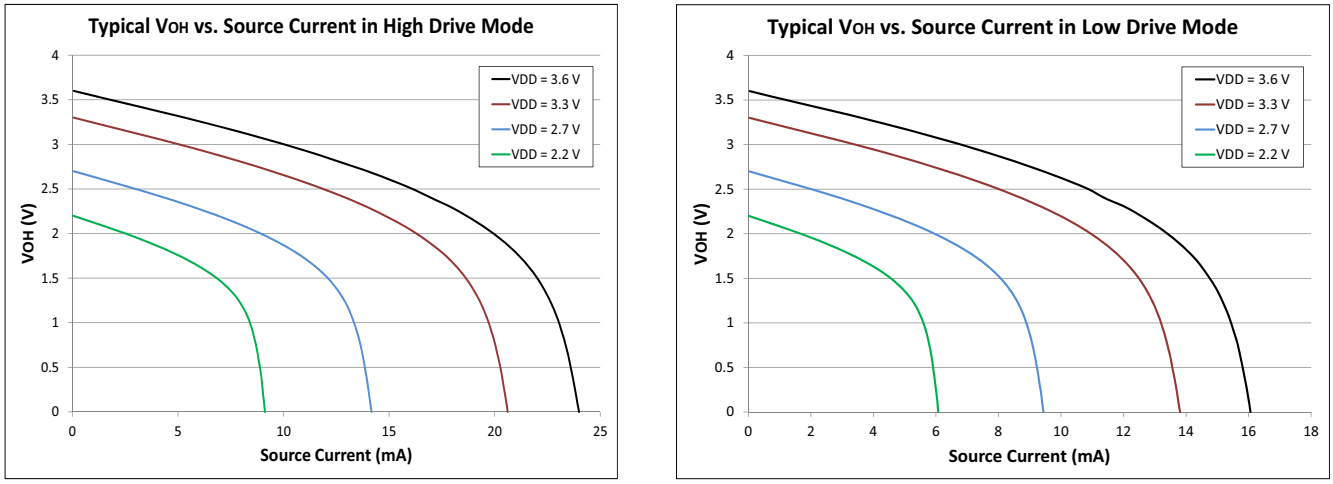

Figure 1.5. Typical V_{OH} vs. Source Current

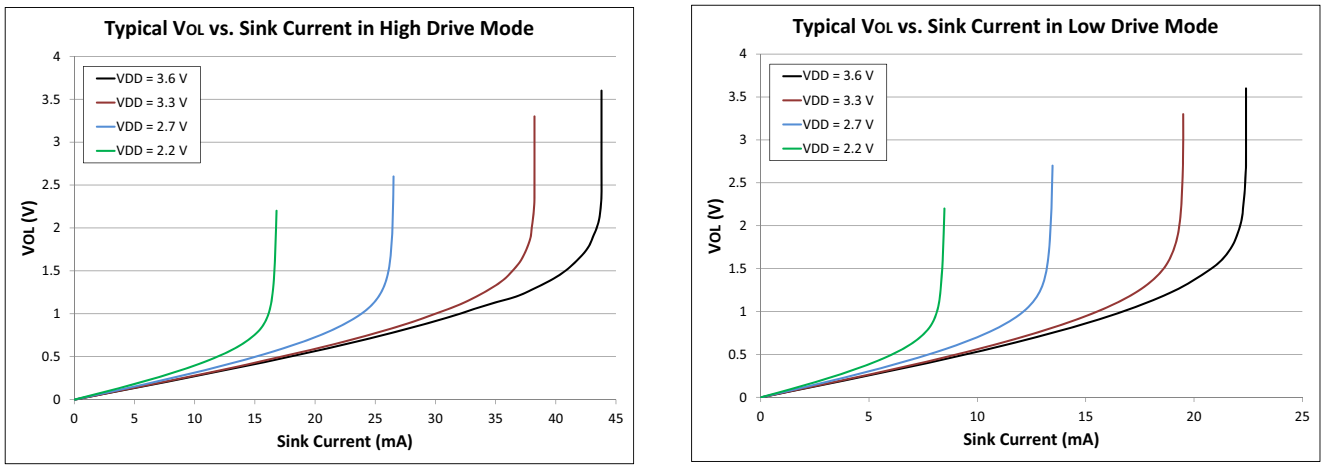

Figure 1.6. Typical V_{OL} vs. Sink Current

1.3. Thermal Conditions

Table 1.12. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	SOIC-16 Packages	—	70	—	°C/W
		QFN-20 Packages	—	60	—	°C/W
		QSOP-24 Packages	—	65	—	°C/W
***Note:** Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

1.4. Absolute Maximum Ratings

Stresses above those listed under Table 1.13 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 1.13. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		–55	125	°C
Storage Temperature	T_{STG}		–65	150	°C
Voltage on V_{DD}	V_{DD}		GND–0.3	4.2	V
Voltage on I/O pins or $\overline{RST}$	V_{IN}	$V_{DD} \geq 3.3$ V	GND–0.3	5.8	V
		$V_{DD} < 3.3$ V	GND–0.3	V_{DD}+2.5	V
Total Current Sunk into Supply Pin	I_{VDD}		—	400	mA
Total Current Sourced out of Ground Pin	I_{GND}		400	—	mA
Current Sourced or Sunk by Any I/O Pin or $\overline{RST}$	I_{PIO}		-100	100	mA
Operating Junction Temperature	T_J	Commercial Grade Devices (-GM, -GS, -GU)	–40	105	°C
		Industrial Grade Devices (-IM, -IS, -IU)	–40	125	°C
Note: Exposure to maximum rating conditions for extended periods may affect device reliability.					

2. System Overview

The C8051F85x/86x device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 4.1 for specific product feature selection and part ordering numbers.

- **Core:**
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 25 MHz maximum operating frequency
- **Memory:**
  - 2-8 kB flash; in-system programmable in 512-byte sectors
  - 512 bytes RAM (including 256 bytes standard 8051 RAM and 256 bytes on-chip XRAM)
- **Power:**
  - Internal low drop-out (LDO) regulator for CPU core voltage
  - Power-on reset circuit and brownout detectors
- **I/O: Up to 18 total multifunction I/O pins:**
  - All pins 5 V tolerant under bias
  - Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- **Clock Sources:**
  - Low-power internal oscillator: 24.5 MHz ±2%
  - Low-frequency internal oscillator: 80 kHz
  - External CMOS clock option
- **Timers/Counters and PWM:**
  - 3-channel Programmable Counter Array (PCA) supporting PWM, capture/compare and frequency output modes
  - 4x 16-bit general-purpose timers
  - Independent watchdog timer, clocked from low frequency oscillator
- **Communications and Other Digital Peripherals:**
  - UART
  - SPI™
  - I^2C / SMBus™
  - 16-bit CRC Unit, supporting automatic CRC of flash at 256-byte boundaries
- **Analog:**
  - 12-Bit Analog-to-Digital Converter (ADC)
  - 2 x Low-Current Comparators
- **On-Chip Debugging**

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the C8051F85x/86x devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware.

The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging.

Each device is specified for 2.2 to 3.6 V operation, and are available in 20-pin QFN, 16-pin SOIC or 24-pin QSOP packages. All package options are lead-free and RoHS compliant. The device is available in two temperature grades: -40 to +85 °C or –40 to +125 °C. See Table 4.1 for ordering information. A block diagram is included in Figure 2.1.

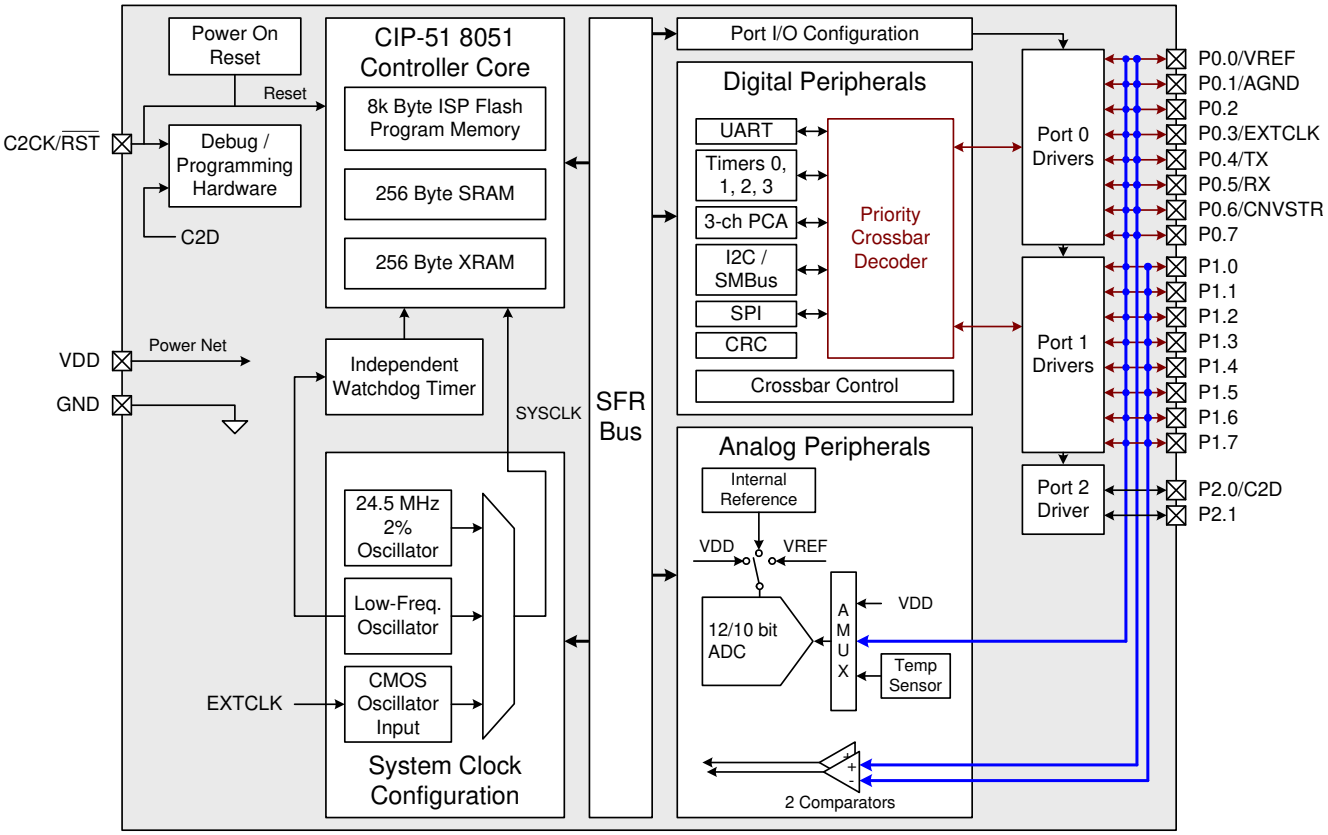

Figure 2.1. C8051F85x/86x Family Block Diagram (QSOP-24 Shown)

2.1. Power

2.1.1. LDO

The C8051F85x/86x devices include an internal regulator to regulate the supply voltage down the core operating voltage of 1.8 V. This LDO consumes little power, but can be shut down in the power-saving Stop mode.

2.1.2. Voltage Supply Monitor (VMON0)

The C8051F85x/86x devices include a voltage supply monitor which allows devices to function in known, safe operating condition without the need for external hardware.

The supply monitor module includes the following features:

- Holds the device in reset if the main VDD supply drops below the VDD Reset threshold.

2.1.3. Device Power Modes

The C8051F85x/86x devices feature three low power modes in addition to normal operating mode, allowing the designer to save power when the core is not in use. All power modes are detailed in Table 2.1.

Table 2.1. C8051F85x/86x Power Modes

Mode	Description	Mode Entrance	Mode Exit
Normal	Core and peripherals operating at full speed		
Idle	■ Core halted ■ Peripherals operate at full speed	Set IDLE bit in PCON	Any enabled interrupt or reset source
Stop	■ All clocks stopped ■ Core LDO and (optionally) comparators still running ■ Pins retain state	Clear STOPCF in REG0MD and Set STOP bit in PCON	Device reset
Shutdown	■ All clocks stopped ■ Core LDO and all analog circuits shut down ■ Pins retain state	Set STOPCF in REG0MD and Set STOP bit in PCON	Device reset

In addition, the user may choose to lower the clock speed in Normal and Idle modes to save power when the CPU requirements allow for lower speed.