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C8051F93x-C8051F92x

SILICON LABS Single/Dual Battery, 0.9–3.6 V, 64/32 kB, SmaRTClock, 10-Bit ADC MCU

Supply Voltage 0.9 to 3.6 V

- One-Cell Mode supports 0.9 to 1.8 V operation
- Two-Cell Mode supports 1.8 to 3.6 V operation
- Built-in dc-dc converter with 1.8 to 3.3 V output for use in one-cell mode
- Built-in LDO regulator allows a high analog supply voltage and low digital core voltage
- 2 built in supply monitors (brownout detectors)

10-Bit Analog to Digital Converter

- ± 1 LSB INL; no missing codes
- Programmable throughput up to 300 ksps
- Up to 23 external inputs
- On-Chip Voltage Reference
- On-Chip PGA allows measuring voltages up to twice the reference voltage
- 16-bit Auto-Averaging Accumulator with Burst Mode provides increased ADC resolution
- Data dependent windowed interrupt generator
- Built-in temperature sensor

Two Comparators

- Programmable hysteresis and response time
- Configurable as wake-up or reset source
- Up to 23 Capacitive Touch Sense Inputs

6-Bit Programmable Current Reference

- Up to ± 500 μ A. Can be used as a bias or for generating a custom reference voltage

On-Chip Debug

- On-chip debug circuitry facilitates full-speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Complete development kit

High-Speed 8051 μ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to **25 MIPS** throughput with 25 MHz clock
- Expanded interrupt handler

Memory

- 4352 bytes internal data RAM (256 + 4096)
- 64 kB (F93x) or 32 kB (F92x) Flash; In-system programmable in 1024-byte sectors—1024 bytes are reserved in the 64 kB devices

Digital Peripherals

- 24 or 16 port I/O; All 5 V tolerant with high sink current and programmable drive strength-Hardware SMBus™ (I²C™ Compatible), 2 x SPI™, and UART serial ports available concurrently
- Four general purpose 16-bit counter/timers
- Programmable 16-bit counter/timer array with six capture/compare modules and watchdog timer
- Hardware SmaRTClock operates down to 0.9 V and requires less than 0.5 μ A supply current

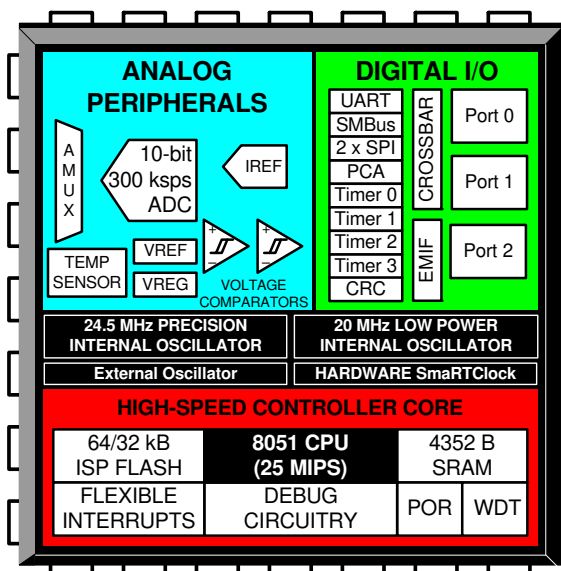
Clock Sources

- Internal oscillators: 24.5 MHz, 2% accuracy supports UART operation; 20 MHz low power oscillator requires very little bias current
- External oscillator: Crystal, RC, C, or CMOS Clock
- SmaRTClock oscillator: 32 kHz Crystal or internal self-oscillate mode
- Can switch between clock sources on-the-fly; useful in implementing various power saving modes

Packages

- 32-pin QFN (5 x 5 mm)
- 24-pin QFN (4 x 4 mm)
- 32-pin LQFP (7 x 7 mm, easy to hand-solder)

Temperature Range: -40 to $+85$ °C



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1. System Overview

C8051F93x-C8051F92x devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- Single/Dual Battery operation with on-chip dc-dc boost converter.
- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 10-bit 300 ksps 23-channel single-ended ADC with analog multiplexer
- 6-Bit Programmable Current Reference
- Precision programmable 24.5 MHz internal oscillator with spread spectrum technology.
- 64 kB or 32 kB of on-chip Flash memory
- 4352 bytes of on-chip RAM
- SMBus/I²C, Enhanced UART, and two Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with six capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, V_{DD} Monitor, and Temperature Sensor
- Two On-chip Voltage Comparators with 23 Touch Sense inputs.
- 24 or 16 Port I/O (5 V tolerant)

With on-chip Power-On Reset, V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051F93x-C8051F92x devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 0.9 to 1.8 V or 1.8 to 3.6 V operation over the industrial temperature range (–40 to +85 °C). The Port I/O and $\overline{\text{RST}}$ pins are tolerant of input signals up to 5 V. The C8051F930/20 are available in 32-pin QFN or LQFP packages and the C8051F931/21 are available in a 24-pin QFN package. Both package options are lead-free and RoHS compliant. See Table 2.1 for ordering information. Block diagrams are included in Figure 1.1 through Figure 1.4.

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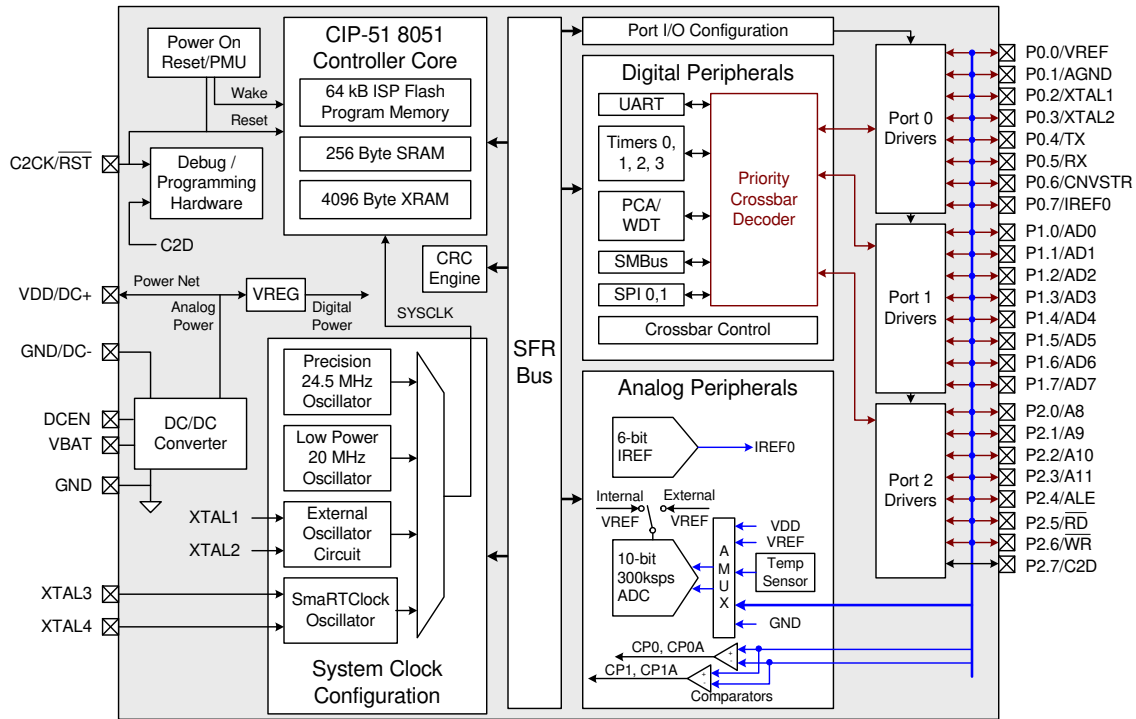


Figure 1.1. C8051F930 Block Diagram

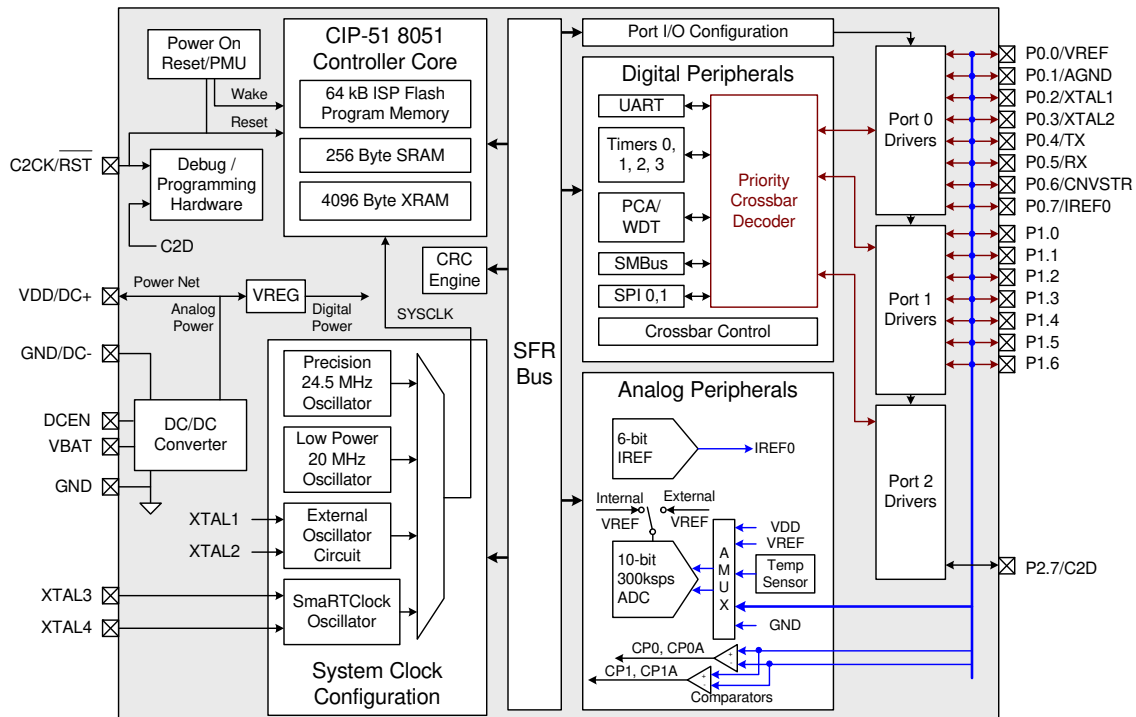


Figure 1.2. C8051F931 Block Diagram

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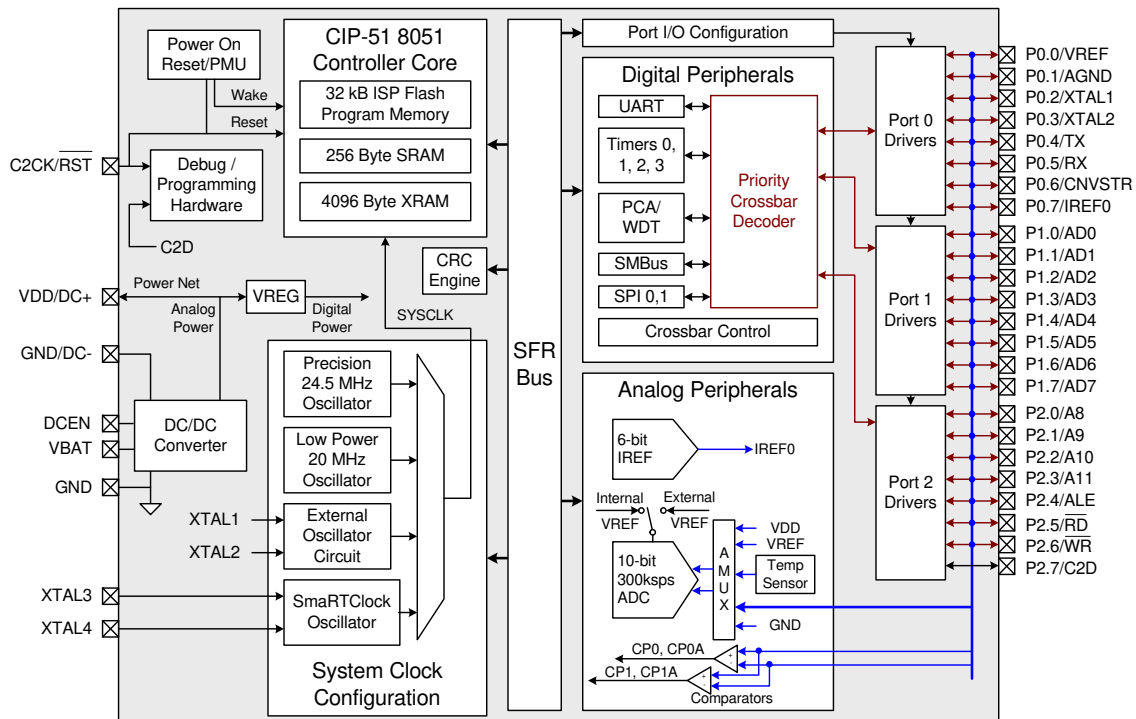


Figure 1.3. C8051F920 Block Diagram

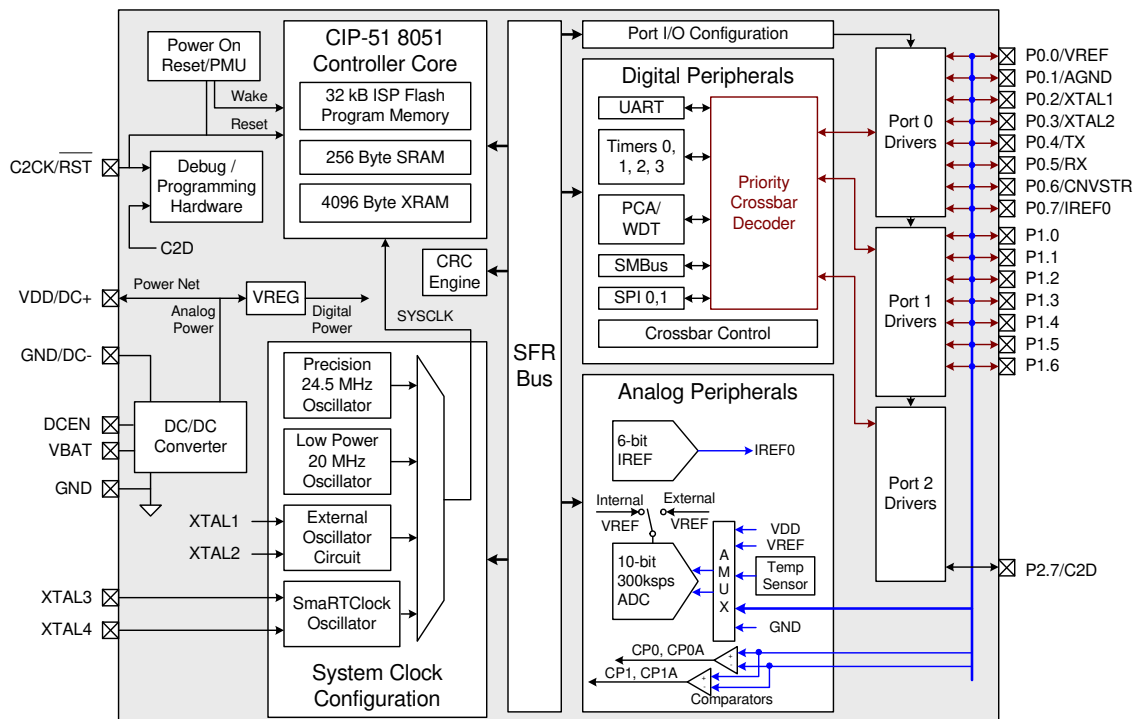


Figure 1.4. C8051F921 Block Diagram

1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F93x-C8051F92x family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS.

1.1.3. Additional Features

The C8051F93x-C8051F92x SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides multiple interrupt sources into the CIP-51 allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} monitor (forces reset when power supply voltage drops below safe levels), a Watchdog Timer, a Missing Clock Detector, SmaRTClock oscillator fail or alarm, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an illegal Flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently disabled in software after a power-on reset during MCU initialization.

The internal oscillator factory calibrated to 24.5 MHz and is accurate to $\pm 2\%$ over the full temperature and supply range. The internal oscillator period can also be adjusted by user firmware. An additional 20 MHz low power oscillator is also available which facilitates low-power operation. An external oscillator drive circuit is included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. If desired, the system clock source may be switched on-the-fly between both internal and external oscillator circuits. An external oscillator can also be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) source, while periodically switching to the fast (up to 25 MHz) internal oscillator as needed.

1.2. Port Input/Output

Digital and analog resources are available through 24 I/O pins (C8051F930/20) or 16 I/O pins (C8051F931/21). Port pins are organized as three byte-wide ports. Port pins P0.0–P2.6 can be defined as digital or analog I/O. Digital I/O pins can be assigned to one of the internal digital resources or used as general purpose I/O (GPIO). Analog I/O pins are used by the internal analog resources. P2.7 can be used

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as GPIO and is shared with the C2 Interface Data signal (C2D). See Section “27. C2 Interface” on page 319 for more details.

The designer has complete control over which digital and analog functions are assigned to individual Port pins, limited only by the number of physical I/O pins. This resource assignment flexibility is achieved through the use of a Priority Crossbar Decoder. See Section “21.3. Priority Crossbar Decoder” on page 216 for more information on the Crossbar.

All Port I/Os are 5 V tolerant when used as digital inputs or open-drain outputs. For Port I/Os configured as push-pull outputs, current is sourced from the VDD/DC+ supply. Port I/Os used for analog functions can operate up to the VDD/DC+ supply voltage. See Section “21.1. Port I/O Modes of Operation” on page 213 for more information on Port I/O operating modes and the electrical specifications chapter for detailed electrical specifications.

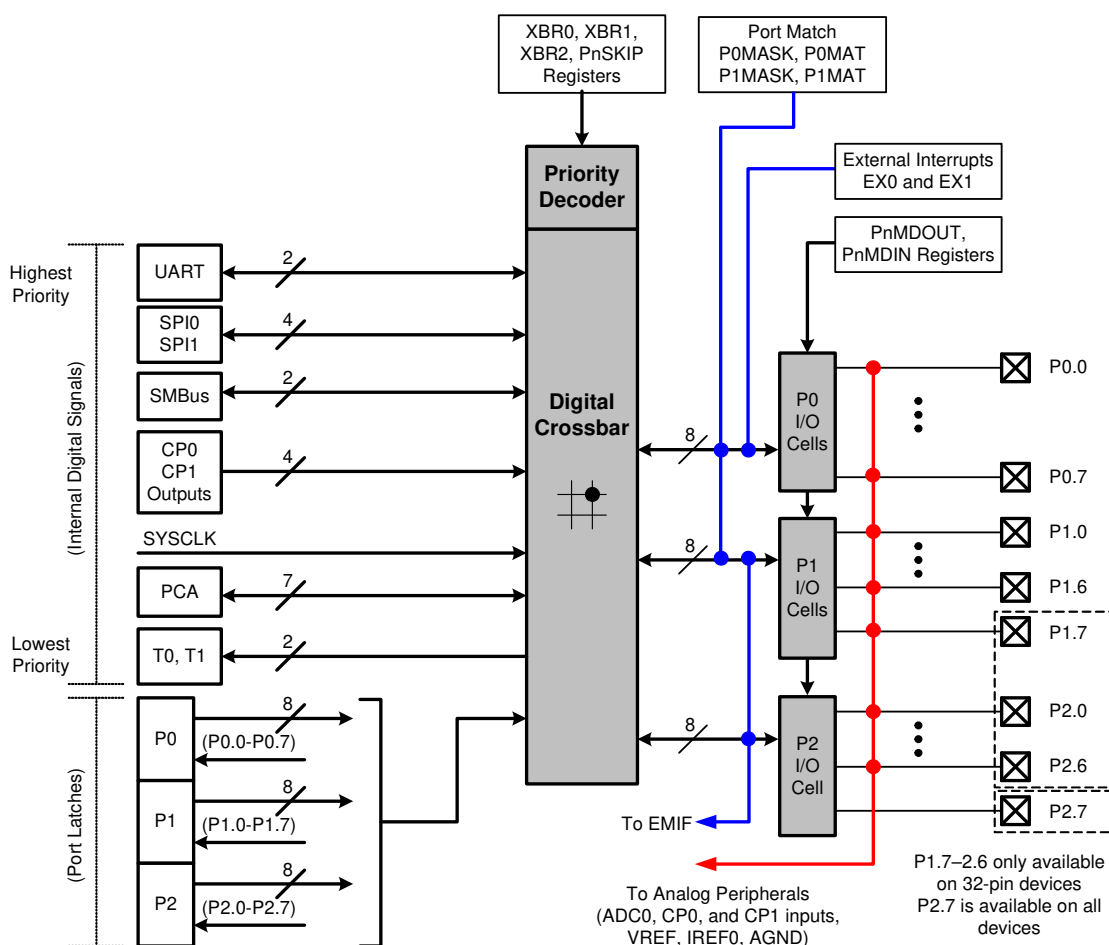


Figure 1.5. Port I/O Functional Block Diagram

1.3. Serial Ports

The C8051F93x-C8051F92x Family includes an SMBus/I²C interface, a full-duplex UART with enhanced baud rate configuration, and two Enhanced SPI interfaces. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.

1.4. Programmable Counter Array

An on-chip Programmable Counter/Timer Array (PCA) is included in addition to the four 16-bit general purpose counter/timers. The PCA consists of a dedicated 16-bit counter/timer time base with six programmable capture/compare modules. The PCA clock is derived from one of six sources: the system clock divided by 12, the system clock divided by 4, Timer 0 overflows, an External Clock Input (ECI), the system clock, or the external oscillator clock source divided by 8.

Each capture/compare module can be configured to operate in a variety of modes: edge-triggered capture, software timer, high-speed output, pulse width modulator (8, 9, 10, 11, or 16-bit), or frequency output. Additionally, Capture/Compare Module 5 offers watchdog timer (WDT) capabilities. Following a system reset, Module 5 is configured and enabled in WDT mode. The PCA Capture/Compare Module I/O and External Clock Input may be routed to Port I/O via the Digital Crossbar.

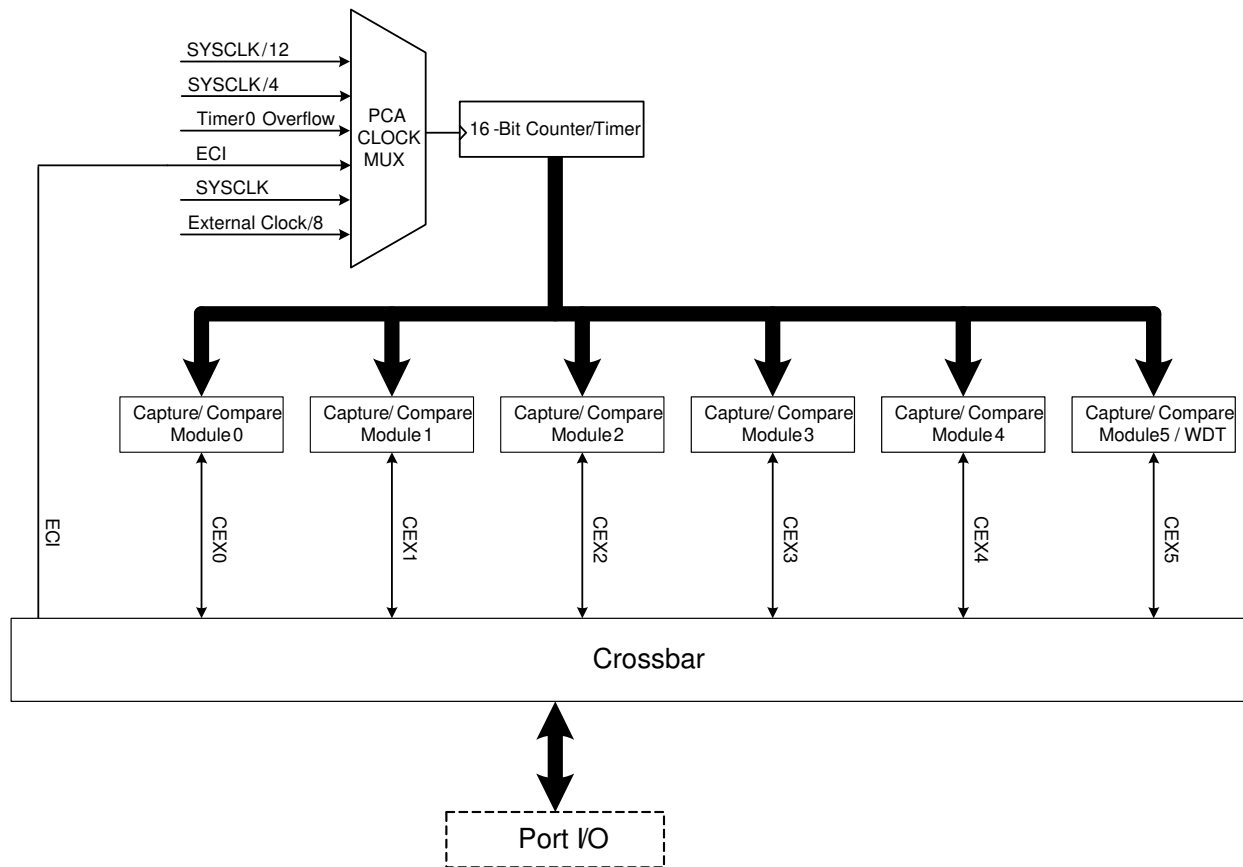


Figure 1.6. PCA Block Diagram

1.5. 10-Bit SAR ADC with 16-bit Auto-Averaging Accumulator and Autonomous Low Power Burst Mode

C8051F93x-C8051F92x devices have a 300 kpsps, 10-bit successive-approximation-register (SAR) ADC with integrated track-and-hold and programmable window detector. ADC0 also has an autonomous low power Burst Mode which can automatically enable ADC0, capture and accumulate samples, then place ADC0 in a low power shutdown mode without CPU intervention. It also has a 16-bit accumulator that can automatically average the ADC results, providing an effective 11, 12, or 13 bit ADC result without any additional CPU intervention.

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The ADC can sample the voltage at any of the GPIO pins (with the exception of P2.7) and has an on-chip attenuator that allows it to measure voltages up to twice the voltage reference. Additional ADC inputs include an on-chip temperature sensor, the VDD/DC+ supply voltage, the VBAT supply voltage, and the internal digital supply voltage.

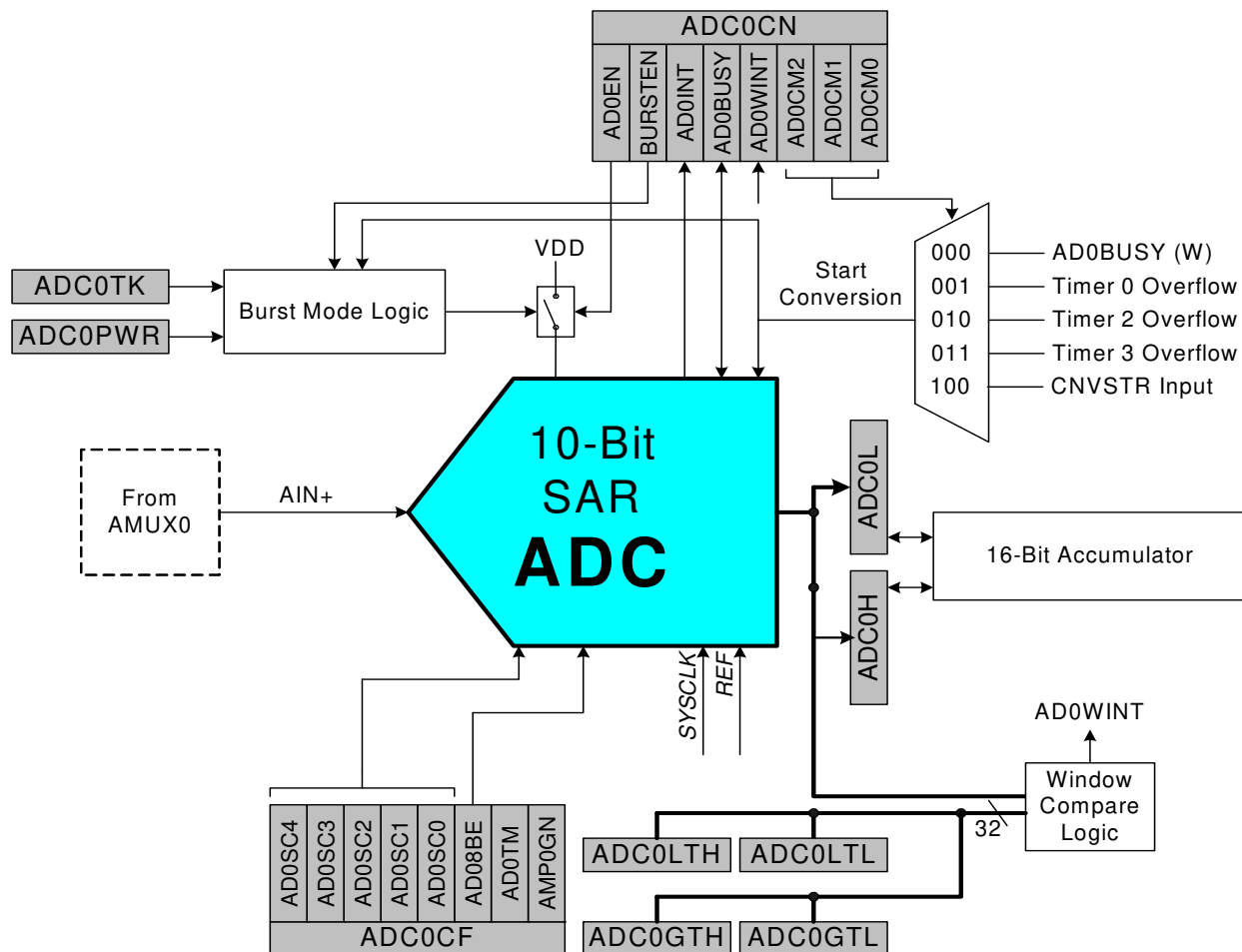


Figure 1.7. ADC0 Functional Block Diagram

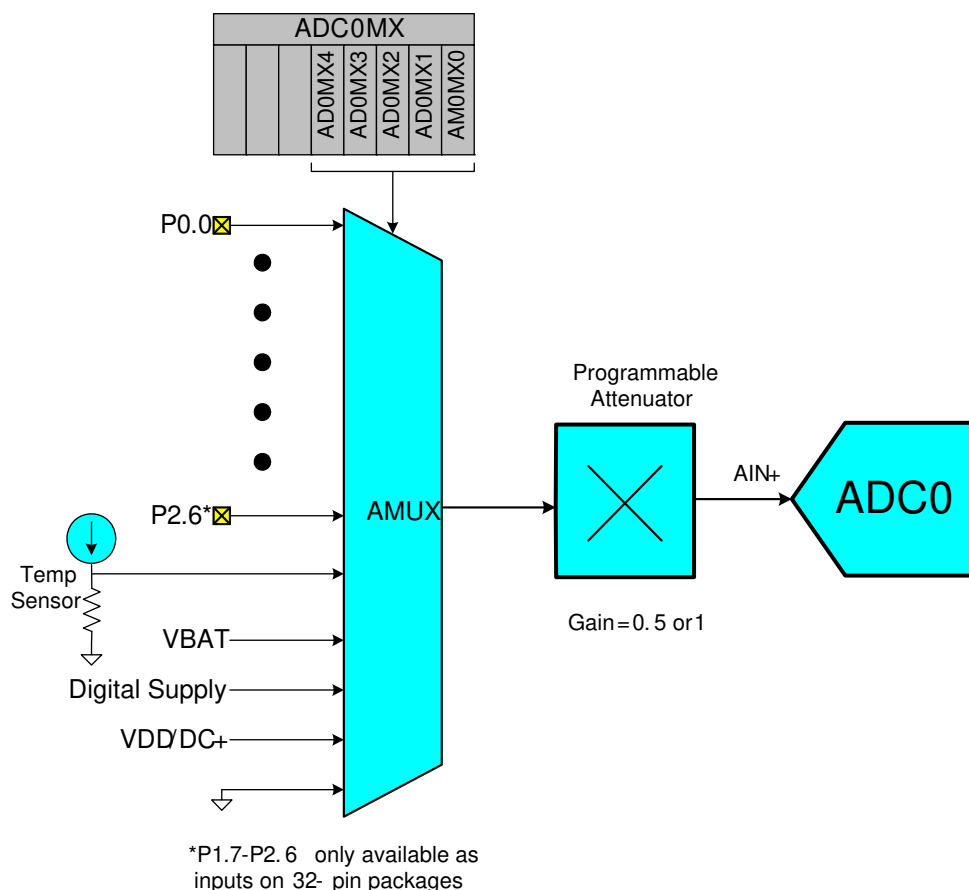


Figure 1.8. ADC0 Multiplexer Block Diagram

1.6. Programmable Current Reference (IREF0)

C8051F93x-C8051F92x devices include an on-chip programmable current reference (source or sink) with two output current settings: low power mode and high current mode. The maximum current output in low power mode is 63 μA (1 μA steps) and the maximum current output in high current mode is 504 μA (8 μA steps).

1.7. Comparators

C8051F93x-C8051F92x devices include two on-chip programmable voltage comparators: Comparator 0 (CPT0) which is shown in Figure 1.9; Comparator 1 (CPT1) which is shown in Figure 1.10. The two comparators operate identically but may differ in their ability to be used as reset or wake-up sources. See Section “18. Reset Sources” on page 180 and the Section “14. Power Management” on page 156 for details on reset sources and low power mode wake-up sources, respectively.

The Comparator offers programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the Port pins: a synchronous “latched” output (CP0, CP1), or an asynchronous “raw” output (CP0A, CP1A). The asynchronous CP0A signal is available even when the system clock is not active. This allows the Comparator to operate and generate an output when the device is in some low power modes.

The comparator inputs may be connected to Port I/O pins or to other internal signals. Port pins may also be used to directly sense capacitive touch switches.