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C8051F99x-C8051F98x

Ultra Low Power, 8-2 kB Flash, Capacitive Sensing MCU

Ultra Low Power Consumption
- 150 µA/MHz in active mode (24.5 MHz clock)
- 2 µs wakeup time
- 10 nA sleep mode with memory retention
- 50 nA sleep mode with brownout detector
- 300 nA sleep mode with LFO
- 600 nA sleep mode with external crystal

Supply Voltage 1.8 to 3.6 V
- Built-in LDO regulator allows a high analog supply voltage and low digital core voltage
- 2 built-in supply monitors (brownout detector) for sleep mode and active modes

12-Bit or 10-Bit Analog to Digital Converter
- ±1 LSB INL (10-bit mode); ±1.5 LSB INL (12-bit mode) no missing codes
- Programmable throughput up to 300 ksps (10-bit mode) or 75 ksps (12-bit mode)
- Up to 10 external inputs
- On-chip voltage reference; 0.5x gain allows measuring voltages up to twice the reference voltage
- 16-bit auto-averaging accumulator with burst mode provides increased ADC resolution
- Data dependent windowed interrupt generator
- Built-in temperature sensor

Capacitive Sense Interface (F99x)
- Supports buttons, sliders, wheels, and capacitive proximity sensing
- Fast 40 µs per channel conversion time
- 16-bit resolution, up to 14 input channels
- Auto scan and wake-on-touch
- Auto-accumulate up to 64x samples

Analog Comparator
- Programmable hysteresis and response time
- Configurable as wake-up or reset source

6-Bit Programmable Current Reference
- Up to ±500 µA, can be used as a bias or for generating a custom reference voltage
- PWM enhanced resolution mode

High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to **25 MIPS** throughput with 25 MHz clock
- Expanded interrupt handler

Memory
- 512 bytes RAM
- 8 kB (F990/1/6/7, F980/1/6/7), 4 kB (F982/3/8/9), or 2 kB (F985) Flash; in-system programmable

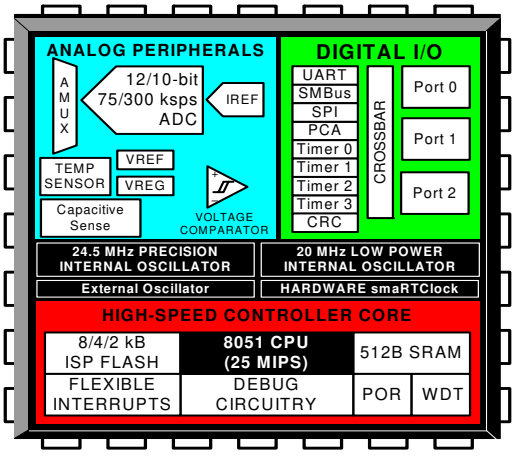
Digital Peripherals
- Up to 17 port I/O; high sink current and programmable drive strength
  Hardware SMBus™/I²C™, SPI™, and UART serial ports available concurrently
- Four general purpose 16-bit counter/timers
- Programmable 16-bit counter/timer array with three capture/compare modules and watchdog timer

Clock Sources
- Internal oscillators: 24.5 MHz, 2% accuracy supports UART operation; 20 MHz low power oscillator requires very little bias current.
- External oscillator: Crystal, RC, C, or CMOS Clock
- SmaRTClock oscillator: 32 kHz Crystal or internal
- Can switch between clock sources on-the-fly; useful in implementing various power saving modes

On-Chip Debug
- On-chip debug circuitry facilitates full-speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Complete development kit

Packages
- 20-pin QFN (3 x 3 mm)
- 24-pin QFN (4 x 4 mm)
- 24-pin QSOP (easy to hand-solder)

Temperature Range: –40 to +85 °C



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1. System Overview

C8051F99x-C8051F98x devices are fully integrated mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- Ultra low power consumption in active and sleep modes.
- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- 10-bit 300 ksps or 12-bit 75 ksps single-ended ADC with analog multiplexer
- 6-bit programmable current reference (resolution can be increased with PWM)
- Precision programmable 24.5 MHz internal oscillator with spread spectrum technology.
- 8 kB, 4 kB, or 2 kB of on-chip Flash memory
- 512 bytes of on-chip RAM
- SMBus/I^2C, Enhanced UART, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable counter/timer array (PCA) with three capture/compare modules and watchdog timer function
- On-chip power-on reset, V_{DD} monitor, and temperature sensor
- One on-chip voltage comparator
- Up to 14 Capacitive Touch Inputs
- Up to 17 Port I/O

With on-chip power-on reset, V_{DD} monitor, watchdog timer, and clock oscillator, the C8051F99x-C8051F98x devices are truly stand-alone system-on-a-chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 1.8 to 3.6 V operation over the industrial temperature range (–40 to +85 °C). The Port I/O and $\overline{RST}$ pins are powered from the supply voltage. The C8051F99x-C8051F98x devices are available in 20-pin or 24-pin QFN or 24-pin QSOP packages. All package options are lead-free and RoHS compliant. See Table 2.1 for ordering information. Block diagrams are included in Figure 1.1 through Figure 1.9.

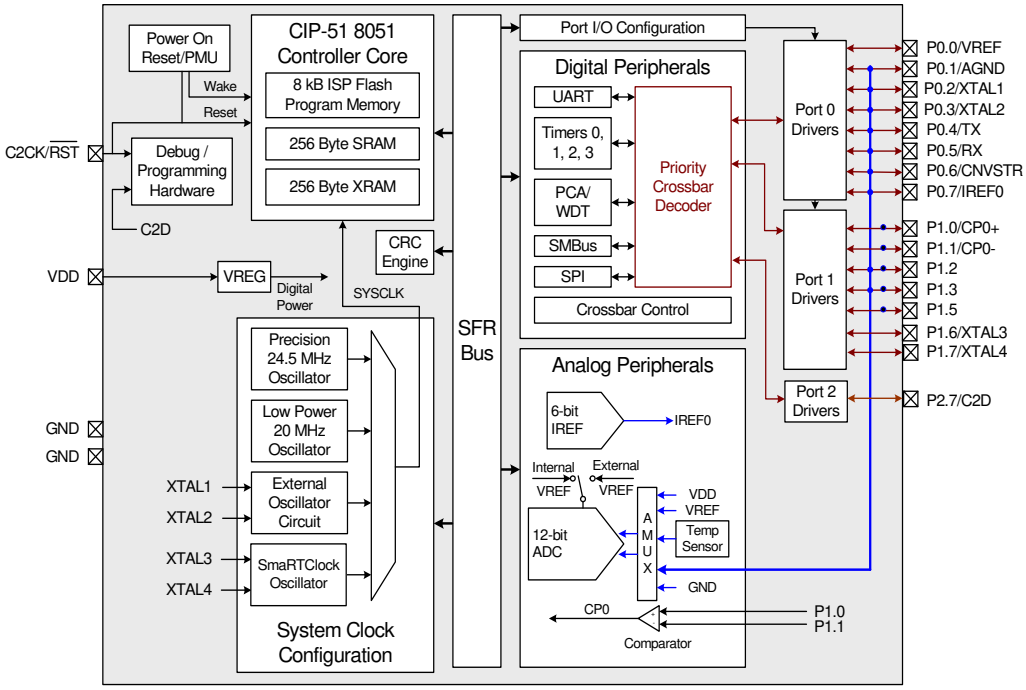

Figure 1.1. C8051F980 Block Diagram

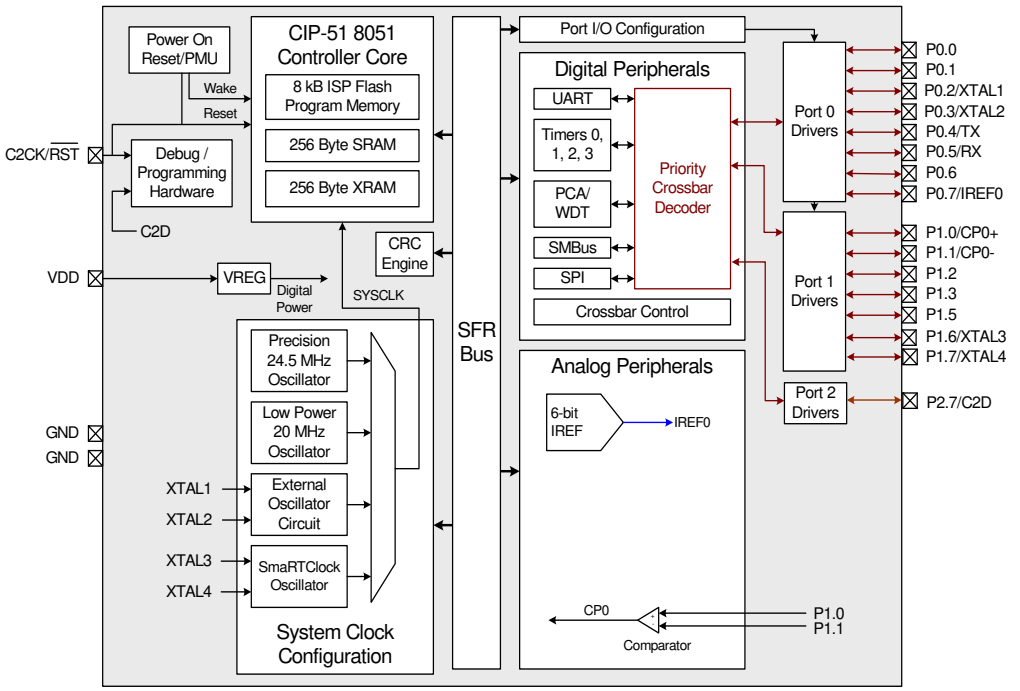

Figure 1.2. C8051F981 Block Diagram

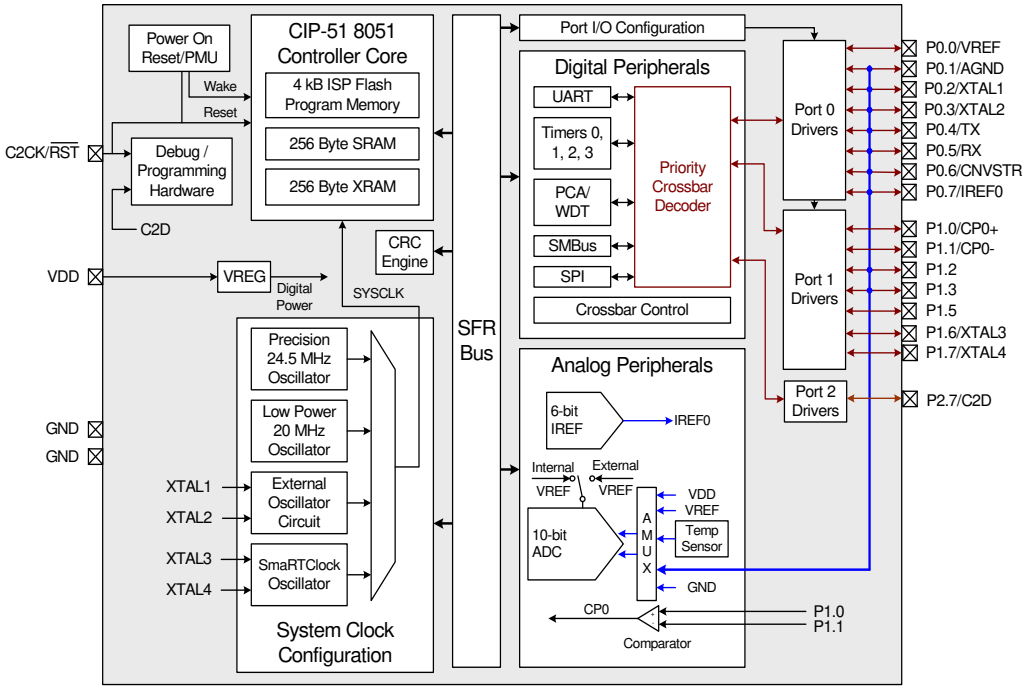

Figure 1.3. C8051F982 Block Diagram

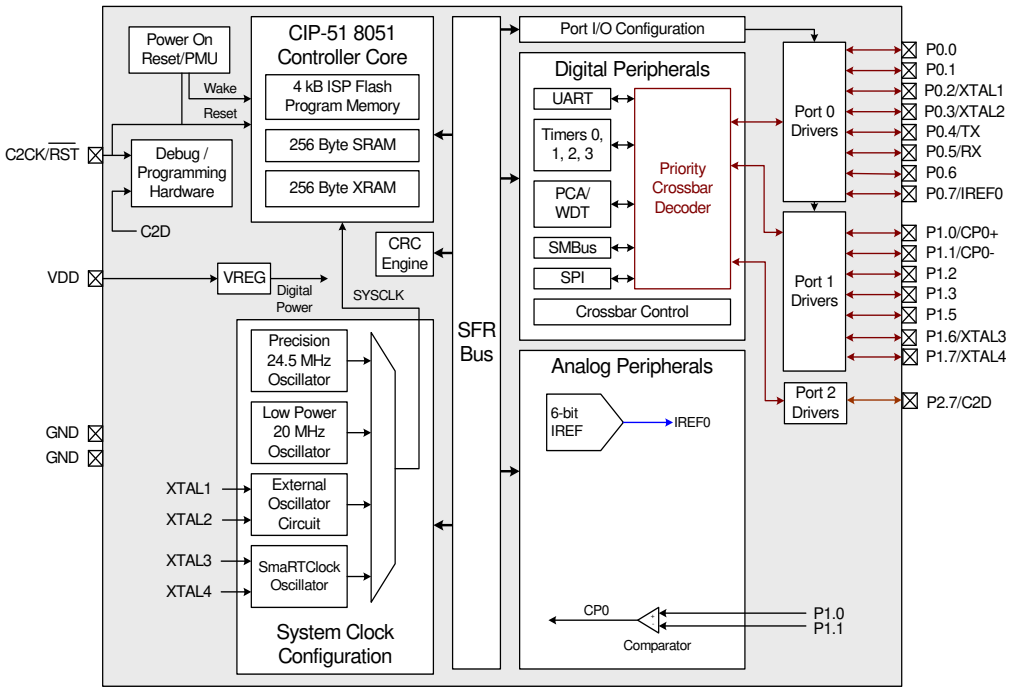

Figure 1.4. C8051F983 Block Diagram

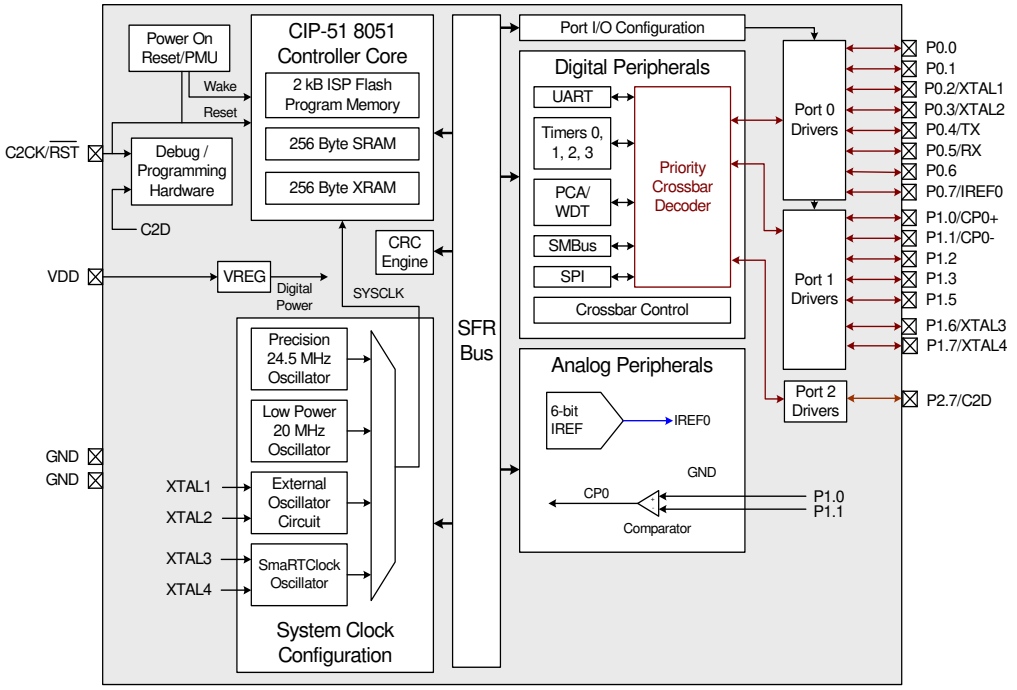

Figure 1.5. C8051F985 Block Diagram

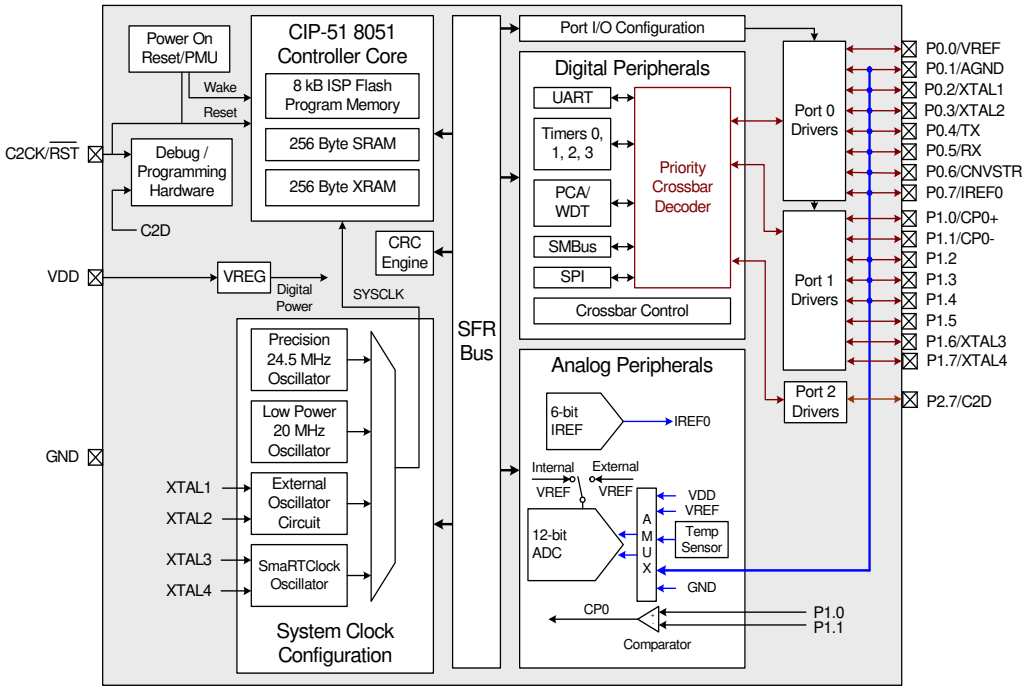

Figure 1.6. C8051F986 Block Diagram

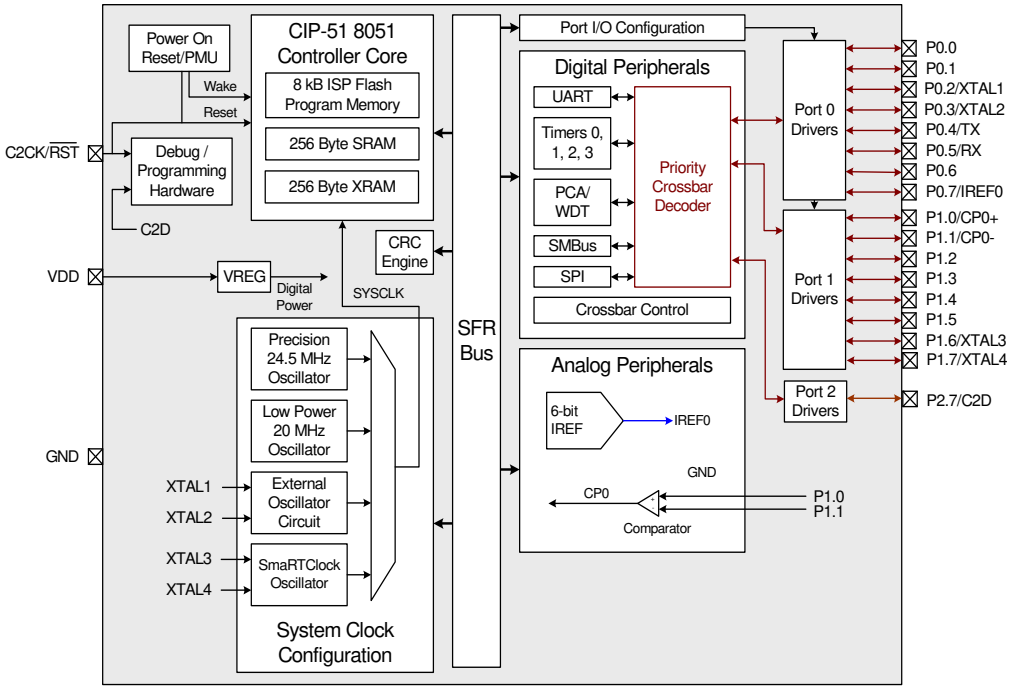

Figure 1.7. C8051F987 Block Diagram

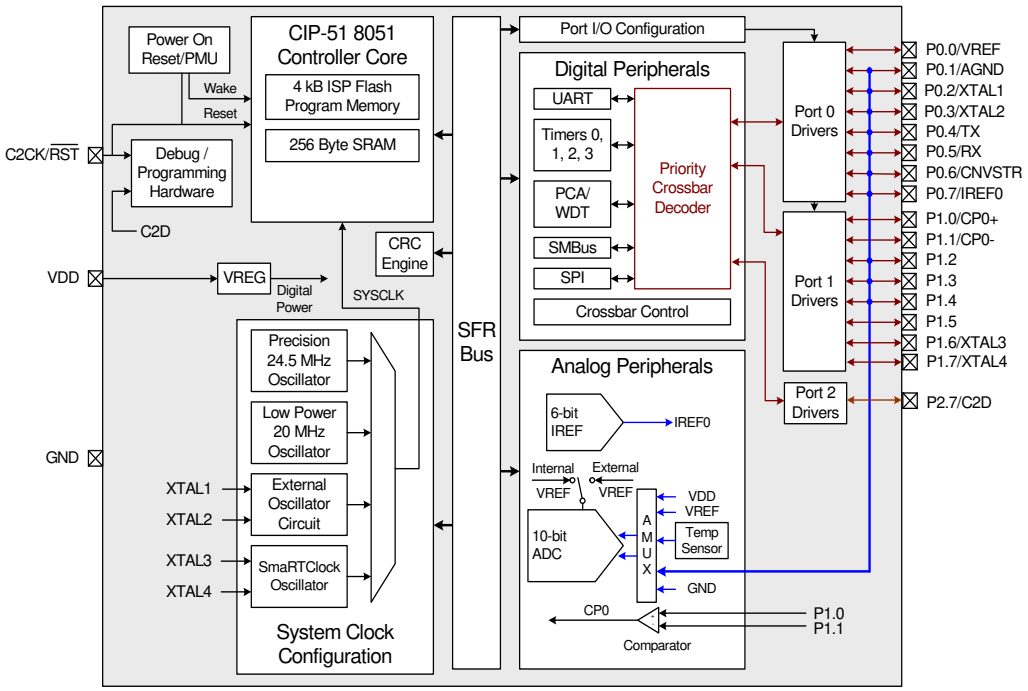

Figure 1.8. C8051F988 Block Diagram

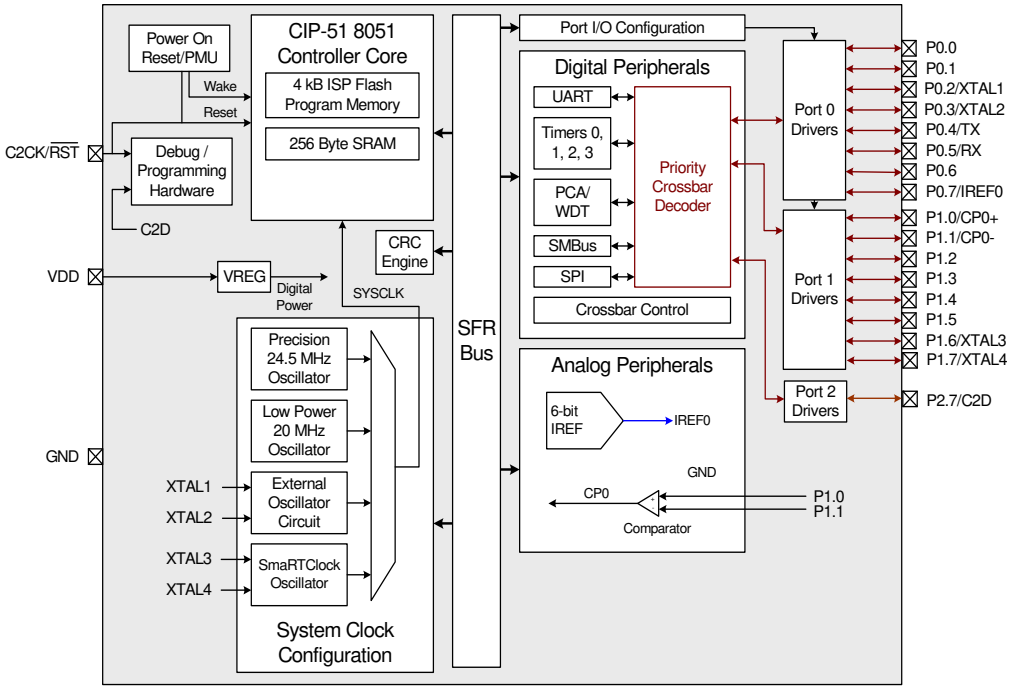

Figure 1.9. C8051F989 Block Diagram

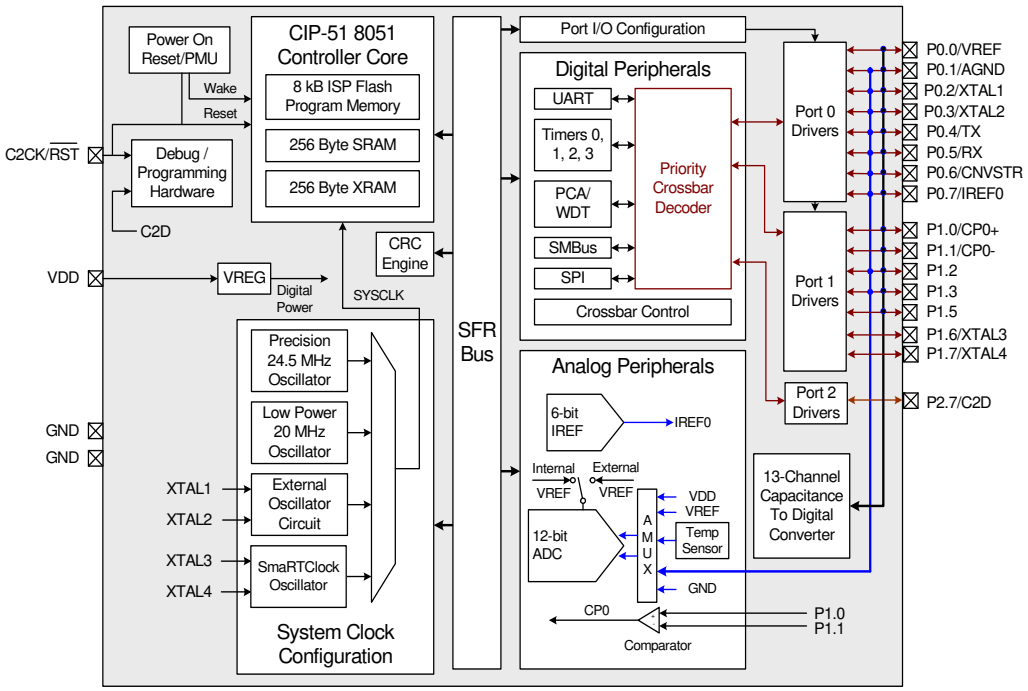

Figure 1.10. C8051F990 Block Diagram

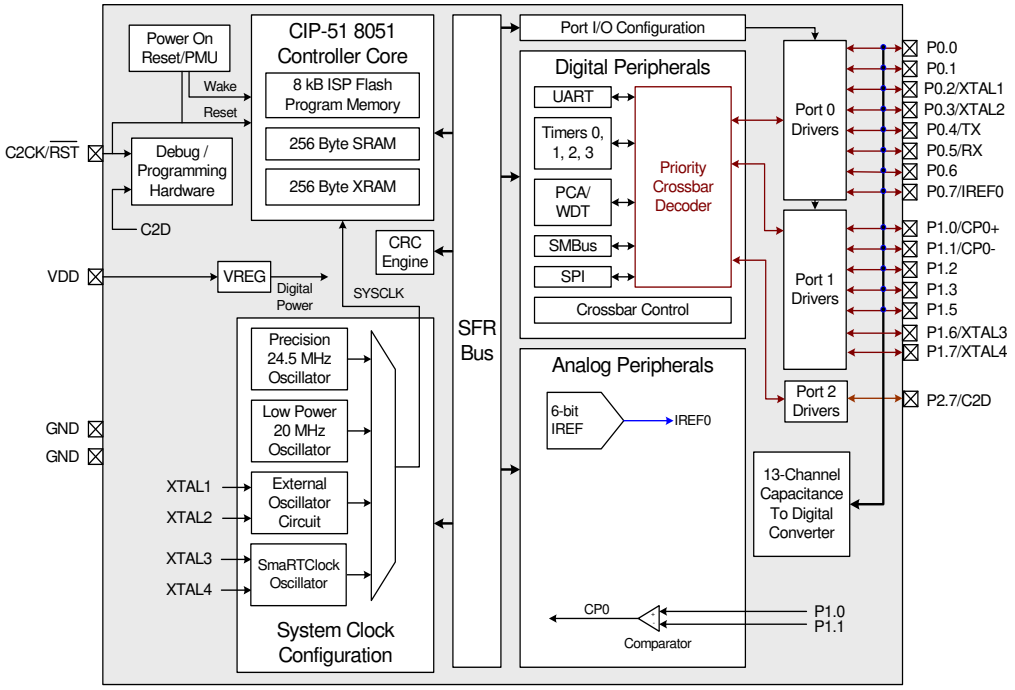

Figure 1.11. C8051F991 Block Diagram

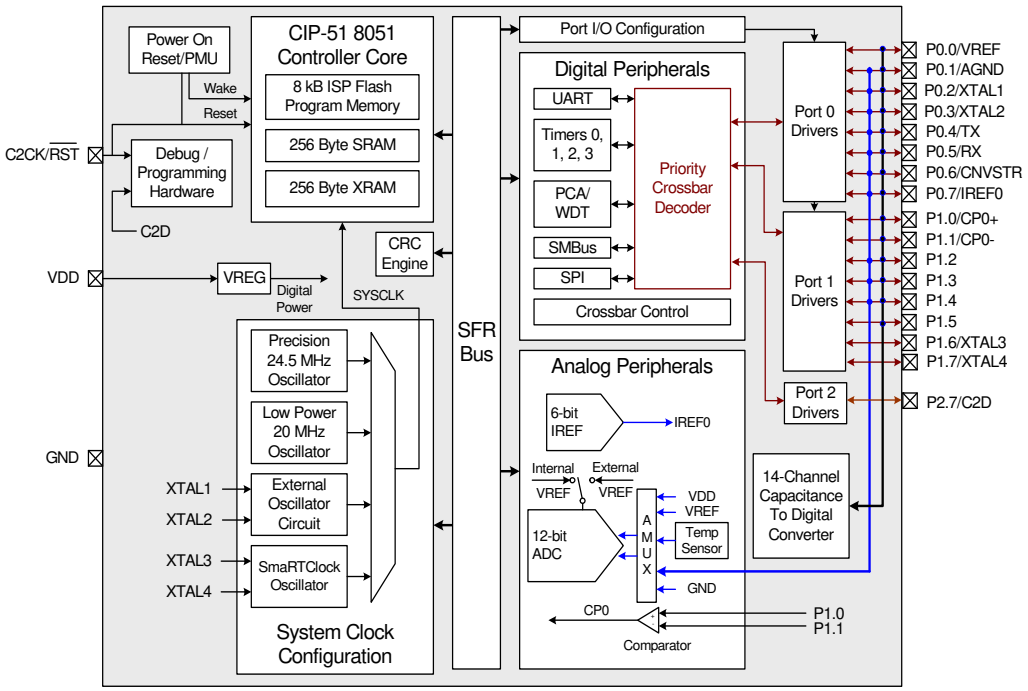

Figure 1.12. C8051F996 Block Diagram

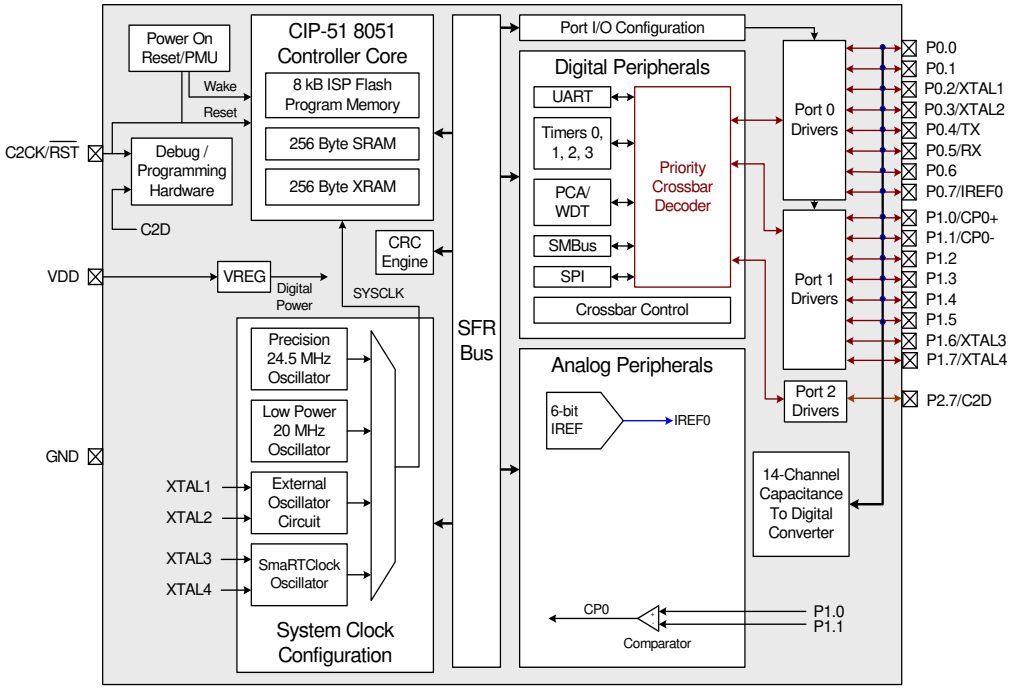

Figure 1.13. C8051F997 Block Diagram

1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F99x-C8051F98x family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS.

1.1.3. Additional Features

The C8051F99x-C8051F98x SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides multiple interrupt sources into the CIP-51 allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} monitor (forces reset when power supply voltage drops below safe levels), a Watchdog Timer, a Missing Clock Detector, SmaRTClock oscillator fail or alarm, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an illegal Flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently disabled in software after a power-on reset during MCU initialization.

The internal oscillator is factory calibrated to 24.5 MHz and is accurate to ±2% over the full temperature and supply range. The internal oscillator period can also be adjusted by user firmware. An additional 20 MHz low power oscillator is also available which facilitates low-power operation. An external oscillator drive circuit is included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. If desired, the system clock source may be switched on-the-fly between both internal and external oscillator circuits. An external oscillator can also be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) source, while periodically switching to the fast (up to 25 MHz) internal oscillator as needed.