Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

C8051T600/1/2/3/4/5/6

Mixed-Signal Byte-Programmable EPROM MCU

Analog Peripherals
- **10-Bit ADC ('T600/602/604 only)**
  - Up to 500 ksps
  - Up to 8 external inputs
  - V_{REF} external pin, Internal Regulator or V_{DD}
  - Internal or external start of conversion source
  - Built-in temperature sensor
- **Comparator**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source
  - Low current

On-Chip Debug
- C8051F300 can be used as code development platform; complete development kit available
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug
- Provides breakpoints, single stepping, inspect/modify memory and registers

Supply Voltage 1.8 to 3.6 V
- On-chip LDO for internal core supply
- Built-in voltage supply monitor

Temperature Range: –40 to +85 °C

Package Options:
- 3 x 3 mm QFN11
- 2 x 2 mm QFN10 (C8051T606 Only)
- MSOP10 (C8051T606 Only)
- SOIC14 (C8051T600/1/2/3/4/5 Only)

High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

Memory
- 256 or 128 Bytes internal data RAM
- 8, 4, 2, or 1.5 kB byte-programmable EPROM code memory

Digital Peripherals
- Up to 8 Port I/O with high sink current capability
- Hardware enhanced UART and SMBus™ serial ports
- Three general purpose 16-bit counter/timers
- 16-bit programmable counter array (PCA) with three capture/compare modules
  - 8 or 16-bit PWM
  - Rising / falling edge capture
  - Frequency output
  - Software timer

Clock Sources
- Internal oscillator: 24.5 MHz with ±2% accuracy supports crystal-less UART operation
- External oscillator: RC, C, or CMOS Clock
- Can switch between clock sources on-the-fly; useful in power saving modes

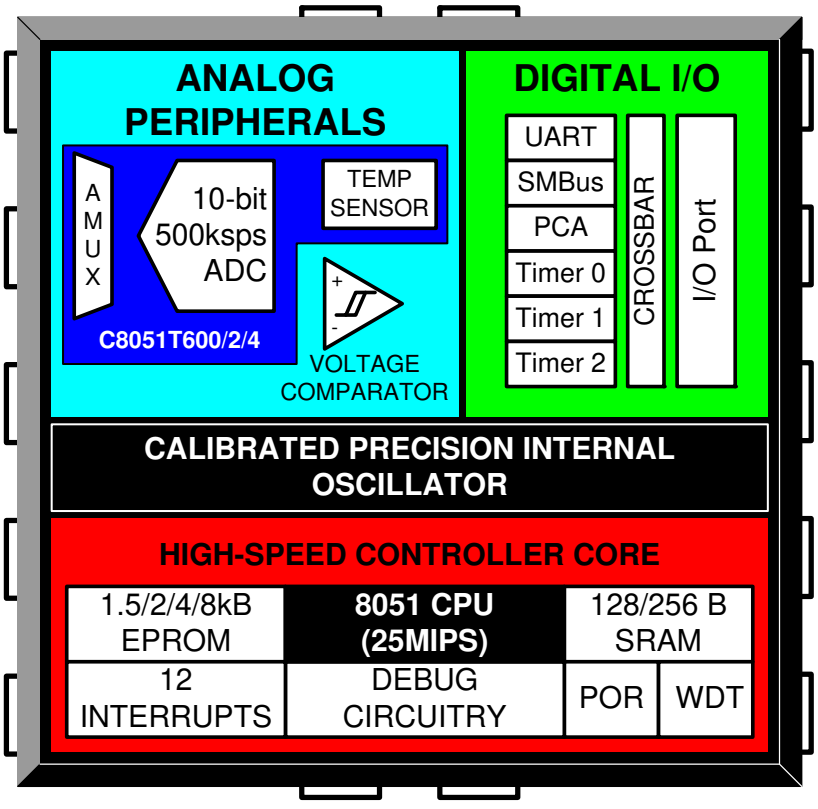

Table of Contents

List of Figures

List of Tables

List of Registers

1. System Overview

C8051T600/1/2/3/4/5/6 devices are fully integrated, mixed-signal, system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- C8051F300 ISP Flash device is available for quick in-system code development
- 10-bit 500 ksps Single-ended ADC with analog multiplexer and integrated temperature sensor
- Precision calibrated 24.5 MHz internal oscillator
- 8 k, 4 k, 2 k or 1.5 kB of on-chip Byte-Programmable EPROM—(512 bytes are reserved on 8k version)
- 256 or 128 bytes of on-chip RAM
- SMBus/I^2C, and ART serial interfaces implemented in hardware
- Three general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with three capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset and Supply Monitor
- On-chip Voltage Comparator
- 8 or 6 Port I/O

With on-chip power-on reset, V_{DD} monitor, watchdog timer, and clock oscillator, the C8051T600/1/2/3/4/5/6 devices are truly stand-alone, system-on-a-chip solutions. User software has complete control of all peripherals and may individually shut down any or all peripherals for power savings.

Code written for the C8051T600/1/2/3/4/5/6 family of processors will run on the C8051F300 Mixed-Signal ISP Flash microcontroller, providing a quick, cost-effective way to develop code without requiring special emulator circuitry. The C8051T600/1/2/3/4/5/6 processors include Silicon Laboratories' 2-Wire C2 Debug and Programming interface, which allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection of memory, viewing and modification of special function registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 1.8–3.6 V operation over the industrial temperature range (–45 to +85 °C). An internal LDO is used to supply the processor core voltage at 1.8 V. The Port I/O and $\overline{RST}$ pins are tolerant of input signals up to 5 V. See Table 2.1 for ordering information. Block diagrams of the devices in the C8051T600/1/2/3/4/5/6 family are shown in Figure 1.1, Figure 1.2, and Figure 1.3.

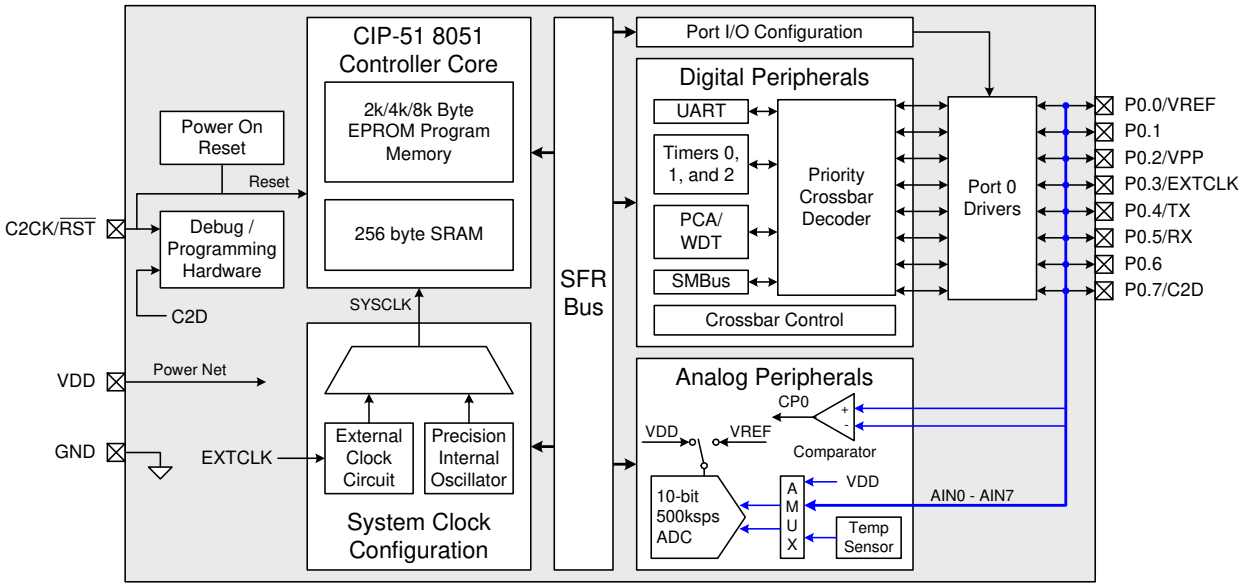

Figure 1.1. C8051T600/2/4 Block Diagram

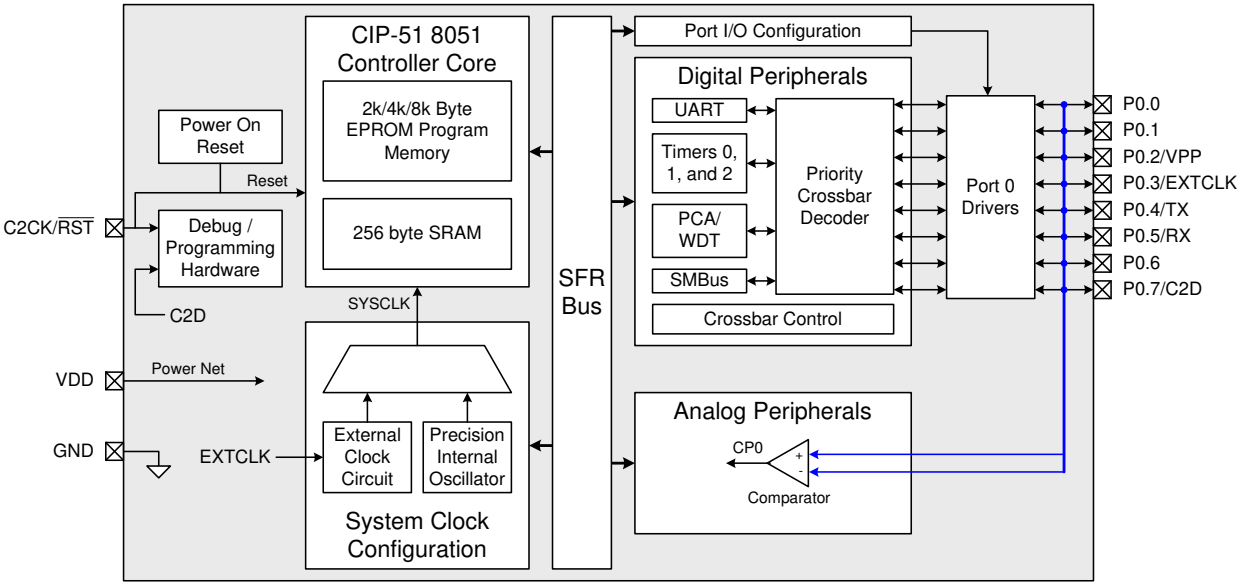

Figure 1.2. C8051T601/3/5 Block Diagram

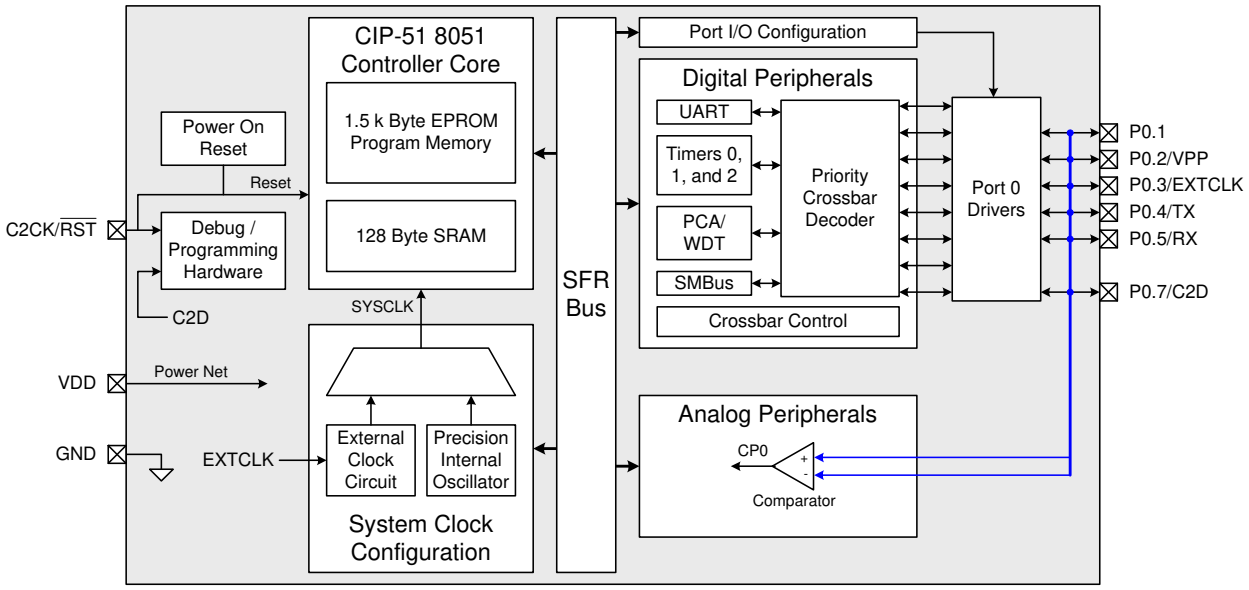

Figure 1.3. C8051T606 Block Diagram

2. Ordering Information

Table 2.1. Product Selection Guide

Part Number	MIPS (Peak)	OTP EPROM (Bytes)	RAM (Bytes)	Calibrated Internal Oscillator	SMBus/I²C	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 500ksps ADC	Temperature Sensor	Analog Comparators	Lead-Free (ROHS Compliant)[2]	Package
C8051T600-GM	25	8k[1]	256	Y	Y	Y	3	Y	8	Y	Y	1	Y	QFN-11
C8051T600-GS	25	8k[1]	256	Y	Y	Y	3	Y	8	Y	Y	1	Y	SOIC-14
C8051T601-GM	25	8k[1]	256	Y	Y	Y	3	Y	8	—	—	1	Y	QFN-11
C8051T601-GS	25	8k[1]	256	Y	Y	Y	3	Y	8	—	—	1	Y	SOIC-14
C8051T602-GM	25	4k	256	Y	Y	Y	3	Y	8	Y	Y	1	Y	QFN-11
C8051T602-GS	25	4k	256	Y	Y	Y	3	Y	8	Y	Y	1	Y	SOIC-14
C8051T603-GM	25	4k	256	Y	Y	Y	3	Y	8	—	—	1	Y	QFN-11
C8051T603-GS	25	4k	256	Y	Y	Y	3	Y	8	—	—	1	Y	SOIC-14
C8051T604-GM	25	2k	256	Y	Y	Y	3	Y	8	Y	Y	1	Y	QFN-11
C8051T604-GS	25	2k	256	Y	Y	Y	3	Y	8	Y	Y	1	Y	SOIC-14
C8051T605-GM	25	2k	256	Y	Y	Y	3	Y	8	—	—	1	Y	QFN-11
C8051T605-GS	25	2k	256	Y	Y	Y	3	Y	8	—	—	1	Y	SOIC-14
C8051T606-GM	25	1.5k	128	Y	Y	Y	3	Y	6	—	—	1	Y	QFN-11
C8051T606-GT	25	1.5k	128	Y	Y	Y	3	Y	6	—	—	1	Y	MSOP-10
C8051T606-ZM	25	1.5k	128	Y	Y	Y	3	Y	6	—	—	1	Y	QFN-10

Notes:
1. 512 Bytes Reserved
2. Lead Finish is 100% Matte Tin (Sn)

3. Pin Definitions

Table 3.1. Pin Definitions for the C8051T600/1/2/3/4/5

Name	QFN11 Pin	SOIC14 Pin	Type	Description
V_{DD}	3	7		Power Supply Voltage.
GND	11	3		Ground.
$\overline{RST}$ /	8	14	D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor.
C2CK			D I/O	Clock signal for the C2 Debug Interface.
P0.7 /	10	2	D I/O or A In	Port 0.7.
C2D			D I/O	Bi-directional data signal for the C2 Debug Interface.
P0.0 /	1	5	D I/O or A In	Port 0.0.
VREF			A In	External VREF input.
P0.1	2	6	D I/O or A In	Port 0.1.
P0.2 /	4	8	D I/O or A In	Port 0.2.
V_{PP}			A In	V_{PP} Programming Supply Voltage.
P0.3 /	5	10	D I/O or A In	Port 0.3.
EXTCLK			A I/O or D In	External Clock Pin. This pin can be used as the external clock input for CMOS, capacitor, or RC oscillator configurations.
P0.4	6	12	D I/O or A In	Port 0.4.
P0.5	7	13	D I/O or A In	Port 0.5.
P0.6 /	9	1	D I/O or A In	Port 0.6.
CNVSTR			D In	ADC0 External Convert Start Input.
NC	—	4,9,11		No Connection.

Table 3.2. Pin Definitions for the C8051T606

Name	QFN11 Pin	MSOP10 Pin	QFN10 Pin	Type	Description
V_{DD}	3	3	2		Power Supply Voltage.
GND	9	9	8		Ground (Required).
GND*	11	—	—		Ground (Optional).
$\overline{RST}$ /	8	8	7	D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor.
C2CK				D I/O	Clock signal for the C2 Debug Interface.
P0.7 /	10	10	9	D I/O or A In	Port 0.7.
C2D				D I/O	Bi-directional data signal for the C2 Debug Interface.
P0.1	2	2	1	D I/O or A In	Port 0.1.
P0.2 /	4	4	3	D I/O or A In	Port 0.2.
V_{PP}				A In	V_{PP} Programming Supply Voltage.
P0.3 /	5	5	4	D I/O or A In	Port 0.3.
EXTCLK				A I/O or D In	External Clock Pin. This pin can be used as the external clock input for CMOS, capacitor, or RC oscillator configurations.
P0.4	6	6	5	D I/O or A In	Port 0.4.
P0.5	7	7	6	D I/O or A In	Port 0.5.
NC	1	1	10		No Connection.

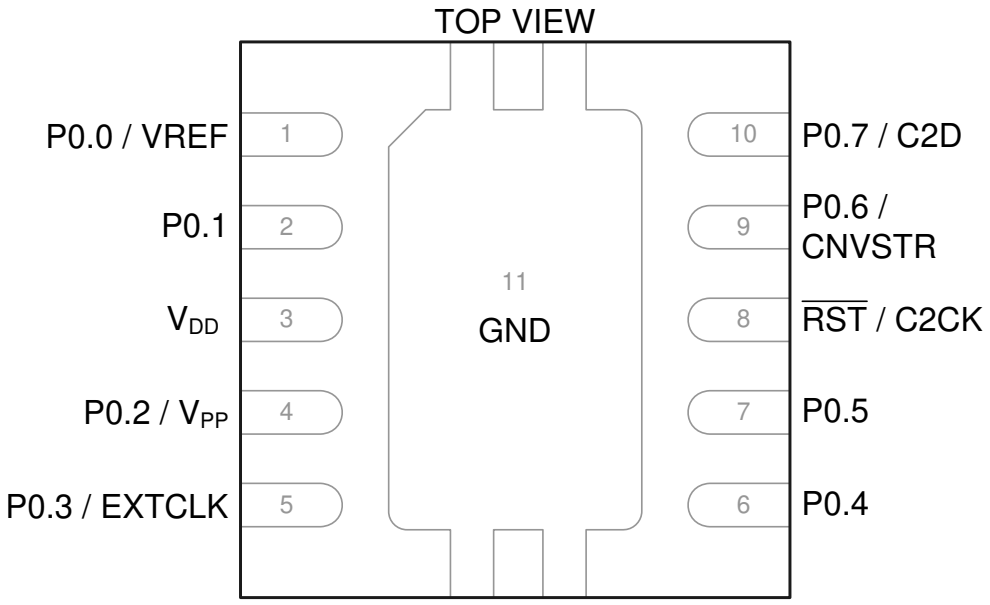

Figure 3.1. C8051T600/1/2/3/4/5-GM QFN11 Pinout Diagram (Top View)

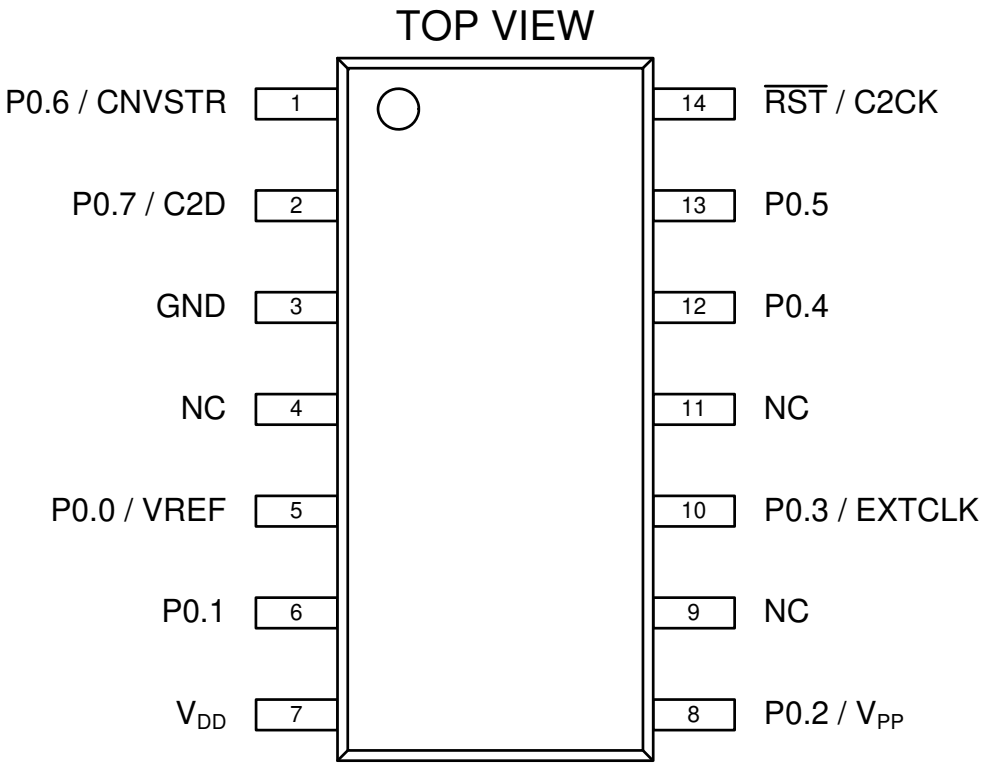

Figure 3.2. C8051T600/1/2/3/4/5-GS SOIC14 Pinout Diagram (Top View)

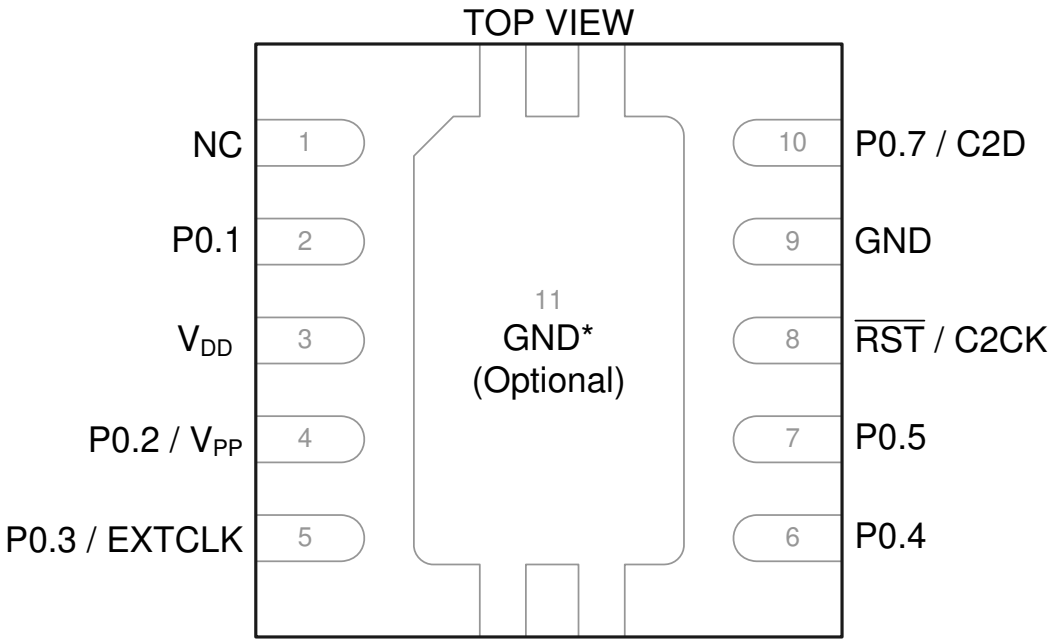

Figure 3.3. C8051T606-GM QFN11 Pinout Diagram (Top View)

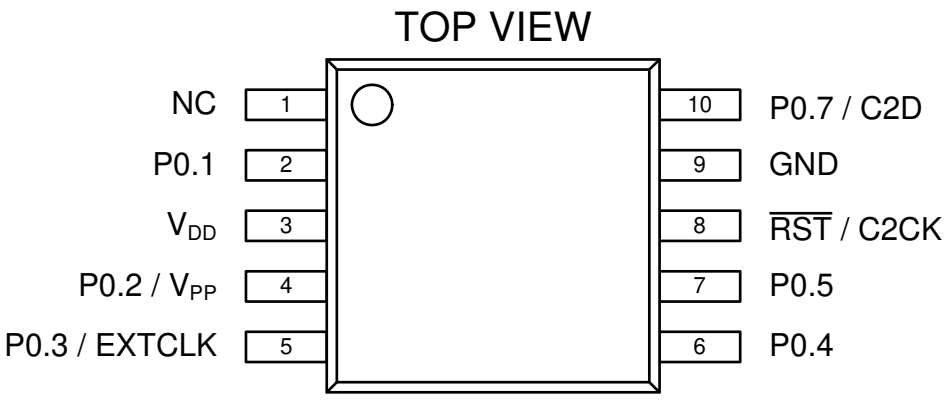

Figure 3.4. C8051T606-GT MSOP10 Pinout Diagram (Top View)

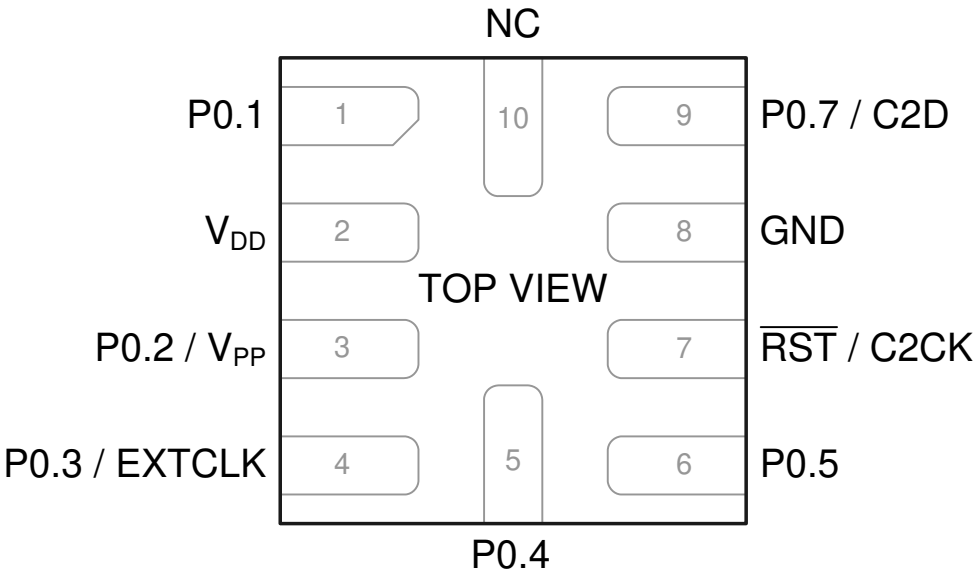

Figure 3.5. C8051T606-ZM QFN10 Pinout Diagram (Top View)

4. QFN-11 Package Specifications

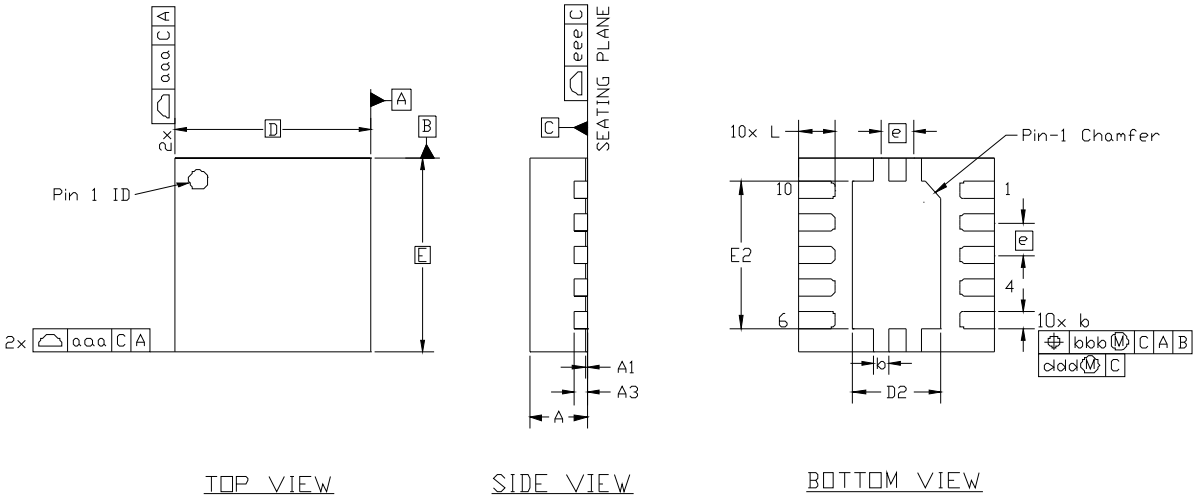

Figure 4.1. QFN-11 Package Drawing

Table 4.1. QFN-11 Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.90	1.00
A1	0.03	0.07	0.11
A3		0.25 REF	
b	0.18	0.25	0.30
D		3.00 BSC	
D2	1.30	1.35	1.40
e		0.50 BSC	

Dimension	Min	Nom	Max
E		3.00 BSC	
E2	2.20	2.25	2.30
L	0.45	0.55	0.65
aaa	—	—	0.15
bbb	—	—	0.15
ddd	—	—	0.05
eee	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-243, variation VEED except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

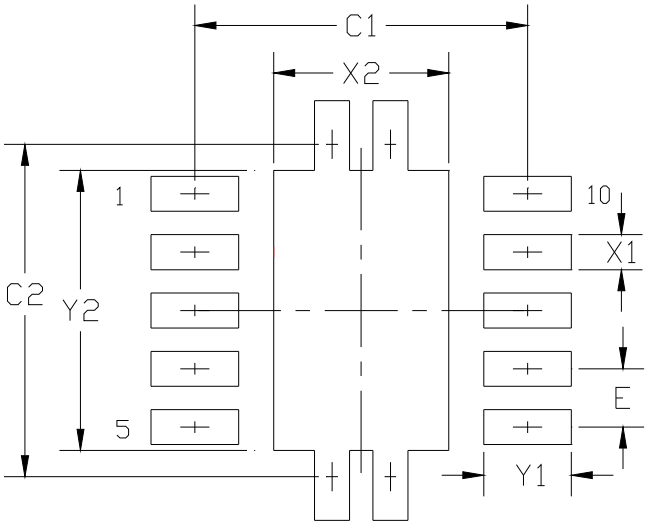

Figure 4.2. QFN-11 PCB Land Pattern

Table 4.2. QFN-11 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	2.75	2.85
C2	2.75	2.85
E	0.50 BSC	
X1	0.20	0.30

Dimension	Min	Max
X2	1.40	1.50
Y1	0.65	0.75
Y2	2.30	2.40

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
7. A 3 x 1 array of 1.30 x 0.60 mm openings on 0.80 mm pitch should be used for the center pad.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5. SOIC-14 Package Specifications

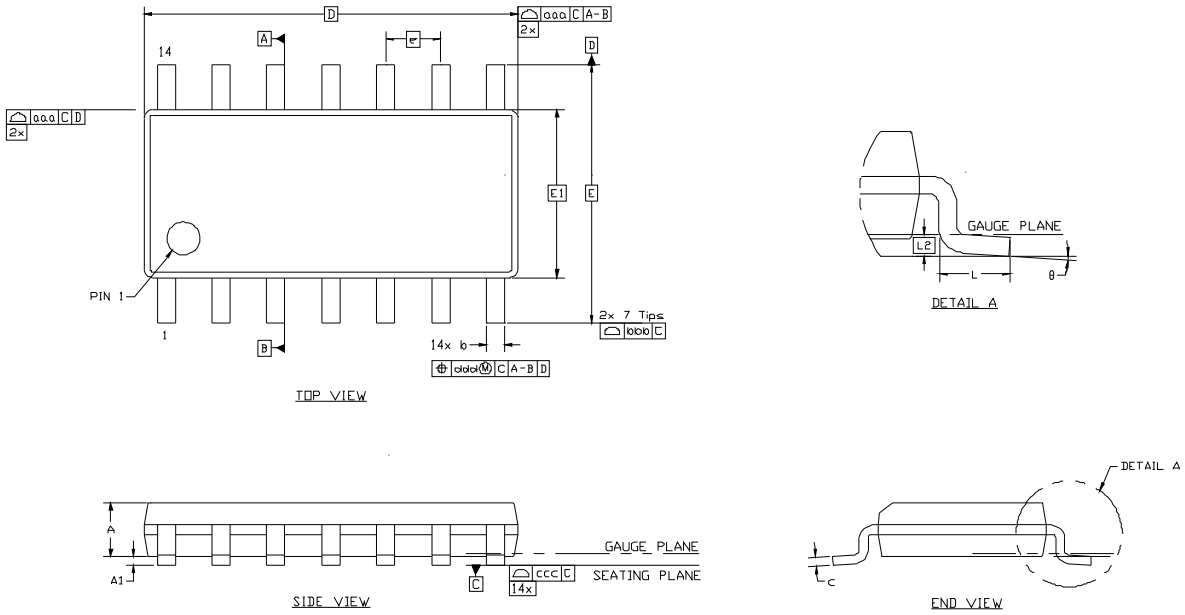

Figure 5.1. SOIC-14 Package Drawing

Table 5.1. SOIC-14 Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.33	—	0.51
c	0.17	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		

Dimension	Min	Nom	Max
L	0.40	—	1.27
L2	0.25 BSC		
θ	0°	—	8°
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		

Notes:
1. All dimensions shown are in millimeters (mm).
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS012, variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

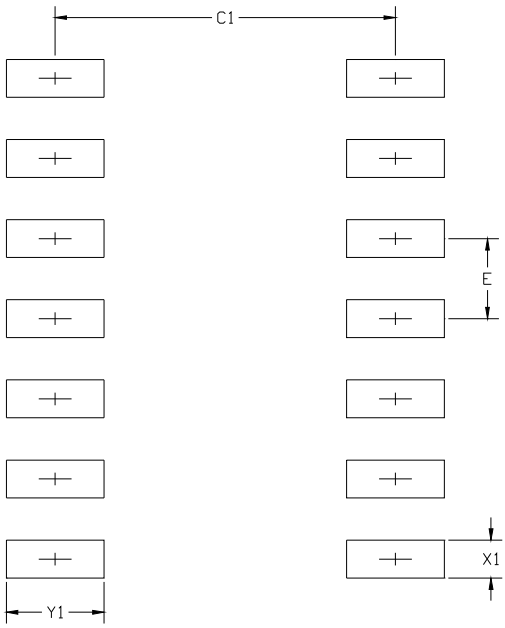

Figure 5.2. SOIC-14 Recommended PCB Land Pattern

Table 5.2. SOIC-14 PCB Land Pattern Dimensions

Dimension	Min	Max	Dimension	Min	Max
C1	5.30	5.40	X1	0.50	0.60
E	1.27 BSC		Y1	1.45	1.55

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

Card Assembly

7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.