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C8051T610/1/2/3/4/5/6/7

Mixed-Signal Byte-Programmable EPROM MCU

Analog Peripherals
- **10-Bit ADC ('T610/1/2/3/6 only)**
  - Up to 500 ksps
  - Up to 21, 17, or 13 external inputs
  - VREF from external pin, Internal Regulator or V_{DD}
  - Internal or external start of conversion source
  - Built-in temperature sensor
- **Comparators**
  - Programmable hysteresis and response time
  - Configurable as interrupt sources
  - Configurable as reset source (Comparator 0)
  - Low current (<0.5 µA)

On-Chip Debug
- C8051F310 can be used as code development platform; Complete development kit available
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug
- Provides breakpoints, single stepping, inspect/modify memory and registers

Supply Voltage 1.8 to 3.6 V
- On-chip LDO for internal core supply
- Built-in voltage supply monitor

Memory
- 1280 Bytes internal data RAM (256 + 1024)
- 16 or 8 kB byte-programmable EPROM code memory

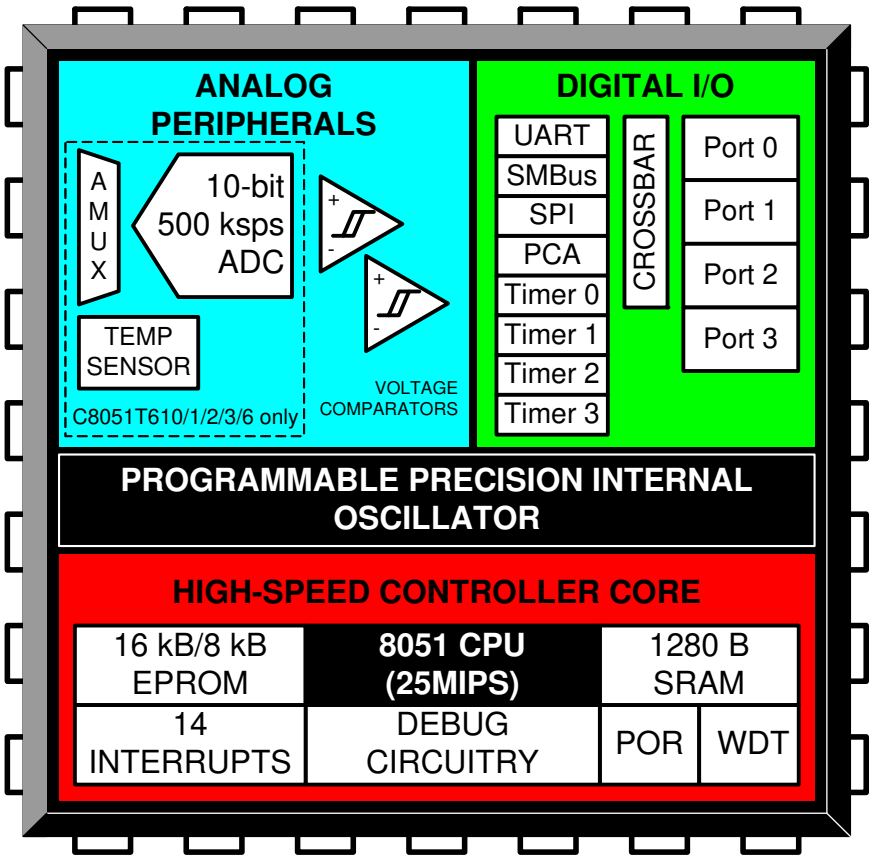
Temperature Range: –40 to +85 °C

High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

Digital Peripherals
- 29/25/21 Port I/O with high sink current capability
- Hardware enhanced UART, SMBus™, and enhanced SPI™ serial ports
- Four general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with five capture/compare modules and PWM functionality

Clock Sources
- Internal oscillator: 24.5 MHz with ±2% accuracy supports crystal-less UART operation
- External oscillator: RC, C, or CMOS Clock
- Can switch between clock sources on-the-fly; useful in power saving modes

Packages
- 32-pin LQFP (C8051T610/2/4)
- 28-pin QFN (C8051T611/3/5)
- 24-pin QFN (C8051T616/7)



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1. System Overview

C8051T610/1/2/3/4/5/6/7 devices are fully integrated, mixed-signal, system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 2.1 for specific product feature selection and part ordering numbers.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- C8051F310 ISP Flash device is available for quick in-system code development
- 10-bit 500 ksps Single-ended ADC with analog multiplexer and integrated temperature sensor
- Precision calibrated 24.5 MHz internal oscillator
- 16 k or 8 k of on-chip Byte-Programmable EPROM—(512 bytes are reserved on 16k version)
- 1280 bytes of on-chip RAM
- SMBus/I^2C, SPI, and Enhanced UART serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with five capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset and V_{DD} Monitor
- On-chip Voltage Comparators (2)
- 29/25/21 Port I/O

With on-chip power-on reset, V_{DD} monitor, watchdog timer, and clock oscillator, the C8051T610/1/2/3/4/5/6/7 devices are truly stand-alone, system-on-a-chip solutions. User software has complete control of all peripherals and may individually shut down any or all peripherals for power savings.

Code written for the C8051T610/1/2/3/4/5/6/7 family of processors will run on the C8051F310 Mixed-Signal ISP Flash microcontroller, providing a quick, cost-effective way to develop code without requiring special emulator circuitry. The C8051T610/1/2/3/4/5/6/7 processors include Silicon Laboratories' 2-Wire C2 Debug and Programming interface, which allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection of memory, viewing and modification of special function registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 1.8–3.6 V operation over the industrial temperature range (–45 to +85 °C). An internal LDO is used to supply the processor core voltage. The Port I/O and $\overline{RST}$ pins are tolerant of input signals up to 5 V. See Table 2.1 for ordering information. Block diagrams of the devices in the C8051T610/1/2/3/4/5/6/7 family are shown in Figure 1.1, Figure 1.2 and Figure 1.3.

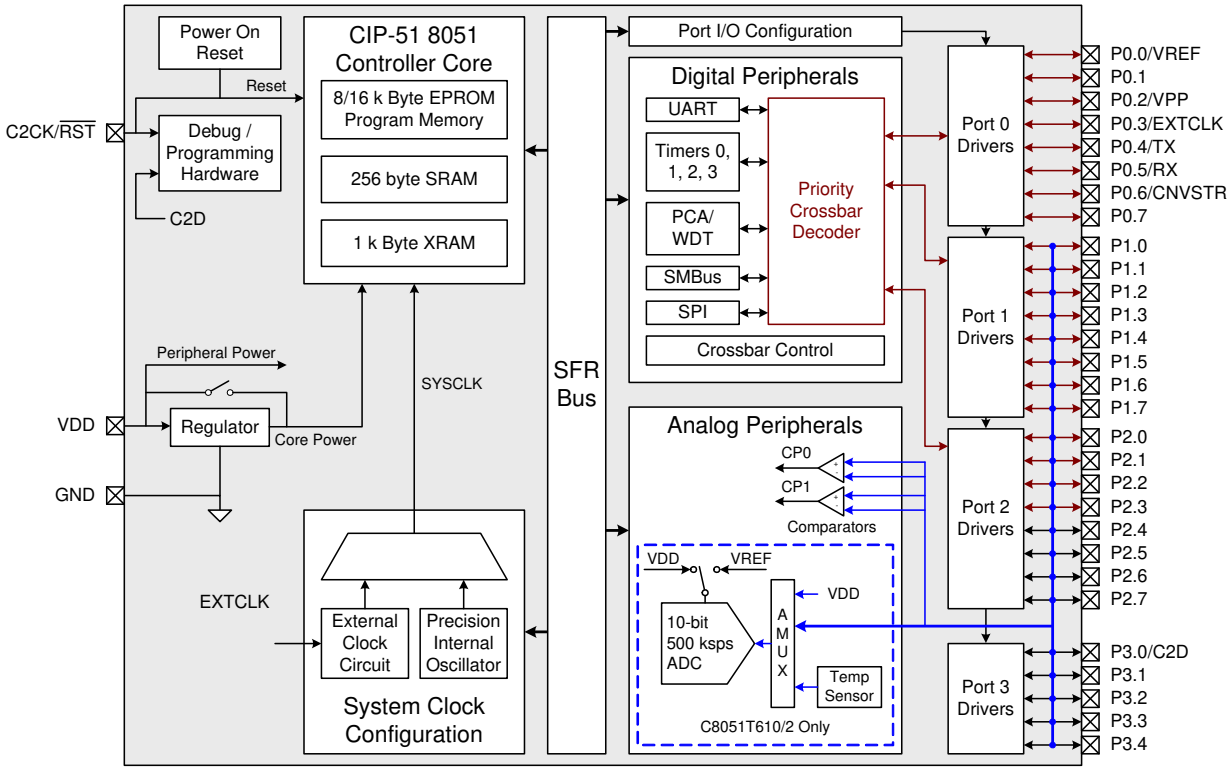

Figure 1.1. C8051T610/2/4 Block Diagram (32-pin LQFP)

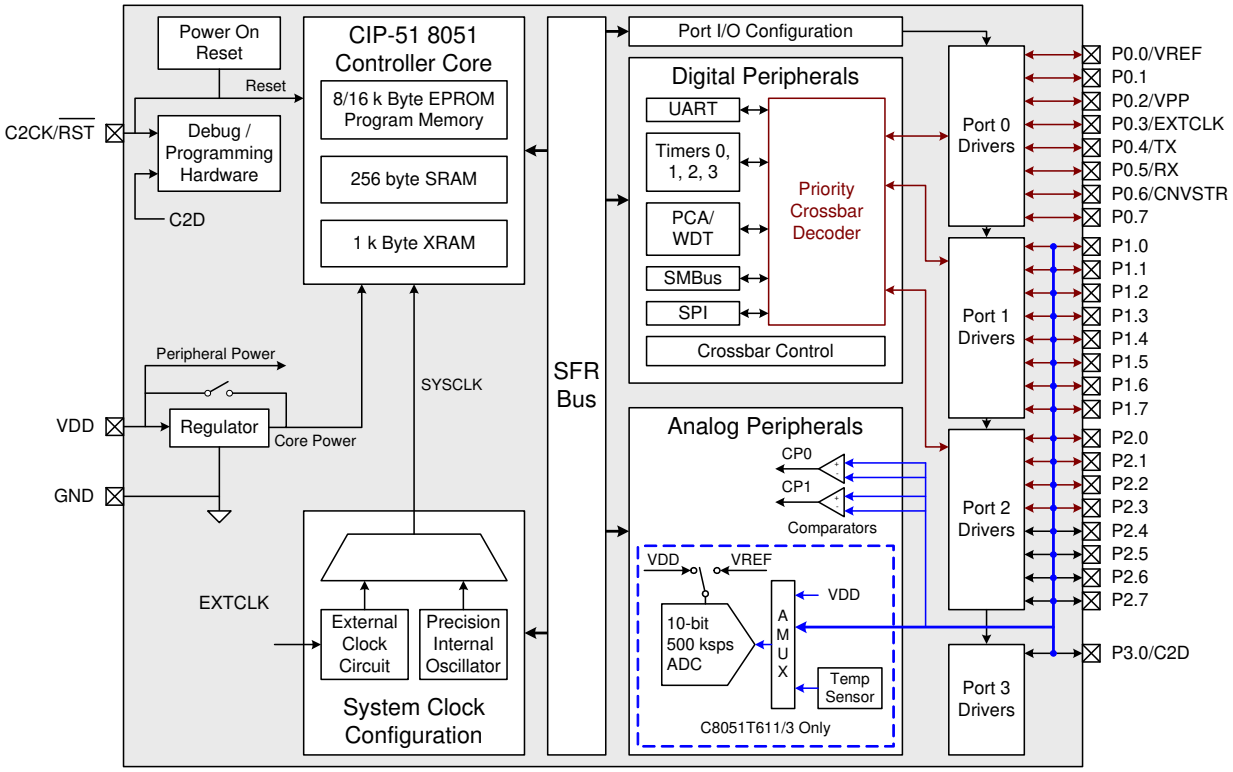

Figure 1.2. C8051T611/3/5 Block Diagram (28-pin QFN)

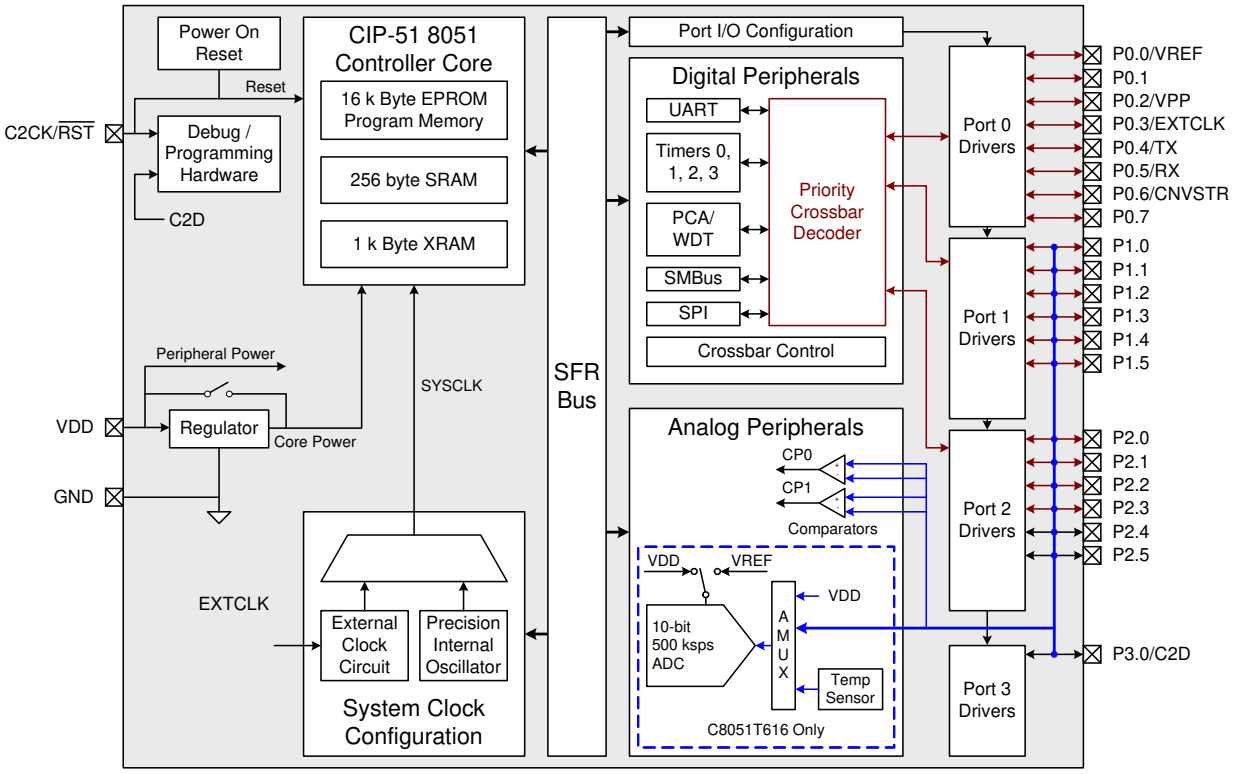

Figure 1.3. C8051T616/7 Block Diagram (24-pin QFN)

2. Ordering Information

Table 2.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	EPROM Memory (Bytes)	RAM (Bytes)	Calibrated Internal 24.5 MHz Oscillator	SMBus/I^2C	Enhanced SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 500ksps ADC	Temperature Sensor	Analog Comparators	Lead-free (RoHS Compliant)	Package
C8051T610-GQ	25	16k*	1280	Y	Y	Y	Y	4	Y	29	Y	Y	2	Y	LQFP-32
C8051T611-GM	25	16k*	1280	Y	Y	Y	Y	4	Y	25	Y	Y	2	Y	QFN-28
C8051T612-GQ	25	8k	1280	Y	Y	Y	Y	4	Y	29	Y	Y	2	Y	LQFP-32
C8051T613-GM	25	8k	1280	Y	Y	Y	Y	4	Y	25	Y	Y	2	Y	QFN-28
C8051T614-GQ	25	8k	1280	Y	Y	Y	Y	4	Y	29	—	—	2	Y	LQFP-32
C8051T615-GM	25	8k	1280	Y	Y	Y	Y	4	Y	25	—	—	2	Y	QFN-28
C8051T616-GM	25	16k*	1280	Y	Y	Y	Y	4	Y	21	Y	Y	2	Y	QFN-24
C8051T617-GM	25	16k*	1280	Y	Y	Y	Y	4	Y	21	—	—	2	Y	QFN-24
* 512 Bytes Reserved for Factory Use															

3. Pin Definitions

Table 3.1. Pin Definitions for the C8051T610/1/2/3/4/5/6/7

Name	Pin T610/2/4	Pin T611/3/5	Pin T616/7	Type	Description
V_{DD}	4	4	4		Power Supply Voltage.
GND	3	3	3		Ground.
$\overline{RST}$/ C2CK	5	5	5	D I/O D I/O	Device Reset. Open-drain output of internal POR. Clock signal for the C2 Debug Interface.
P3.0/ C2D	6	6	6	D I/O or A In D I/O	Port 3.0. Bi-directional data signal for the C2 Debug Interface.
P0.0	2	2	2	D I/O or A In	Port 0.0.
P0.1	1	1	1	D I/O or A In	Port 0.1.
P0.2/ VPP	32	28	24	D I/O or A In A In	Port 0.2. VPP Programming Voltage Input.
P0.3	31	27	23	D I/O or A in	Port 0.3.
P0.4	30	26	22	D I/O or A In	Port 0.4.
P0.5	29	25	21	D I/O or A In	Port 0.5.
P0.6	28	24	20	D I/O or A In	Port 0.6.
P0.7	27	23	19	D I/O	Port 0.7.
P1.0	26	22	18	D I/O or A In	Port 1.0.
P1.1	25	21	17	D I/O or A In	Port 1.1.
P1.2	24	20	16	D I/O or A In	Port 1.2.

Table 3.1. Pin Definitions for the C8051T610/1/2/3/4/5/6/7(Continued)

Name	Pin T610/2/4	Pin T611/3/5	Pin T616/7	Type	Description
P1.3	23	19	15	D I/O or A In	Port 1.3.
P1.4	22	18	14	D I/O or A In	Port 1.4.
P1.5	21	17	13	D I/O or A In	Port 1.5.
P1.6	20	16	—	D I/O or A In	Port 1.6.
P1.7	19	15	—	D I/O or A In	Port 1.7.
P2.0	18	14	12	D I/O or A In	Port 2.0.
P2.1	17	13	11	D I/O or A In	Port 2.1.
P2.2	16	12	10	D I/O or A In	Port 2.2.
P2.3	15	11	9	D I/O or A In	Port 2.3.
P2.4	14	10	8	D I/O or A In	Port 2.4.
P2.5	13	9	7	D I/O or A In	Port 2.5.
P2.6	12	8	—	D I/O or A In	Port 2.6.
P2.7	11	7	—	D I/O or A In	Port 2.7.
P3.1	7	—	—	D I/O or A In	Port 3.1.
P3.2	8	—	—	D I/O or A In	Port 3.2.
P3.3	9	—	—	D I/O or A In	Port 3.3.
P3.4	10	—	—	D I/O or A In	Port 3.4.

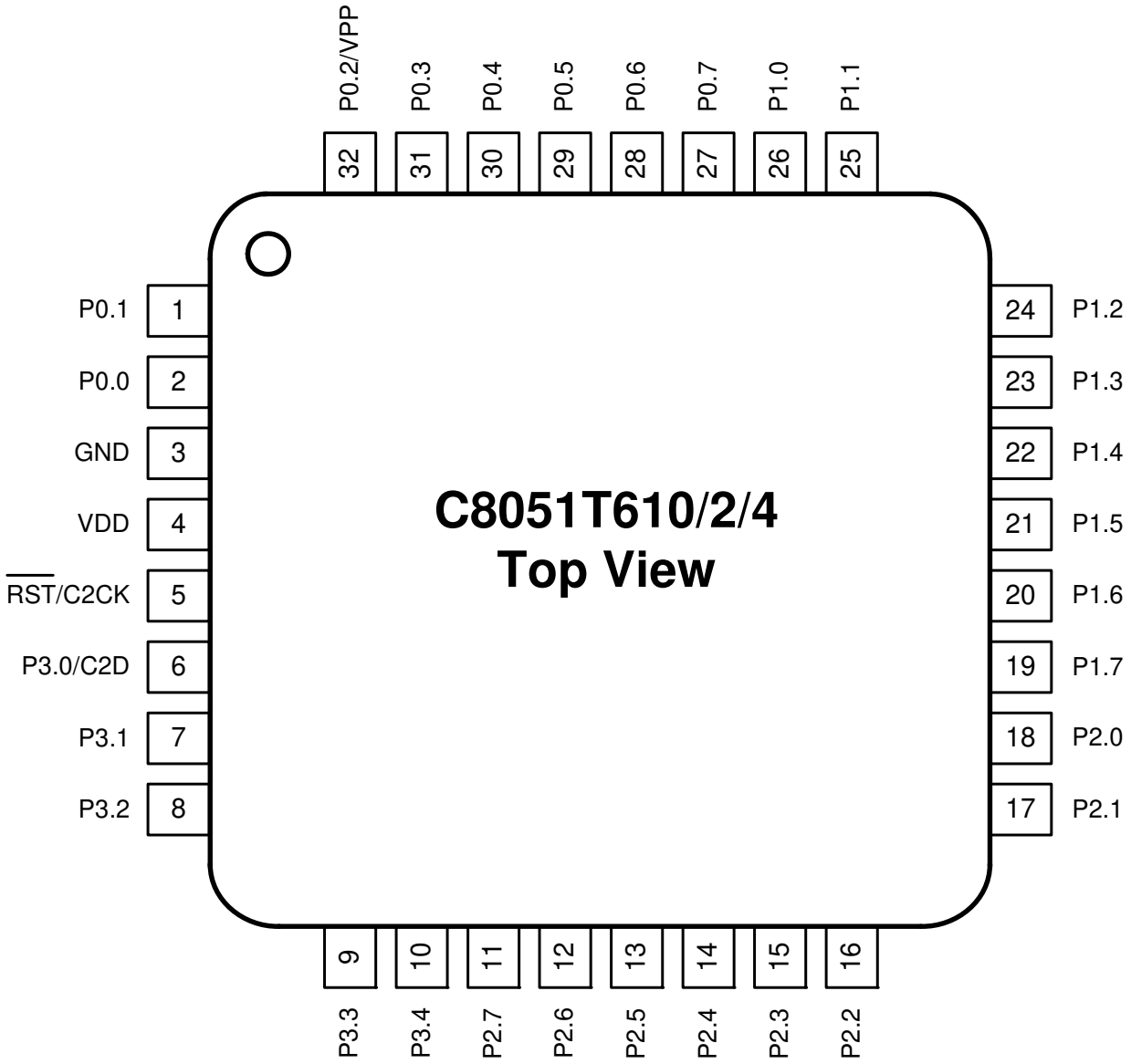

Figure 3.1. LQFP-32 Pinout Diagram (Top View)

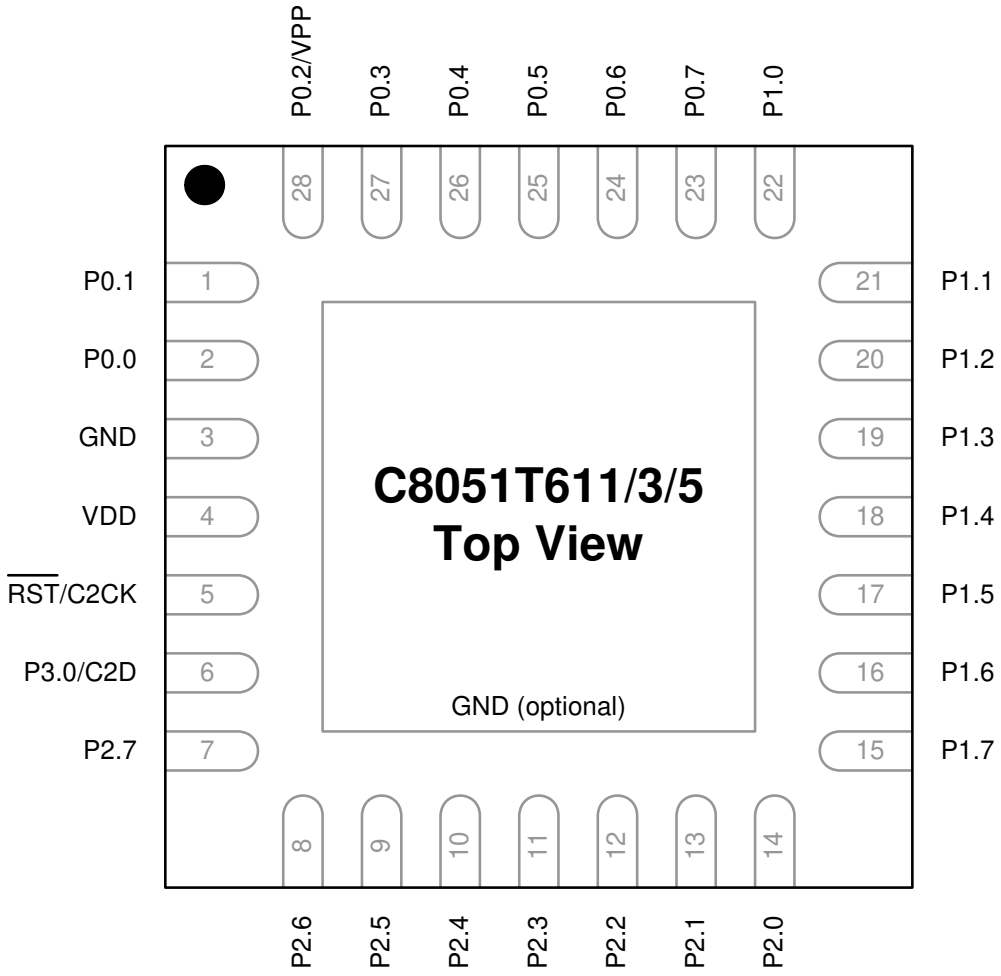

Figure 3.2. QFN-28 Pinout Diagram (Top View)

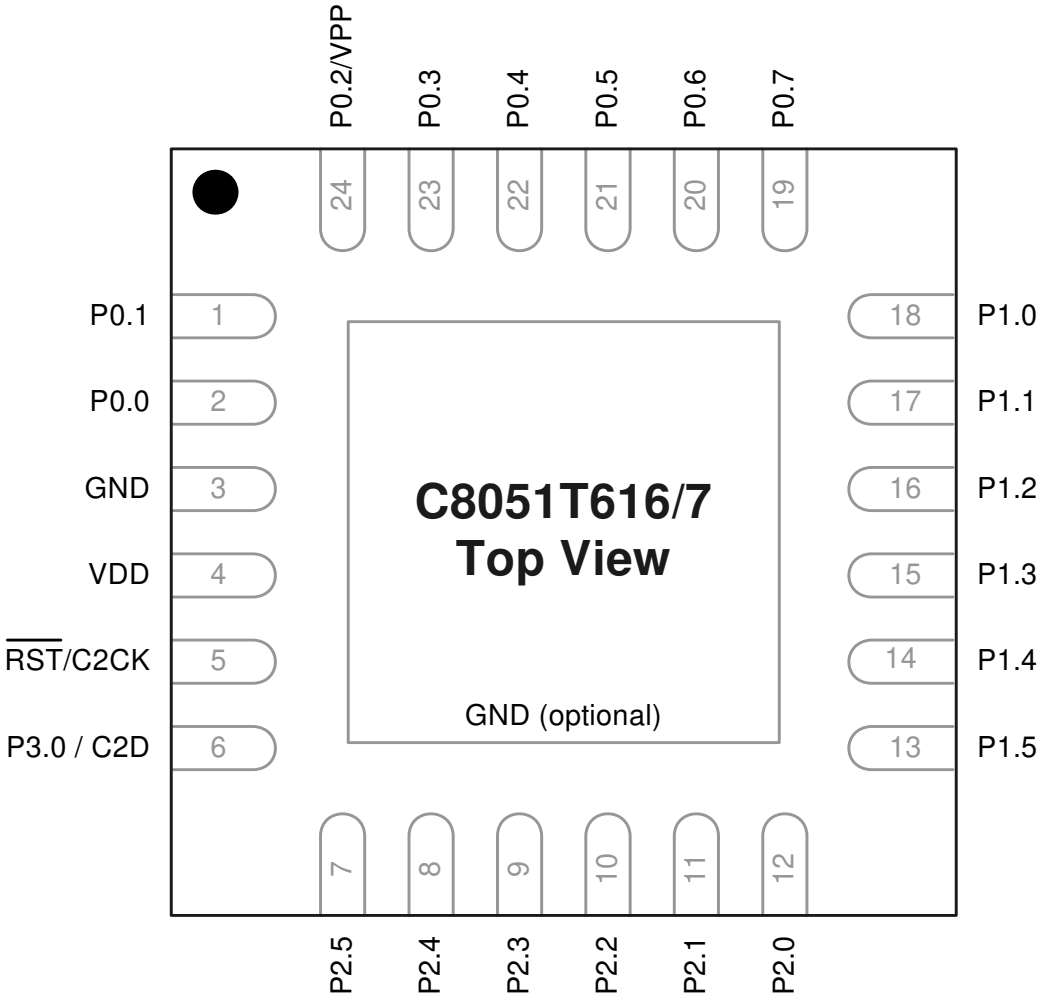

Figure 3.3. QFN-24 Pinout Diagram (Top View)

4. LQFP-32 Package Specifications

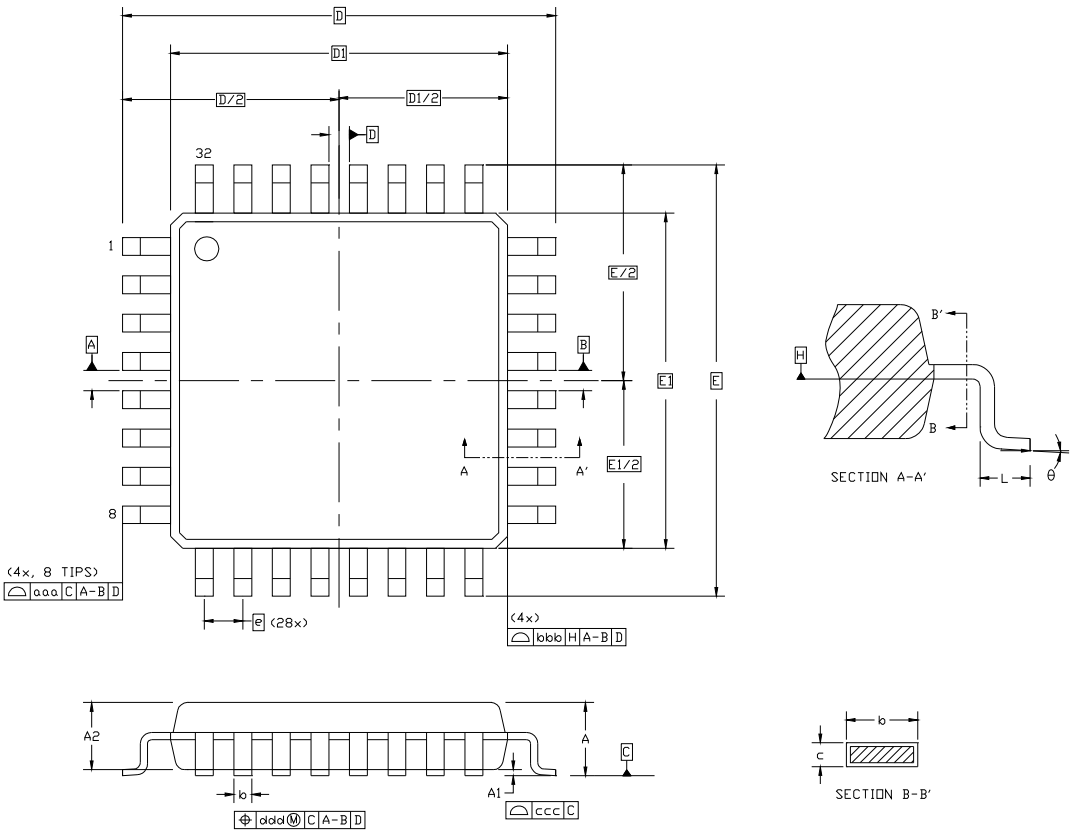

Figure 4.1. LQFP-32 Package Drawing

Table 4.1. LQFP-32 Package Dimensions

Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	—	—	1.60	E	9.00 BSC.		
A1	0.05	—	0.15	E1	7.00 BSC.		
A2	1.35	1.40	1.45	L	0.45	0.60	0.75
b	0.30	0.37	0.45	aaa	0.20		
c	0.09	—	0.20	bbb	0.20		
D	9.00 BSC.			ccc	0.10		
D1	7.00 BSC.			ddd	0.20		
e	0.80 BSC.			θ	0°	3.5°	7°

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.