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CAP1105 / CAP1106

5 and 6 Channel Capacitive Touch Sensor

PRODUCT FEATURES

Datasheet

General Description

The CAP1106 and CAP1105, which incorporate SMSC's RightTouch® [1] technology, are multiple channel Capacitive Touch sensors. The CAP1106 contains six (6) individual capacitive touch sensor inputs while the CAP1105 contains five (5) sensor inputs. Both devices offer programmable sensitivity for use in touch sensor applications. Each sensor input automatically recalibrates to compensate for gradual environmental changes.

The CAP1105 / CAP1106 includes Multiple Pattern Touch recognition that allows the user to select a specific set of buttons to be touched simultaneously. If this pattern is detected, then a status bit is set and an interrupt generated.

Additionally, the CAP1105 / CAP1106 includes circuitry and support for enhanced sensor proximity detection.

The CAP1105 / CAP1106 offers multiple power states operating at low quiescent currents. In the Standby state of operation, one or more capacitive touch sensor inputs are active.

Deep Sleep is the lowest power state available, drawing 5uA (typical) of current. In this state, no sensor inputs are active. Communications will wake the device.

Applications

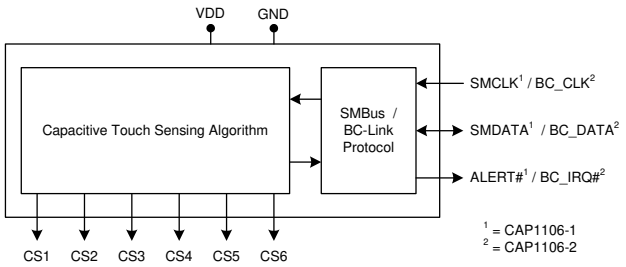
- Desktop and Notebook PCs
- LCD Monitors
- Consumer Electronics
- Appliances

Features

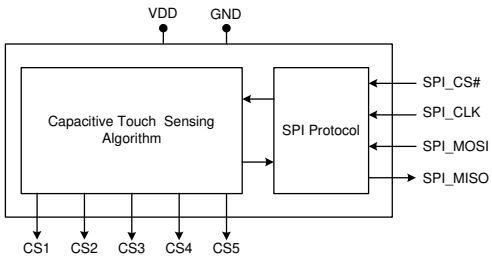
- Six (6) Capacitive Touch Sensor Inputs - CAP1106
- Five (5) Capacitive Touch Sensor Inputs - CAP1105
  - Programmable sensitivity
  - Automatic recalibration
  - Individual thresholds for each button
- Proximity Detection
- Multiple Button Pattern Detection
- Calibrates for Parasitic Capacitance
- Analog Filtering for System Noise Sources
- Press and Hold feature for Volume-like Applications
- Multiple Communication Interfaces
  - SMBus / I^2C compliant interface (CAP1106-1 only)
  - SMSC BC-Link interface (CAP1106-2 only)
  - SPI communications (CAP1105 only)
- Low Power Operation
  - 5uA quiescent current in Deep Sleep
  - 50uA quiescent current in Standby (1 sensor input monitored)
  - Samples one or more channels in Standby
- Available in 10-pin 3mm x 3mm RoHS compliant DFN package

1. SMSC, the SMSC logo and RightTouch are registered trademarks and the RightTouch logo is a trademark of Standard Microsystems Corporation ("SMSC").

CAP1106 BLOCK DIAGRAM



CAP1105 BLOCK DIAGRAM



Ordering Information:

ORDERING NUMBER	PACKAGE	FEATURES
CAP1106-1-AIA-TR	10-pin DFN 3mm x 3mm (Lead-free RoHS compliant)	Six capacitive touch sensor inputs, SMBus interface
CAP1106-2-AIA-TR	10-pin DFN 3mm x 3mm (Lead-free RoHS compliant)	Six capacitive touch sensor inputs, BC-Link interface
CAP1105-1-AIA-TR	10-pin DFN 3mm x 3mm (Lead-free RoHS compliant)	Five capacitive touch sensor inputs, Full Duplex SPI interface

Reel size is 4,000 pieces

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

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Chapter 1 Pin Description

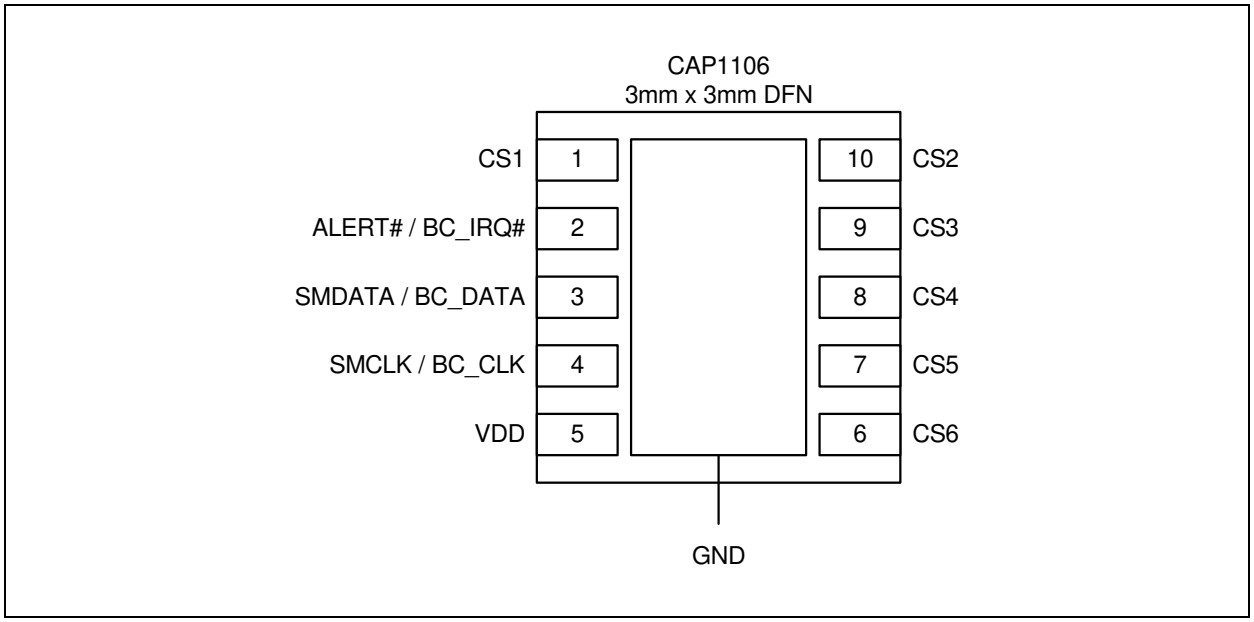

Figure 1.1 CAP1106 Pin Diagram (10-Pin DFN)

Table 1.1 Pin Description for CAP1106

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE	UNUSED CONNECTION
1	CS1	Capacitive Touch Sensor Input 1	AIO	Connect to Ground
2	ALERT# / BC_IRQ#	ALERT# - Active low alert / interrupt output for SMBus alert (CAP1106-1)	OD (5V)	Connect to Ground
		ALERT# - Active high alert / interrupt output for SMBus alert (CAP1106-1)	DO	leave open
		BC_IRQ# - Active low interrupt / optional for BC-Link (CAP1106-2)	OD (5V)	Connect to Ground
		BC_IRQ# - Active high push-pull interrupt / optional for BC-Link (CAP1106-2)	DO	leave open
3	SMDATA / BC_DATA	SMDATA - Bi-directional, open-drain SMBus data - requires pull-up resistor (CAP1106-1)	DIOD (5V)	n/a
		BC_DATA - Bi-directional, open-drain BC-Link data - requires pull-up resistor (CAP1106-2)	DIO	
4	SMCLK / BC_CLK	SMCLK - SMBus clock input - requires pull-up resistor (CAP1106-1)	DI (5V)	n/a
		BC_CLK - BC-Link clock input (CAP1106-2)	DI (5V)	

Table 1.1 Pin Description for CAP1106 (continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE	UNUSED CONNECTION
5	VDD	Positive Power supply	Power	n/a
6	CS6	Capacitive Touch Sensor Input 6	AIO	Connect to Ground
7	CS5	Capacitive Touch Sensor Input 5	AIO	Connect to Ground
8	CS4	Capacitive Touch Sensor Input 4	AIO	Connect to Ground
9	CS3	Capacitive Touch Sensor Input 3	AIO	Connect to Ground
10	CS2	Capacitive Touch Sensor Input 2	AIO	Connect to Ground
Bottom Pad	GND	Ground	Power	n/a

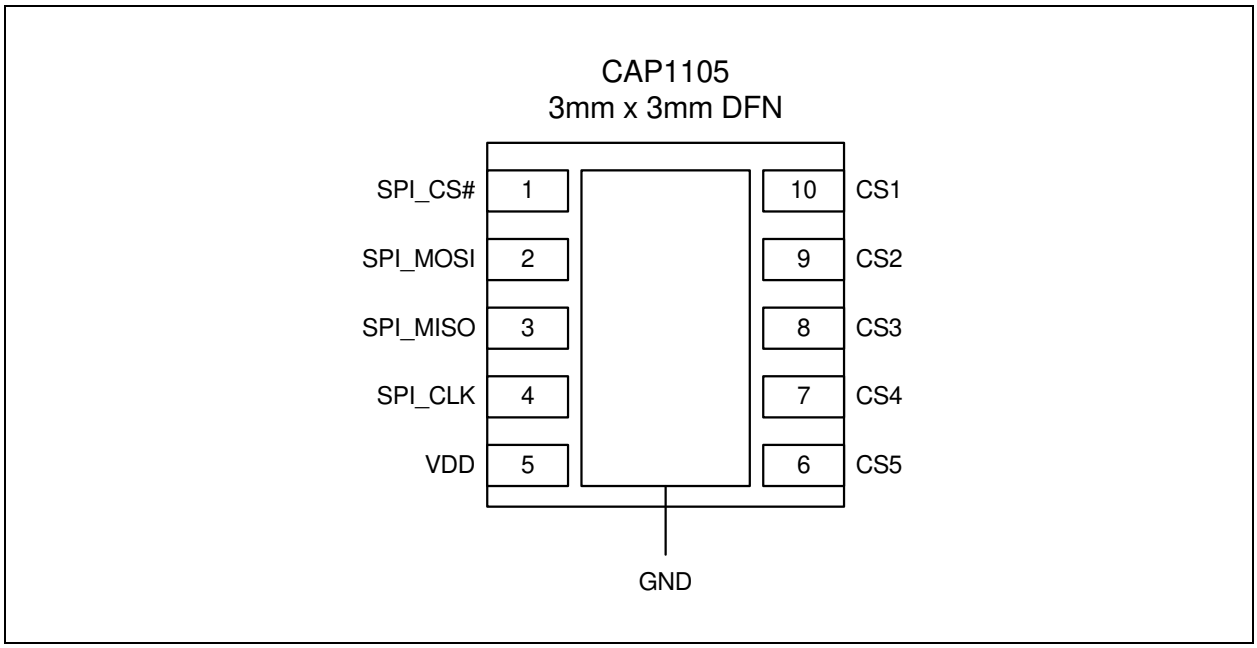

Figure 1.2 CAP1105 Pin Diagram (10-Pin DFN)

Table 1.2 Pin Description for CAP1105

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE	UNUSED CONNECTION
1	SPI_CS#	Active low chip-select for SPI bus	DI (5V)	n/a
2	SPI_MOSI	SPI_MOSI - SPI Master-Out-Slave-In port	DI (5V)	n/a

Table 1.2 Pin Description for CAP1105 (continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE	UNUSED CONNECTION
3	SPI_MISO	SPI Master-In-Slave-Out data port	DO	n/a
4	SPI_CLK	SPI clock input	DI (5V)	n/a
5	VDD	Positive Power supply	Power	n/a
6	CS5	Capacitive Touch Sensor Input 5	AIO	Connect to Ground
7	CS4	Capacitive Touch Sensor Input 4	AIO	Connect to Ground
8	CS3	Capacitive Touch Sensor Input 3	AIO	Connect to Ground
9	CS2	Capacitive Touch Sensor Input 2	AIO	Connect to Ground
10	CS1	Capacitive Touch Sensor Input 1	AIO	Connect to Ground
Bottom Pad	GND	Ground	Power	n/a

APPLICATION NOTE: When the ALERT# pin (CAP1106 only) is configured as an active low output, it will be open drain. When it is configured as an active high output, it will be push-pull.

APPLICATION NOTE: For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the CAP1105 / CAP1106 is unpowered.

The pin types are described in Table 1.3. All pins labeled with (5V) are 5V tolerant.

Table 1.3 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
DI	Digital Input - This pin is used as a digital input. This pin is 5V tolerant.
AIO	Analog Input / Output -This pin is used as an I/O for analog signals.
DIOD	Digital Input / Open Drain Output - This pin is used as a digital I/O. When it is used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output - This pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.
DO	Push-pull Digital Output - This pin is used as a digital output and can sink and source current.
DIO	Push-pull Digital Input / Output - This pin is used as an I/O for digital signals.

Chapter 2 Electrical Specifications

Table 2.1 Absolute Maximum Ratings

Voltage on 5V tolerant pins (V_{5VT_PIN})	-0.3 to 5.5	V
Voltage on 5V tolerant pins ($\|V_{5VT\_PIN} - V_{DD}\|$) Note 2.2	0 to 3.6	V
Voltage on VDD pin	-0.3 to 4	V
Voltage on any other pin to GND	-0.3 to VDD + 0.3	V
Package Power Dissipation up to T_A = 85°C for 10 pin DFN (see Note 2.3)	0.7	W
Junction to Ambient (θ_{JA})	77.7	°C/W
Operating Ambient Temperature Range	-40 to 125	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating, All Pins, HBM	8000	V

Note 2.1 Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note 2.2 For the 5V tolerant pins that have a pull-up resistor, the voltage difference between V_{5VT_PIN} and V_{DD} must never exceed 3.6V.

Note 2.3 The Package Power Dissipation specification assumes a recommended thermal via design consisting of a 2x2 matrix of 0.3mm (12mil) vias at 1.0mm pitch connected to the ground plane with a 1.6 x 2.3mm thermal landing.

Table 2.2 Electrical Specifications

V_{DD} = 3V to 3.6V, T_A = 0°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	

Table 2.2 Electrical Specifications (continued)

V_{DD} = 3V to 3.6V, T_A = 0°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Supply Current	I_{STBY}		120	170	uA	Standby state active 1 sensor input monitored Default conditions (8 avg, 70ms cycle time)
	I_{STBY}		50		uA	Standby state active 1 sensor input monitored 1 avg, 140ms cycle time,
	I_{DSLEEP}		5	15	uA	Deep Sleep state active No communications T_A < 40°C 3.135 < V_{DD} < 3.465V
	I_{DD}		500	600	uA	Capacitive Sensing Active
Capacitive Touch Sensor Inputs						
Maximum Base Capacitance	C_{BASE}		50		pF	Pad untouched
Minimum Detectable Capacitive Shift	ΔC_{TOUCH}	20			fF	Pad touched - default conditions (1 avg, 35ms cycle time, 1x sensitivity)
Recommended Cap Shift	ΔC_{TOUCH}	0.1		2	pF	Pad touched - Not tested
Power Supply Rejection	PSR		±3	±10	counts / V	Untouched Current Counts Base Capacitance 5pF - 50pF Maximum sensitivity Negative Delta Counts disabled All other parameters default
Timing						
Time to communications ready	t_{COMM_DLY}			15	ms	
Time to first conversion ready	t_{CONV_DLY}		170	200	ms	
I/O Pins						
Output Low Voltage	V_{OL}			0.4	V	I_{SINK_IO} = 8mA
Output High Voltage	V_{OH}	V_{DD} - 0.4			V	I_{SOURCE_IO} = 8mA
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Leakage Current	I_{LEAK}			±5	uA	powered or unpowered T_A < 85°C pull-up voltage ≤ 3.6V if unpowered
SMBus Timing (CAP1106-1 only)						

Table 2.2 Electrical Specifications (continued)

V_{DD} = 3V to 3.6V, T_A = 0°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Input Capacitance	C_{IN}		5		pF	
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus Free Time Stop to Start	t_{BUF}	1.3			us	
Start Setup Time	$t_{SU:STA}$	0.6			us	
Start Hold Time	$t_{HD:STA}$	0.6			us	
Stop Setup Time	$t_{SU:STO}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0			us	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3			us	When receiving from the master
Data Setup Time	$t_{SU:DAT}$	0.6			us	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock / Data Fall Time	t_{FALL}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Clock / Data Rise Time	t_{RISE}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Capacitive Load	C_{LOAD}			400	pF	per bus line
BC-Link Timing (CAP1106-2 only)						
Clock Period	t_{CLK}	250			ns	
Data Hold Time	$t_{HD:DAT}$	0			ns	
Data Setup Time	$t_{SU:DAT}$	30			ns	Data must be valid before clock
Clock Duty Cycle	Duty	40	50	60	%	
SPI Timing (CAP1105 only)						
Clock Period	t_P	250			ns	
Clock Low Period	t_{LOW}	0.4 x t_P		0.6 x t_P	ns	
Clock High Period	t_{HIGH}	0.4 x t_P		0.6 x t_P	ns	
Clock Rise / Fall time	t_{RISE} / t_{FALL}			0.1 x t_P	ns	
Data Output Delay	$t_{D:CLK}$			10	ns	
Data Setup Time	$t_{SU:DAT}$	20			ns	
Data Hold Time	$t_{HD:DAT}$	20			ns	

Table 2.2 Electrical Specifications (continued)

V_{DD} = 3V to 3.6V, T_A = 0°C to 85°C, all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
SPI_CS# to SPI_CLK setup time	$t_{SU:CS}$	0			ns	
Wake Time	t_{WAKE}	10		20	us	SPI_CS# asserted to CLK assert

Note 2.4 The ALERT pin will not glitch high or low at power up if connected to VDD or another voltage.

Note 2.5 The SMCLK and SMDATA pins will not glitch low at power up if connected to VDD or another voltage.

Chapter 3 Communications

3.1 Communications

The CAP1106-1 communicates using the SMBus or I^2C protocol. The CAP1106-2 communicates using the 2-wire proprietary BC-Link protocol. The CAP1105 communicates using 4-wire SPI bus. Regardless of the communications mechanism, the device functionality remains unchanged.

3.1.1 SMBus (I^2C) Communications

The CAP1106-1 supports the following protocols: Send Byte, Receive Byte, Read Byte, Write Byte, Read Block, and Write Block. In addition, the device supports I^2C formatting for block read and block write protocols.

See Section 3.2 and Section 3.3 for more information on the SMBus bus and protocols respectively.

3.1.2 SPI Communications

The CAP1105 is configured to communicate via SPI bus, using a 4-wire protocol. It does not support the 3-wire protocol.

See Section 3.5 and Section 3.6 for more information on the SPI bus and protocols respectively.

3.1.3 BC-Link Communications

The CAP1106-2 supports the read byte protocol and the write byte protocol.

See Section 3.7 for more information on the BC-Link Bus and protocols respectively.

APPLICATION NOTE: Upon power up, the CAP1106-2 will not respond to any communications for up to 15ms. After this time, full functionality is available.

3.2 System Management Bus

The CAP1106-1 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 3.1. Stretching of the SMCLK signal is supported; however, the CAP1106-1 will not stretch the clock signal.

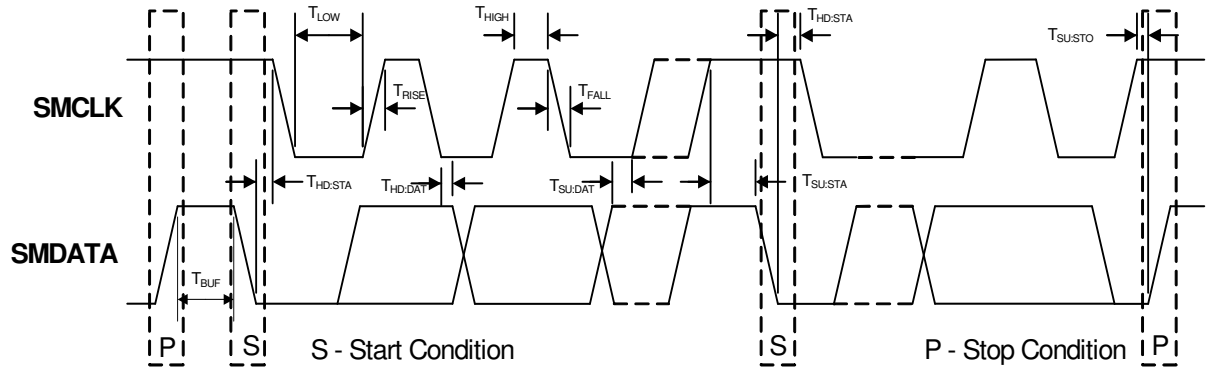

Figure 3.1 SMBus Timing Diagram

3.2.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic ‘1’ state to a logic ‘0’ state while the SMBus Clock line is in a logic ‘1’ state.

3.2.2 SMBus Address and RD / $\overline{WR}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by the RD / $\overline{WR}$ indicator bit. If this RD / $\overline{WR}$ bit is a logic ‘0’, then the SMBus Host is writing data to the client device. If this RD / $\overline{WR}$ bit is a logic ‘1’, then the SMBus Host is reading data from the client device.

The CAP1106-1 responds to SMBus address 0101_000(r/w).

3.2.3 SMBus Data Bytes

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

3.2.4 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives. This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted. This applies to both the Write Byte and Block Write protocols.

The Host will NACK (not acknowledge) the last data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent. For the Block Read protocol, the Host will ACK each data byte that it receives except the last data byte.

3.2.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic ‘0’ state to a logic ‘1’ state while the SMBus clock line is in a logic ‘1’ state. When the CAP1106-1 detects an SMBus Stop bit and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

3.2.6 SMBus Timeout

The CAP1106-1 includes an SMBus timeout feature. Following a 30ms period of inactivity on the SMBus where the SMCLK pin is held low, the device will timeout and reset the SMBus interface.

The timeout function defaults to disabled. It can be enabled by setting the TIMEOUT bit in the Configuration register (see Section 5.6, "Configuration Registers").

3.2.7 SMBus and I²C Compatibility

The major differences between SMBus and I²C devices are highlighted here. For more information, refer to the SMBus 2.0 and I²C specifications. For information on using the CAP1106-1 in an I²C system, refer to SMSC AN 14.0 SMSC Dedicated Slave Devices in I²C Systems.

1. CAP1106-1 supports I²C fast mode at 400kHz. This covers the SMBus max time of 100kHz.
2. Minimum frequency for SMBus communications is 10kHz.
3. The SMBus client protocol will reset if the clock is held at a logic '0' for longer than 30ms. This timeout functionality is disabled by default in the CAP1106-1 and can be enabled by writing to the TIMEOUT bit. I²C does not have a timeout.
4. The SMBus client protocol will reset if both the clock and data lines are held at a logic '1' for longer than 200µs (idle condition). This function is disabled by default in the CAP1106-1 and can be enabled by writing to the TIMEOUT bit. I²C does not have an idle condition.
5. I²C devices do not support the Alert Response Address functionality (which is optional for SMBus).
6. I²C devices support block read and write differently. I²C protocol allows for unlimited number of bytes to be sent in either direction. The SMBus protocol requires that an additional data byte indicating number of bytes to read / write is transmitted. The CAP1106-1 supports I²C formatting only.

3.3 SMBus Protocols

The CAP1106-1 is SMBus 2.0 compatible and supports Write Byte, Read Byte, Send Byte, and Receive Byte as valid protocols as shown below.

All of the below protocols use the convention in Table 3.1.

Table 3.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
Data sent	Data sent

3.3.1 SMBus Write Byte

The Write Byte is used to write one byte of data to a specific register as shown in Table 3.2.

Table 3.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 ->0	0101_000	0	0	XXh	0	XXh	0	0 -> 1

3.3.2 SMBus Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 3.3.

Table 3.3 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	CLIENT ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1->0	0101_000	0	0	XXh	0	1 ->0	0101_000	1	0	XXh	1	0 -> 1

3.3.3 SMBus Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 3.4.

APPLICATION NOTE: The Send Byte protocol is not functional in Deep Sleep (i.e., DSLEEP bit is set).

Table 3.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1 -> 0	0101_000	0	0	XXh	0	0 -> 1

3.3.4 SMBus Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g., set via Send Byte). This is used for consecutive reads of the same register as shown in Table 3.5.

APPLICATION NOTE: The Receive Byte protocol is not functional in Deep Sleep (i.e., DSLEEP bit is set).

Table 3.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	0101_000	1	0	XXh	1	0 -> 1

3.4 I^2C Protocols

The CAP1106-1 supports I^2C Block Write and Block Read.

The protocols listed below use the convention in Table 3.1.

3.4.1 Block Write

The Block Write is used to write multiple data bytes to a group of contiguous registers as shown in Table 3.6.

APPLICATION NOTE: When using the Block Write protocol, the internal address pointer will be automatically incremented after every data byte is received. It will wrap from FFh to 00h.

Table 3.6 Block Write Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK
1 ->0	0101_000	0	0	XXh	0	XXh	0
REGISTER DATA	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**ACK**	**STOP**
XXh	0	XXh	0	. . .	XXh	0	0 -> 1

3.4.2 Block Read

The Block Read is used to read multiple data bytes from a group of contiguous registers as shown in Table 3.7.

APPLICATION NOTE: When using the Block Read protocol, the internal address pointer will be automatically incremented after every data byte is received. It will wrap from FFh to 00h.

Table 3.7 Block Read Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA
1->0	0101_000	0	0	XXh	0	1 ->0	0101_000	1	0	XXh
ACK	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	0	. . .	XXh	1	0 -> 1

3.5 SPI Interface (CAP1105 only)

The SMBus has a predefined packet structure, the SPI does not. The SPI Bus can operate in two modes of operation, normal 4-wire mode and bi-directional 3-wire mode. The CAP1105 only supports normal 4-wire mode. All SPI commands consist of 8-bit packets sent to a specific slave device (identified by the CS pin).

The SPI bus will latch data on the rising edge of the clock and the clock and data both idle high.

All commands are supported via both operating modes. The supported commands are: Reset Serial interface, set address pointer, write command and read command. Note that all other codes received during the command phase are ignored and have no effect on the operation of the device.

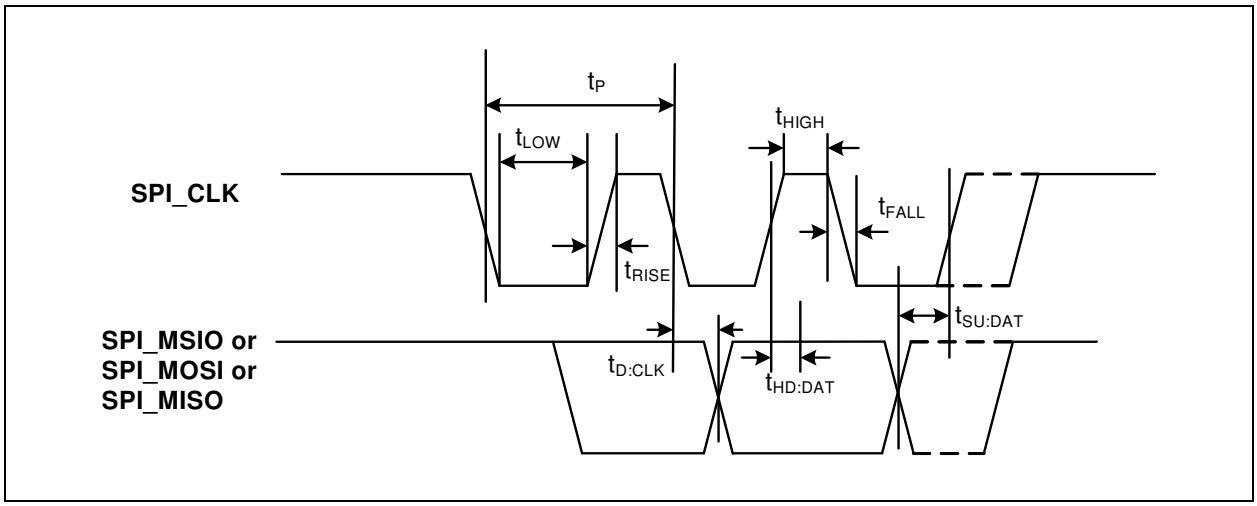

Figure 3.2 SPI Timing

3.5.1 SPI Normal Mode

In the normal mode of operation, there are dedicated input and output data lines. The host communicates by sending a command along the CAP1105 SPI_MOSI data line and reading data on the SPI_MISO data line. Both communications occur simultaneously which allows for larger throughput of data transactions.

All basic transfers consist of two 8 bit transactions from the Master device while the slave device is simultaneously sending data at the current address pointer value.

Data writes consist of two or more 8-bit transactions. The host sends a specific write command followed by the data to write the address pointer. Data reads consist of one or more 8-bit transactions. The host sends the specific read data command and continues clocking for as many data bytes as it wishes to receive.

3.5.2 SPI_CS# Pin

The SPI Bus is a single master, multiple slave serial bus. Each slave has a dedicated CS pin (chip select) that the master asserts low to identify that the slave is being addressed. There are no formal addressing options.

3.5.3 Address Pointer

All data writes and reads are accessed from the current address pointer. In both Bi-directional mode and Full Duplex mode, the Address pointer is automatically incremented following every read command or every write command.

The address pointer will return to 00h after reaching FFh.

3.5.4 SPI Timeout

The CAP1105 does not detect any timeout conditions on the SPI bus.

3.6 Normal SPI Protocols

When operating in normal mode, the SPI bus internal address pointer is incremented depending upon which command has been transmitted. Multiple commands may be transmitted sequentually so long as the SPI_CS# pin is asserted low. Figure 3.3 shows an example of this operation.

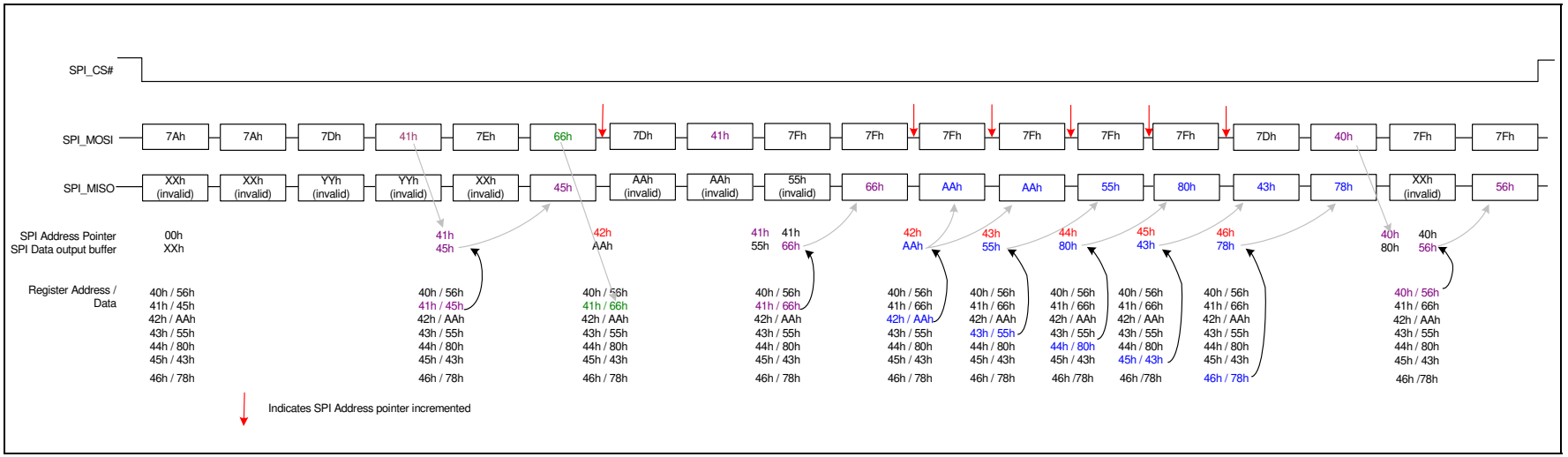

Figure 3.3 Example SPI Bus Communication - Normal Mode

3.6.1 Reset Interface

Resets the Serial interface whenever two successive 7Ah codes are received. Regardless of the current phase of the transaction - command or data, the receipt of the successive reset commands resets the Serial communication interface only. All other functions are not affected by the reset operation.

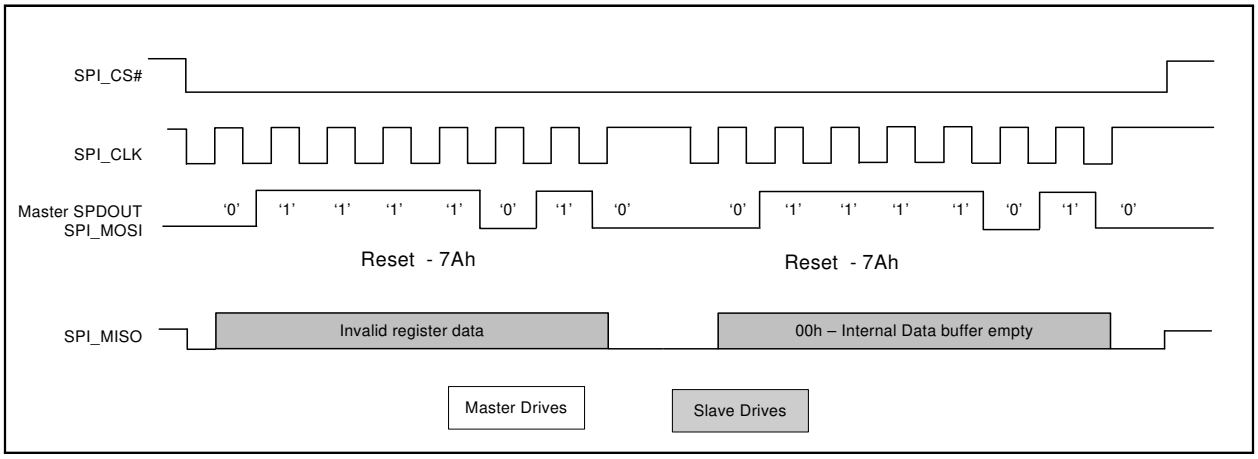

Figure 3.4 SPI Reset Interface Command - Normal Mode

3.6.2 Set Address Pointer

The Set Address Pointer command sets the Address pointer for subsequent reads and writes of data. The pointer is set on the rising edge of the final data bit. At the same time, the data that is to be read is fetched and loaded into the internal output buffer but is not transmitted.

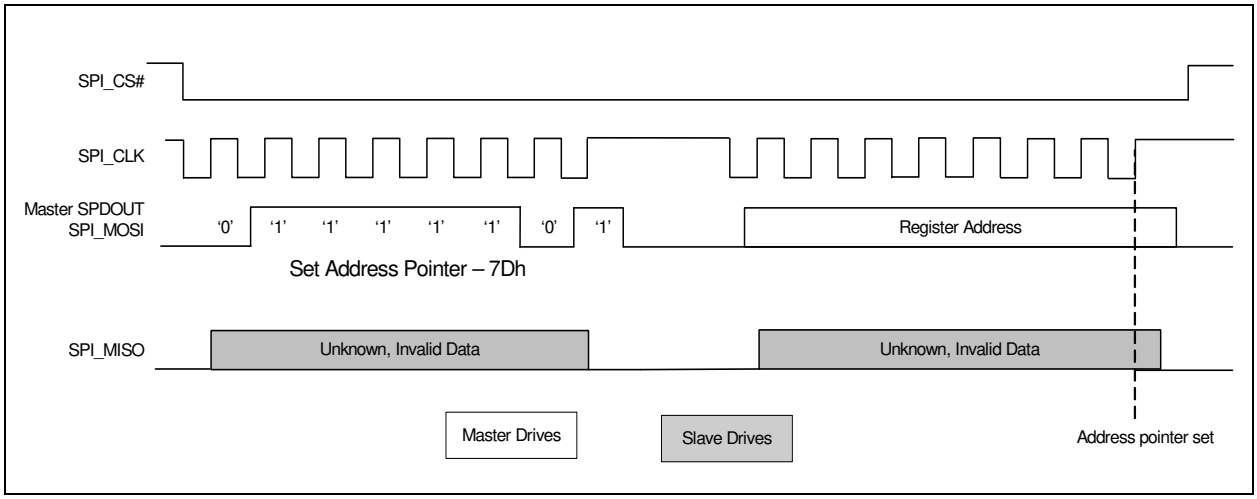

Figure 3.5 SPI Set Address Pointer Command - Normal Mode

3.6.3 Write Data

The Write Data protocol updates the contents of the register referenced by the address pointer. As the command is processed, the data to be read is fetched and loaded into the internal output buffer but not transmitted. Then, the register is updated with the data to be written. Finally, the address pointer is incremented.

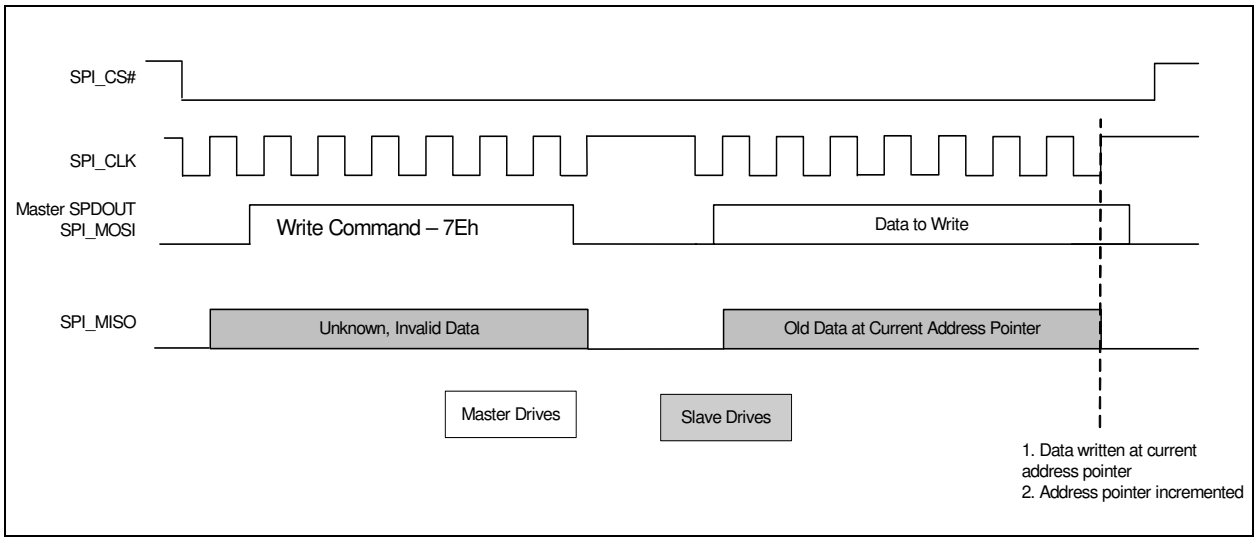

Figure 3.6 SPI Write Command - Normal Mode

3.6.4 Read Data

The Read Data protocol is used to read data from the device. During the normal mode of operation, while the device is receiving data, the CAP1105 is simultaneously transmitting data to the host. For the Set Address commands and the Write Data commands, this data may be invalid and it is recommended that the Read Data command is used.

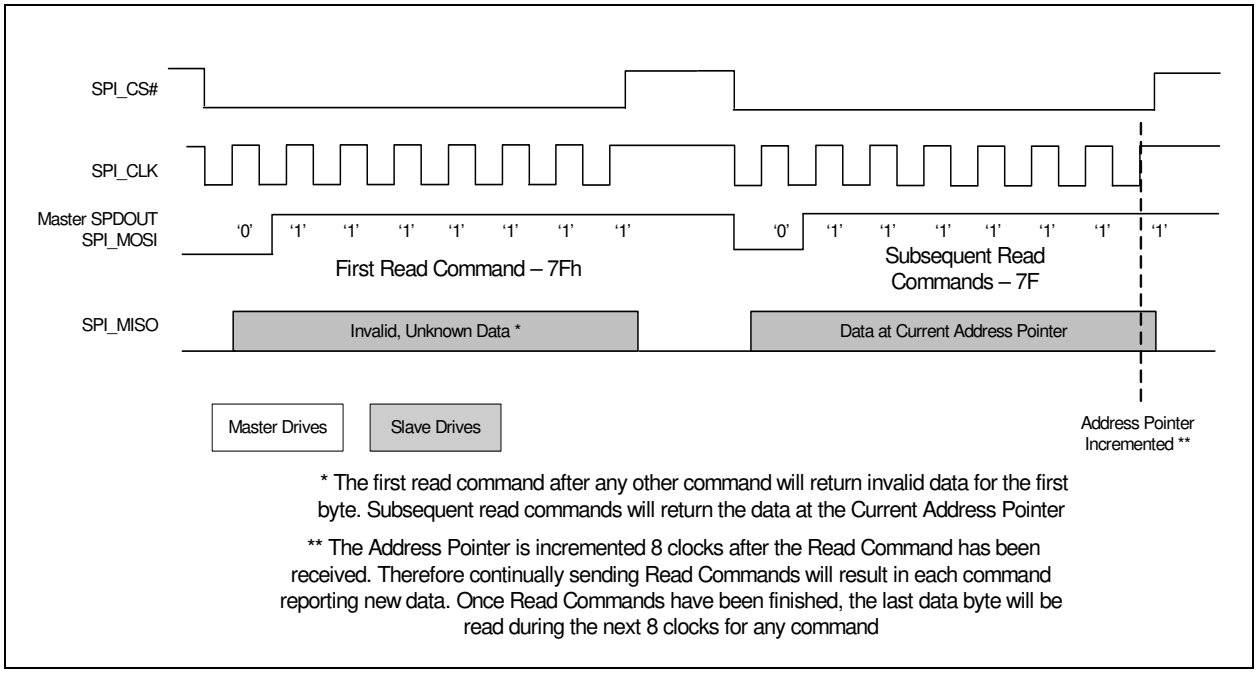

Figure 3.7 SPI Read Command - Normal Mode

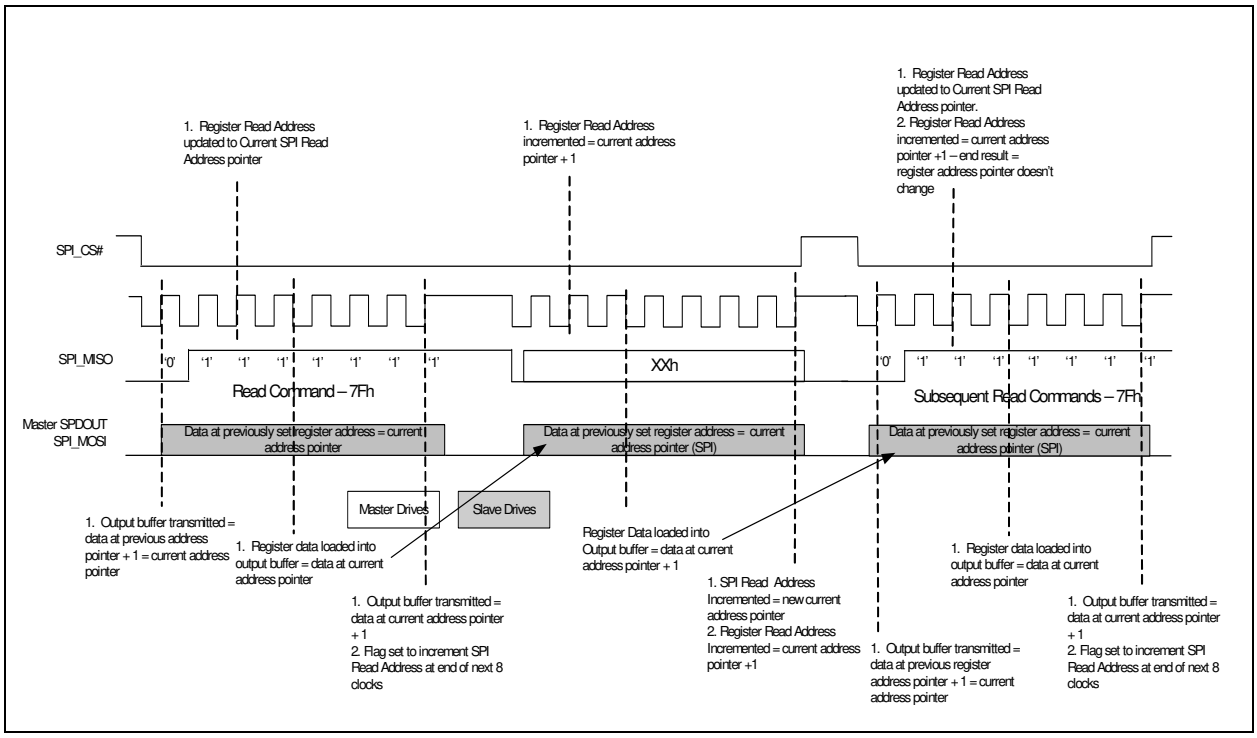

Figure 3.8 SPI Read Command - Normal Mode - Full

3.7 BC-Link Interface (CAP1106-2 only)

The BC-Link is a proprietary bus developed to allow communication between a host controller device to a companion device. This device uses this serial bus to read and write registers and for interrupt processing. The interface uses a data port concept, where the base interface has an address register, data register and a control register, defined in the SMSC's 8051's SFR space.

Refer to documentation for the BC-Link compatible host controller for details on how to access the CAP1106-2 via the BC-Link Interface.