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CAP1166

6 Channel Capacitive Touch Sensor with 6 LED Drivers

General Description

The CAP1166, which incorporates RightTouch® technology, is a multiple channel Capacitive Touch sensor with multiple power LED drivers. It contains six (6) individual capacitive touch sensor inputs with programmable sensitivity for use in touch sensor applications. Each sensor input automatically recalibrates to compensate for gradual environmental changes.

The CAP1166 also contains six (6) LED drivers that offer full-on / off, variable rate blinking, dimness controls, and breathing. Each of the LED drivers may be linked to one of the sensor inputs to be actuated when a touch is detected. As well, each LED driver may be individually controlled via a host controller.

The CAP1166 includes Multiple Pattern Touch recognition that allows the user to select a specific set of buttons to be touched simultaneously. If this pattern is detected, then a status bit is set and an interrupt generated.

Additionally, the CAP1166 includes circuitry and support for enhanced sensor proximity detection.

The CAP1166 offers multiple power states operating at low quiescent currents. In the Standby state of operation, one or more capacitive touch sensor inputs are active and all LEDs may be used. If a touch is detected, it will wake the system using the WAKE/SPI_MOSI pin.

Deep Sleep is the lowest power state available, drawing 5uA (typical) of current. In this state, no sensor inputs are active. Driving the WAKE/SPI_MOSI pin or communications will wake the device.

Applications

- Desktop and Notebook PCs
- LCD Monitors
- Consumer Electronics
- Appliances

Features

- Six (6) Capacitive Touch Sensor Inputs
  - Programmable sensitivity
  - Automatic recalibration
  - Individual thresholds for each button
- Proximity Detection
- Multiple Button Pattern Detection
- Calibrates for Parasitic Capacitance
- Analog Filtering for System Noise Sources
- Press and Hold feature for Volume-like Applications
- Multiple Communication Interfaces
  - SMBus / I^2C compliant interface
  - SPI communications
  - Pin selectable communications protocol and multiple slave addresses (SMBus / I^2C only)
- Low Power Operation
  - 5uA quiescent current in Deep Sleep
  - 50uA quiescent current in Standby (1 sensor input monitored)
  - Samples one or more channels in Standby
- Six (6) LED Driver Outputs
  - Open Drain or Push-Pull
  - Programmable blink, breathe, and dimness controls
  - Can be linked to Capacitive Touch Sensor inputs
- Dedicated Wake output flags touches in low power state
- System RESET pin
- Available in 20-pin 4mm x 4mm QFN or 24-pin SSOP RoHS compliant package

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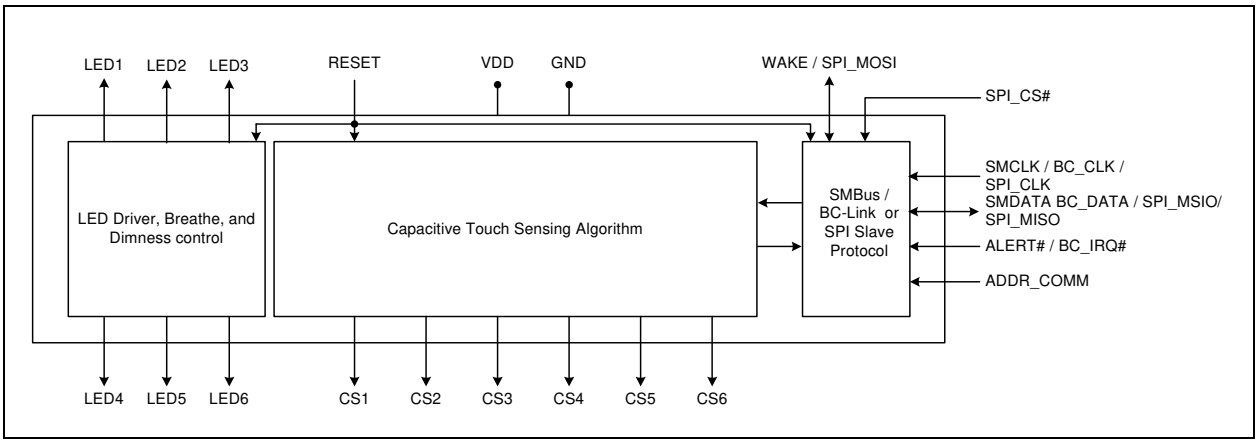
1.0 BLOCK DIAGRAM



2.0 PIN DESCRIPTION

FIGURE 2-1: *CAP1166 Pin Diagram (20-Pin QFN)*

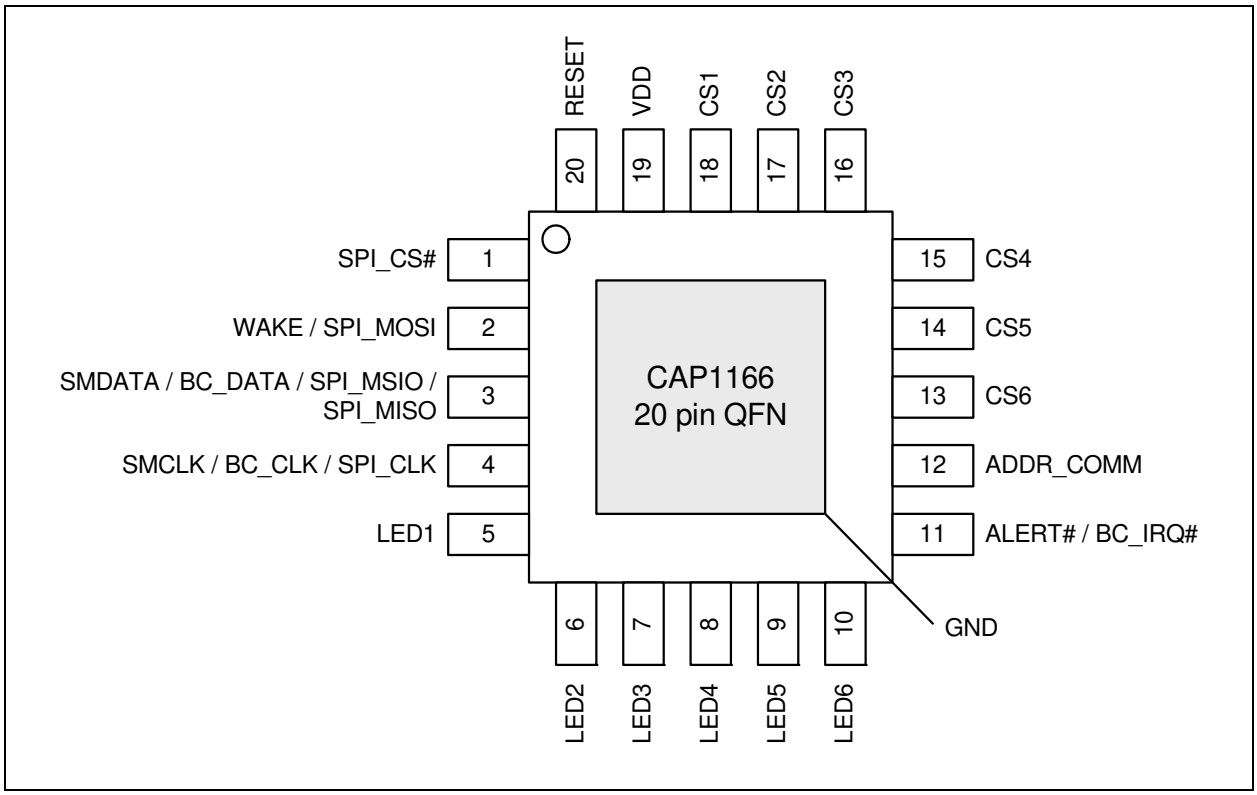


FIGURE 2-2: *CAP1166 Pin Diagram (24-pin SSOP)*

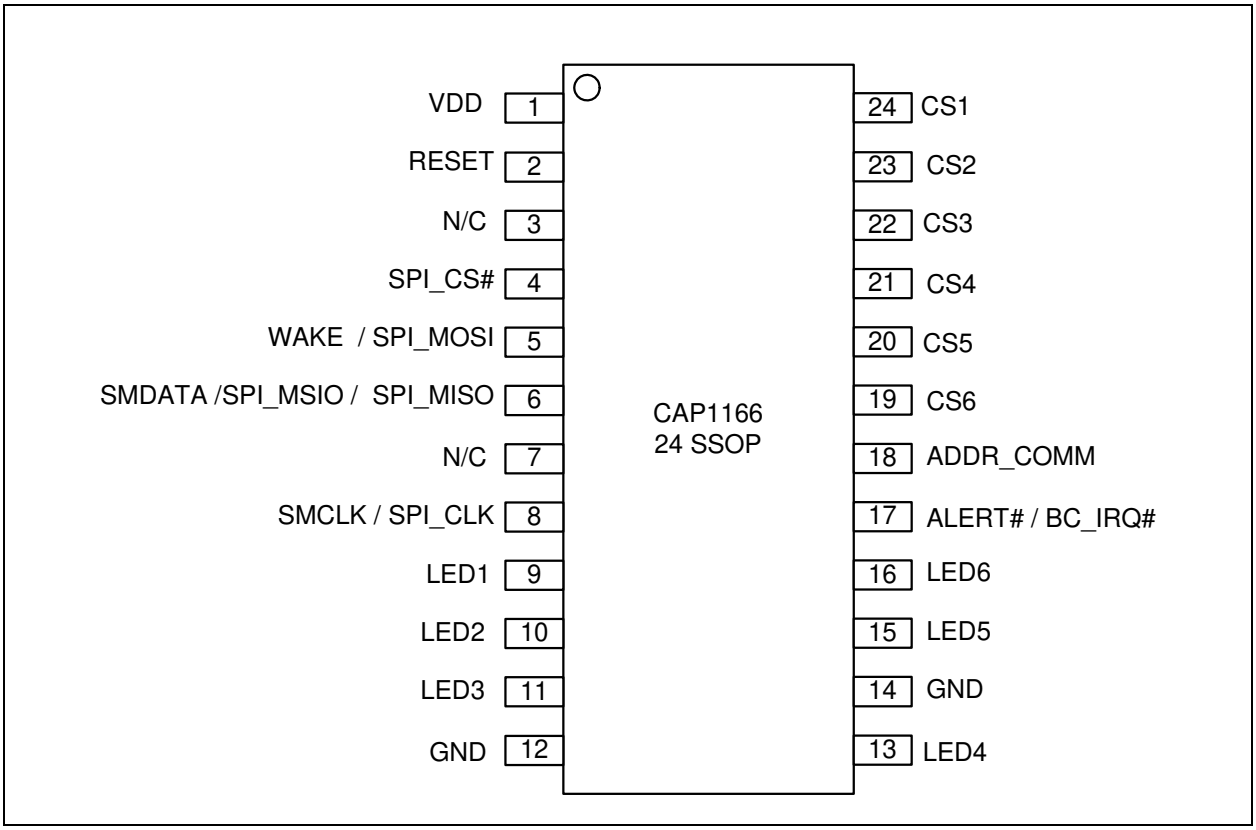


TABLE 2-1: PIN DESCRIPTION FOR CAP1166

Pin Number (QFN 20)	Pin Number (SSOP 24)	Pin Name	Pin Function	Pin Type	Unused Connection
1	4	SPI_CS#	Active low chip-select for SPI bus	DI (5V)	Connect to Ground
2	5	WAKE / SPI_-MOSI	WAKE - Active high wake / interrupt output Standby power state - requires pull-down resistor	DO	Pull-down Resistor
			WAKE - Active high wake input - requires pull-down resistor Deep Sleep power state	DI	
			SPI_MOSI - SPI Master-Out-Slave-In port when used in normal mode	DI (5V)	Connect to GND

TABLE 2-1: PIN DESCRIPTION FOR CAP1166 (CONTINUED)

Pin Number (QFN 20)	Pin Number (SSOP 24)	Pin Name	Pin Function	Pin Type	Unused Connection
3	6	SMDATA / SPI_MSIO / SPI_MISO	SMDATA - Bi-directional, open-drain SMBus data - requires pull-up resistor	DIOD (5V)	n/a
			SPI_MSIO - SPI Master-Slave-In-Out bidirectional port when used in bi-directional mode	DIO	
			SPI_MISO - SPI Master-In-Slave-Out port when used in normal mode	DO	
4	8	SMCLK / SPI_CLK	SMCLK - SMBus clock input - requires pull-up resistor	DI (5V)	n/a
			SPI_CLK - SPI clock input	DI (5V)	
5	9	LED1	Open drain LED 1 driver (default)	OD (5V)	Connect to Ground
			Push-pull LED 1 driver	DO	leave open or connect to Ground
6	10	LED2	Open drain LED 2 driver (default)	OD (5V)	Connect to Ground
			Push-pull LED 2 driver	DO	leave open or connect to Ground
7	11	LED3	Open drain LED 3 driver (default)	OD (5V)	Connect to Ground
			Push-pull LED 3 driver	DO	leave open or connect to Ground
8	13	LED4	Open drain LED 4 driver (default)	OD (5V)	Connect to Ground
			Push-pull LED 4 driver	DO	leave open or connect to Ground
9	15	LED5	Open drain LED 5 driver (default)	OD (5V)	Connect to Ground
			Push-pull LED 5 driver	DO	leave open or connect to Ground
10	16	LED6	Open drain LED 6 driver (default)	OD (5V)	Connect to Ground
			Push-pull LED 6 driver	DO	leave open or connect to Ground

TABLE 2-1: PIN DESCRIPTION FOR CAP1166 (CONTINUED)

Pin Number (QFN 20)	Pin Number (SSOP 24)	Pin Name	Pin Function	Pin Type	Unused Connection
11	17	ALERT#	ALERT# - Active low alert / interrupt output for SMBus alert or SPI interrupt - requires pull-up resistor (default)	OD (5V)	Connect to GND
			ALERT# - Active high push-pull alert / interrupt output for SMBus alert or SPI interrupt	DO	High-Z
12	18	ADDR_ COMM	Address / communications select pin - pull-down resistor determines address / communications mechanism	AI	n/a
13	19	CS6	Capacitive Touch Sensor Input 6	AIO	Connect to Ground
14	20	CS5	Capacitive Touch Sensor Input 5	AIO	Connect to Ground
15	21	CS4	Capacitive Touch Sensor Input 4	AIO	Connect to Ground
16	22	CS3	Capacitive Touch Sensor Input 3	AIO	Connect to Ground
17	23	CS2	Capacitive Touch Sensor Input 2	AIO	Connect to Ground
18	24	CS1	Capacitive Touch Sensor Input 1	AIO	Connect to Ground
19	1	VDD	Positive Power supply	Power	n/a
20	1	RESET	Active high soft reset for system - resets all registers to default values. If not used, connect to ground.	DI (5V)	Connect to Ground
Bottom Pad	12	GND	Ground	Power	n/a
	14	GND	Ground	Power	n/a

APPLICATION NOTE: When the ALERT# pinis configured as an active low output, it will be open drain. When it is configured as an active high output, it will be push-pull.

APPLICATION NOTE: For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the CAP1166 is unpowered.

APPLICATION NOTE: The SPI_CS# pin should be grounded when SMBus, or I^2C,communications are used.

The pin types are described in Table 2-2. All pins labeled with (5V) are 5V tolerant.

TABLE 2-2: PIN TYPES

Pin Type	Description
Power	This pin is used to supply power or ground to the device.
DI	Digital Input - This pin is used as a digital input. This pin is 5V tolerant.
AIO	Analog Input / Output -This pin is used as an I/O for analog signals.
DIOD	Digital Input / Open Drain Output - This pin is used as a digital I/O. When it is used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output - This pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.
DO	Push-pull Digital Output - This pin is used as a digital output and can sink and source current.
DIO	Push-pull Digital Input / Output - This pin is used as an I/O for digital signals.

3.0 ELECTRICAL SPECIFICATIONS

TABLE 3-1: ABSOLUTE MAXIMUM RATINGS

Voltage on 5V tolerant pins (V_{5VT_PIN})	-0.3 to 5.5	V
Voltage on 5V tolerant pins ($\|V_{5VT\_PIN} - V_{DD}\|$) Note 3-2	0 to 3.6	V
Voltage on VDD pin	-0.3 to 4	V
Voltage on any other pin to GND	-0.3 to VDD + 0.3	V
Package Power Dissipation up to T_A = 85°C for 20 pin QFN (see Note 3-3)	0.9	W
Junction to Ambient (θ_{JA}) (see Note 3-4)	58	°C/W
Operating Ambient Temperature Range	-40 to 125	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating, All Pins, HBM	8000	V

Note 3-1 Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note 3-2 For the 5V tolerant pins that have a pull-up resistor, the voltage difference between V_{5VT_PIN} and V_{DD} must never exceed 3.6V.

Note 3-3 The Package Power Dissipation specification assumes a recommended thermal via design consisting of a 3x3 matrix of 0.3mm (12mil) vias at 1.0mm pitch connected to the ground plane with a 2.5 x 2.5mm thermal landing.

Note 3-4 Junction to Ambient (θ_{JA}) is dependent on the design of the thermal vias. Without thermal vias and a thermal landing, the θ_{JA} is approximately 60°C/W including localized PCB temperature increase.

TABLE 3-2: ELECTRICAL SPECIFICATIONS

V_{DD} = 3V to 3.6V, T_A = 0°C to 85°C, all typical values at T_A = 27°C unless otherwise noted.						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Supply Current	I_{STBY}		120	170	uA	Standby state active 1 sensor input monitored No LEDs active Default conditions (8 avg, 70ms cycle time)
	I_{STBY}		50		uA	Standby state active 1 sensor input monitored No LEDs active 1 avg, 140ms cycle time,
	I_{DSLEEP}		5	15	uA	Deep Sleep state active LEDs at 100% or 0% Duty Cycle No communications T_A < 40°C 3.135 < V_{DD} < 3.465V
	I_{DD}		500	600	uA	Capacitive Sensing Active No LEDs active
Capacitive Touch Sensor Inputs						
Maximum Base Capacitance	C_{BASE}		50		pF	Pad untouched
Minimum Detectable Capacitive Shift	ΔC_{TOUCH}	20			fF	Pad touched - default conditions (1 avg, 35ms cycle time, 1x sensitivity)
Recommended Cap Shift	ΔC_{TOUCH}	0.1		2	pF	Pad touched - Not tested
Power Supply Rejection	PSR		±3	±10	counts / V	Untouched Current Counts Base Capacitance 5pF - 50pF Maximum sensitivity Negative Delta Counts disabled All other parameters default
Timing						
RESET Pin Delay	t_{RST_DLY}	10			ms	
Time to communications ready	t_{COMM_DLY}			15	ms	
Time to first conversion ready	t_{CONV_DLY}		170	200	ms	
LED Drivers						
Duty Cycle	$DUTY_{LED}$	0		100	%	Programmable
Drive Frequency	f_{LED}		2		kHz	
Sinking Current	I_{SINK}			24	mA	V_{OL} = 0.4
Sourcing Current	I_{SOURCE}			24	mA	V_{OH} = V_{DD} - 0.4
Leakage Current	I_{LEAK}			±5	uA	powered or unpowered TA < 85°C pull-up voltage ≤ 3.6V if unpowered
I/O Pins						
Output Low Voltage	V_{OL}			0.4	V	I_{SINK_IO} = 8mA
Output High Voltage	V_{OH}	V_{DD} - 0.4			V	I_{SOURCE_IO} = 8mA

TABLE 3-2: ELECTRICAL SPECIFICATIONS (CONTINUED)

V_{DD} = 3V to 3.6V, T_A = 0°C to 85°C, all typical values at T_A = 27°C unless otherwise noted.						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Leakage Current	I_{LEAK}			±5	uA	powered or unpowered T_A < 85°C pull-up voltage ≤ 3.6V if unpowered
RESET Pin Release to conversion ready	t_{RESET}		170	200	ms	
SMBus Timing						
Input Capacitance	C_{IN}		5		pF	
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus Free Time Stop to Start	t_{BUF}	1.3			us	
Start Setup Time	$t_{SU:STA}$	0.6			us	
Start Hold Time	$t_{HD:STA}$	0.6			us	
Stop Setup Time	$t_{SU:STO}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0			us	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3			us	When receiving from the master
Data Setup Time	$t_{SU:DAT}$	0.6			us	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock / Data Fall Time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock / Data Rise Time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}			400	pF	per bus line
SPI Timing						
Clock Period	t_P	250			ns	
Clock Low Period	t_{LOW}	0.4 x t_P		0.6 x t_P	ns	
Clock High Period	t_{HIGH}	0.4 x t_P		0.6 x t_P	ns	
Clock Rise / Fall time	t_{RISE} / t_{FALL}			0.1 x t_P	ns	
Data Output Delay	$t_{D:CLK}$			10	ns	
Data Setup Time	$t_{SU:DAT}$	20			ns	
Data Hold Time	$t_{HD:DAT}$	20			ns	
SPI_CS# to SPI_CLK setup time	$t_{SU:CS}$	0			ns	
Wake Time	t_{WAKE}	10		20	us	SPI_CS# asserted to CLK assert

Note 3-5 The ALERT pin will not glitch high or low at power up if connected to VDD or another voltage.

Note 3-6 The SMCLK and SMDATA pins will not glitch low at power up if connected to VDD or another voltage.

4.0 COMMUNICATIONS

4.1 Communications

The CAP1166communicates using the 2-wire SMBus or I²C bus, the 2-wire proprietary BC-Link, or the SPI bus. If the proprietary BC-Link protocol is required for your application, please contact your Microchip representative for ordering instructions. Regardless of communication mechanism, the device functionality remains unchanged. The communications mechanism as well as the SMBus (or I²C) slave address is determined by the resistor connected between the ADDR_COMM pin and ground as shown in Table 4-1.

TABLE 4-1: ADDR_COMM PIN DECODE

Pull-Down Resistor (+/- 5%)	Protocol Used	SMBus Address
GND	SPI Communications using Normal 4-wire Protocol Used	n/a
56k	SPI Communications using Bi-Directional 3-wire Protocol Used	n/a
68k	Reserved	n/a
82k	SMBus / I²C	0101_100(r/w)
100k	SMBus / I²C	0101_011(r/w)
120k	SMBus / I²C	0101_010(r/w)
150k	SMBus / I²C	0101_001(r/w)
VDD	SMBus / I²C	0101_000(r/w)

4.1.1 SMBUS (I²C) COMMUNICATIONS

When configured to communicate via the SMBus, the CAP1166 supports the following protocols: Send Byte, Receive Byte, Read Byte, Write Byte, Read Block, and Write Block. In addition, the device supports I²C formatting for block read and block write protocols.

APPLICATION NOTE: For SMBus/I²C communications, the SPI_CS# pin is not used and should be grounded; any data presented to this pin will be ignored.

See Section 4.2 and Section 4.3 for more information on the SMBus bus and protocols respectively.

4.1.2 SPI COMMUNICATIONS

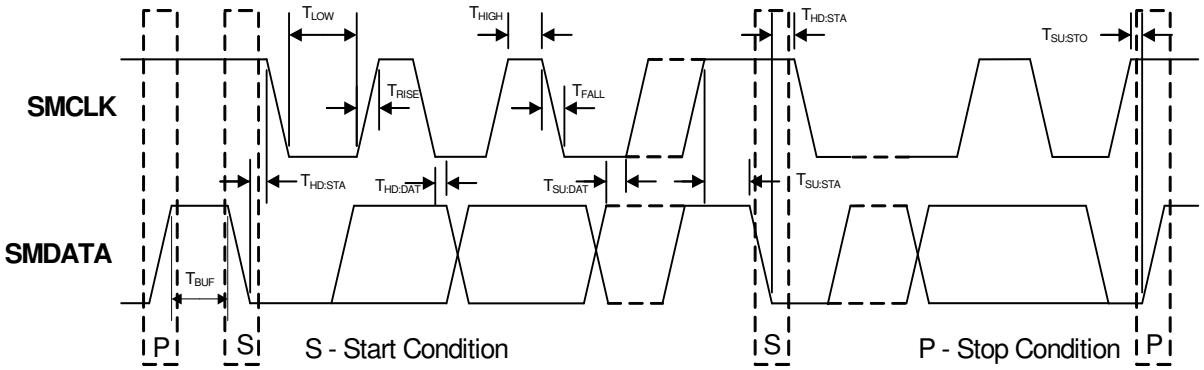
When configured to communicate via the SPI bus, the CAP1166supports both bi-directional 3-wire and normal 4-wire protocols and uses the SPI_CS# pin to enable communications.

APPLICATION NOTE: See Section 4.5 and Section 4.6 for more information on the SPI bus and protocols respectively.Upon power up, the CAP1166 will not respond to any communications for up to 15ms. After this time, full functionality is available.

4.2 System Management Bus

The CAP1166 communicates with a host controller, such as an SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4-1. Stretching of the SMCLK signal is supported; however, the CAP1166 will not stretch the clock signal.

FIGURE 4-1: *SMBus Timing Diagram*



4.2.1 SMBUS START BIT

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic ‘1’ state to a logic ‘0’ state while the SMBus Clock line is in a logic ‘1’ state.

4.2.2 SMBUS ADDRESS AND RD / $\overline{WR}$ BIT

The SMBus Address Byte consists of the 7-bit slave address followed by the RD / $\overline{WR}$ indicator bit. If this RD / $\overline{WR}$ bit is a logic ‘0’, then the SMBus Host is writing data to the slave device. If this RD / $\overline{WR}$ bit is a logic ‘1’, then the SMBus Host is reading data from the slave device.

See Table 4-1 for available SMBus addresses.

4.2.3 SMBUS DATA BYTES

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

4.2.4 SMBUS ACK AND NACK BITS

The SMBus slave will acknowledge all data bytes that it receives. This is done by the slave device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted. This applies to both the Write Byte and Block Write protocols.

The Host will NACK (not acknowledge) the last data byte to be received from the slave by holding the SMBus data line high after the 8th data bit has been sent. For the Block Read protocol, the Host will ACK each data byte that it receives except the last data byte.

4.2.5 SMBUS STOP BIT

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic ‘0’ state to a logic ‘1’ state while the SMBus clock line is in a logic ‘1’ state. When the CAP1166 detects an SMBus Stop bit and it has been communicating with the SMBus protocol, it will reset its slave interface and prepare to receive further communications.

4.2.6 SMBUS TIMEOUT

The CAP1166 includes an SMBus timeout feature. Following a 30ms period of inactivity on the SMBus where the SMCLK pin is held low, the device will timeout and reset the SMBus interface.

The timeout function defaults to disabled. It can be enabled by setting the TIMEOUT bit in the Configuration register (see Section 6.6, "Configuration Registers").

4.2.7 SMBUS AND I^2C COMPATIBILITY

The major differences between SMBus and I^2C devices are highlighted here. For more information, refer to the SMBus 2.0 and I^2C specifications. For information on using the CAP1166 in an I^2C system, refer to AN 14.0 Dedicated Slave Devices in I^2C Systems.

1. CAP1166 supports I^2C fast mode at 400kHz. This covers the SMBus max time of 100kHz.
2. Minimum frequency for SMBus communications is 10kHz.
3. The SMBus slave protocol will reset if the clock is held at a logic '0' for longer than 30ms. This timeout functionality is disabled by default in the CAP1166 and can be enabled by writing to the TIMEOUT bit. I^2C does not have a timeout.
4. The SMBus slave protocol will reset if both the clock and data lines are held at a logic '1' for longer than 200µs (idle condition). This function is disabled by default in the CAP1166 and can be enabled by writing to the TIMEOUT bit. I^2C does not have an idle condition.
5. I^2C devices do not support the Alert Response Address functionality (which is optional for SMBus).
6. I^2C devices support block read and write differently. I^2C protocol allows for unlimited number of bytes to be sent in either direction. The SMBus protocol requires that an additional data byte indicating number of bytes to read / write is transmitted. The CAP1166 supports I^2C formatting only.

4.3 SMBus Protocols

The CAP1166 is SMBus 2.0 compatible and supports Write Byte, Read Byte, Send Byte, and Receive Byte as valid protocols as shown below.

All of the below protocols use the convention in Table 4-2.

TABLE 4-2: PROTOCOL FORMAT

Data Sent to Device	Data Sent to the HOst
Data sent	Data sent

4.3.1 SMBUS WRITE BYTE

The Write Byte is used to write one byte of data to a specific register as shown in Table 4-3.

TABLE 4-3: WRITE BYTE PROTOCOL

Start	Slave Address	WR	ACK	Register Address	ACK	Register Data	ACK	Stop
1 ->0	YYYY_YYY	0	0	XXh	0	XXh	0	0 -> 1

4.3.2 SMBUS READ BYTE

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4-4.

TABLE 4-4: READ BYTE PROTOCOL

Start	Slave Address	WR	ACK	Register Address	ACK	Start	Slave Address	RD	ACK	Register Data	NACK	Stop
1->0	YYYY_YYY	0	0	XXh	0	1 ->0	YYYY_YYY	1	0	XXh	1	0 -> 1

4.3.3 SMBUS SEND BYTE

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4-5.

APPLICATION NOTE: The Send Byte protocol is not functional in Deep Sleep (i.e., DSLEEP bit is set).

TABLE 4-5: SEND BYTE PROTOCOL

Start	Slave Address	WR	ACK	Register Address	ACK	Stop
1 -> 0	YYYY_YYY	0	0	XXh	0	0 -> 1

4.3.4 SMBUS RECEIVE BYTE

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g., set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4-6.

APPLICATION NOTE: The Receive Byte protocol is not functional in Deep Sleep (i.e., DSLEEP bit is set).

TABLE 4-6: RECEIVE BYTE PROTOCOL

Start	Slave Address	RD	ACK	Register Data	NACK	Stop
1 -> 0	YYYY_YYY	1	0	XXh	1	0 -> 1

4.4 I²C Protocols

The CAP1166 supports I²C Block Write and Block Read.

The protocols listed below use the convention in Table 4-2.

4.4.1 BLOCK WRITE

The Block Write is used to write multiple data bytes to a group of contiguous registers as shown in Table 4-7.

APPLICATION NOTE: When using the Block Write protocol, the internal address pointer will be automatically incremented after every data byte is received. It will wrap from FFh to 00h.

TABLE 4-7: BLOCK WRITE PROTOCOL

Start	Slave Address	WR	ACK	Register Address	ACK	Register Data	ACK
1 ->0	YYYY_YYY	0	0	XXh	0	XXh	0
Register Data	ACK	Register Data	ACK	. . .	Register Data	ACK	Stop
XXh	0	XXh	0	. . .	XXh	0	0 -> 1

4.4.2 BLOCK READ

The Block Read is used to read multiple data bytes from a group of contiguous registers as shown in Table 4-8.

APPLICATION NOTE: When using the Block Read protocol, the internal address pointer will be automatically incremented after every data byte is received. It will wrap from FFh to 00h.

TABLE 4-8: BLOCK READ PROTOCOL

Start	Slave Address	WR	ACK	Register Address	ACK	Start	Slave Address	RD	ACK	Register Data
1->0	YYYY_YYY	0	0	XXh	0	1 ->0	YYYY_YYY	1	0	XXh
ACK	Register Data	ACK	Register Data	ACK	Register Data	ACK	. . .	Register Data	NACK	Stop
0	XXh	0	XXh	0	XXh	0	. . .	XXh	1	0 -> 1

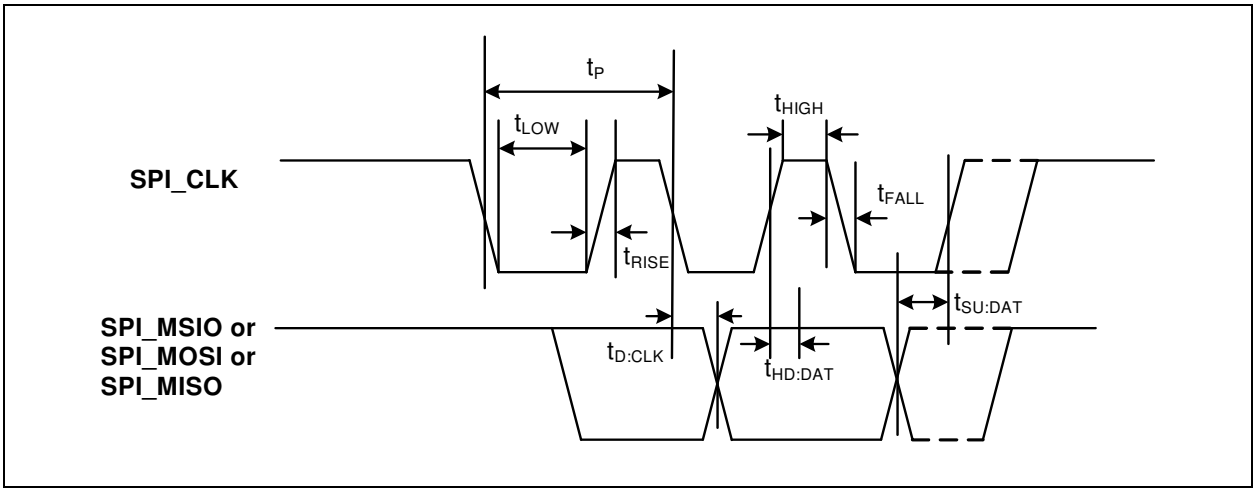
4.5 SPI Interface

The SMBus has a predefined packet structure, the SPI does not. The SPI Bus can operate in two modes of operation, normal 4-wire mode and bi-directional 3-wire mode. All SPI commands consist of 8-bit packets sent to a specific slave device (identified by the CS pin).

The SPI bus will latch data on the rising edge of the clock and the clock and data both idle high.

All commands are supported via both operating modes. The supported commands are: Reset Serial interface, set address pointer, write command and read command. Note that all other codes received during the command phase are ignored and have no effect on the operation of the device.

FIGURE 4-2: *SPI Timing*



4.5.1 SPI NORMAL MODE

The SPI Bus can operate in two modes of operation, normal and bi-directional mode. In the normal mode of operation, there are dedicated input and output data lines. The host communicates by sending a command along the CAP1166 SPI_MOSI data line and reading data on the SPI_MISO data line. Both communications occur simultaneously which allows for larger throughput of data transactions.

All basic transfers consist of two 8 bit transactions from the Master device while the slave device is simultaneously sending data at the current address pointer value.

Data writes consist of two or more 8-bit transactions. The host sends a specific write command followed by the data to write the address pointer. Data reads consist of one or more 8-bit transactions. The host sends the specific read data command and continues clocking for as many data bytes as it wishes to receive.

4.5.2 SPI BI-DIRECTIONAL MODE

In the bi-directional mode of operation, the SPI data signals are combined into the SPI_MSIO line, which is shared for data received by the device and transmitted by the device. The protocol uses a simple handshake and turn around sequence for data communications based on the number of clocks transmitted during each phase.

All basic transfers consist of two 8 bit transactions. The first is an 8 bit command phase driven by the Master device. The second is by an 8 bit data phase driven by the Master for writes, and by the CAP1166 for read operations.

The auto increment feature of the address pointer allows for successive reads or writes. The address pointer will return to 00h after reaching FFh.

4.5.3 SPI_CS# PIN

The SPI Bus is a single master, multiple slave serial bus. Each slave has a dedicated CS pin (chip select) that the master asserts low to identify that the slave is being addressed. There are no formal addressing options.

4.5.4 ADDRESS POINTER

All data writes and reads are accessed from the current address pointer. In both Bi-directional mode and Full Duplex mode, the Address pointer is automatically incremented following every read command or every write command.

The address pointer will return to 00h after reaching FFh.

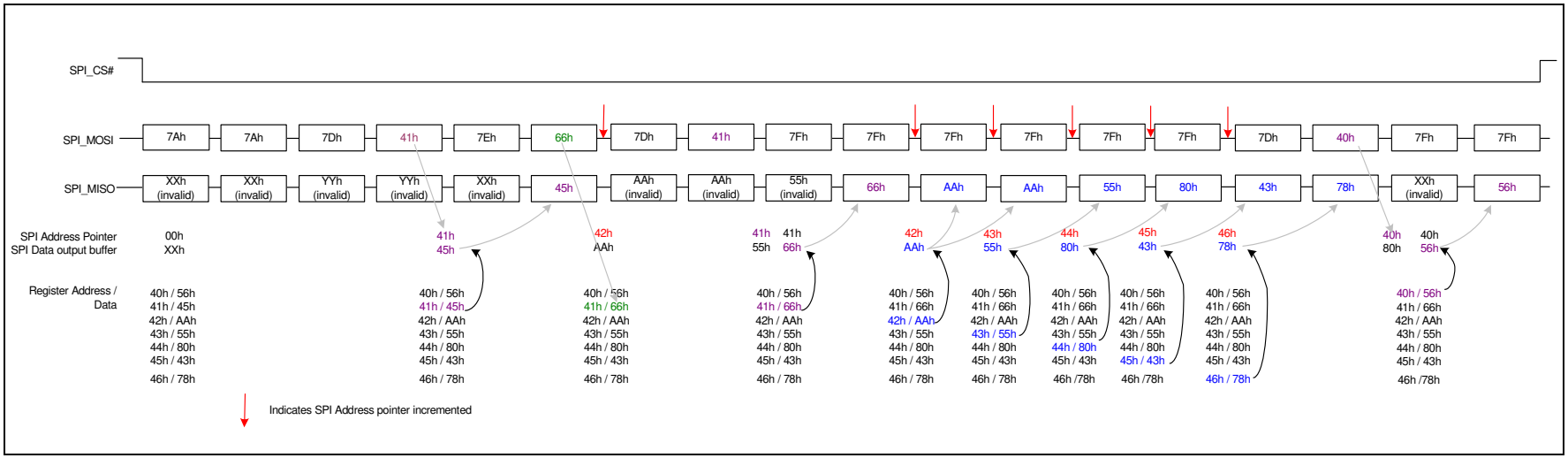
4.5.5 SPI TIMEOUT

The CAP1166 does not detect any timeout conditions on the SPI bus.

4.6 Normal SPI Protocols

When operating in normal mode, the SPI bus internal address pointer is incremented depending upon which command has been transmitted. Multiple commands may be transmitted sequentually so long as the SPI_CS# pin is asserted low. Figure 4-3 shows an example of this operation.

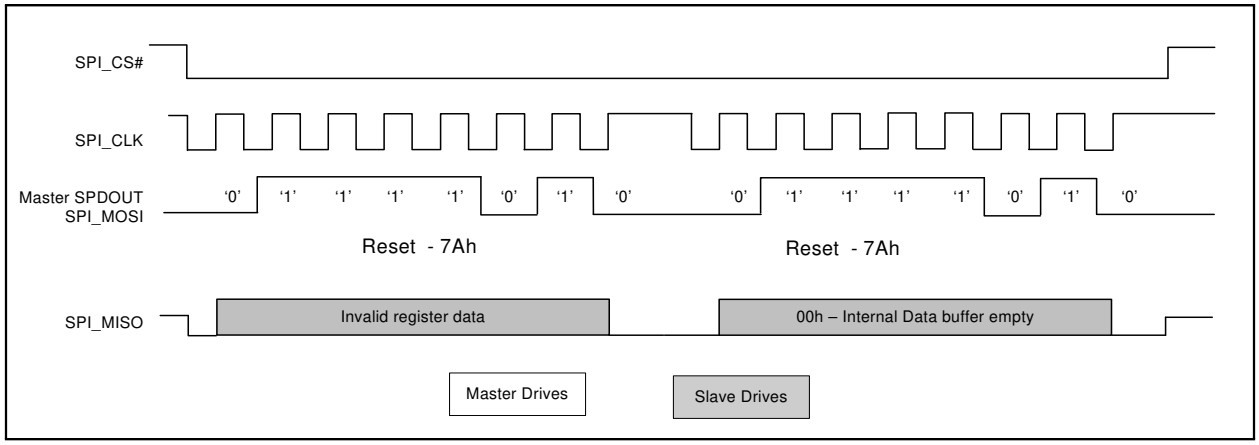
FIGURE 4-3: *Example SPI Bus Communication - Normal Mode*



4.6.1 RESET INTERFACE

Resets the Serial interface whenever two successive 7Ah codes are received. Regardless of the current phase of the transaction - command or data, the receipt of the successive reset commands resets the Serial communication interface only. All other functions are not affected by the reset operation.

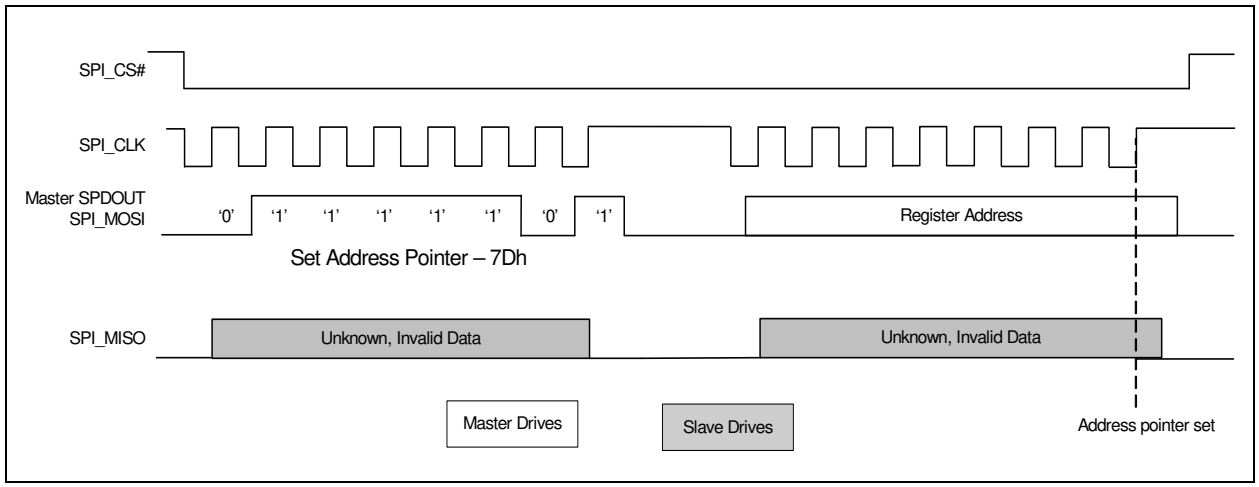
FIGURE 4-4: *SPI Reset Interface Command - Normal Mode*



4.6.2 SET ADDRESS POINTER

The Set Address Pointer command sets the Address pointer for subsequent reads and writes of data. The pointer is set on the rising edge of the final data bit. At the same time, the data that is to be read is fetched and loaded into the internal output buffer but is not transmitted.

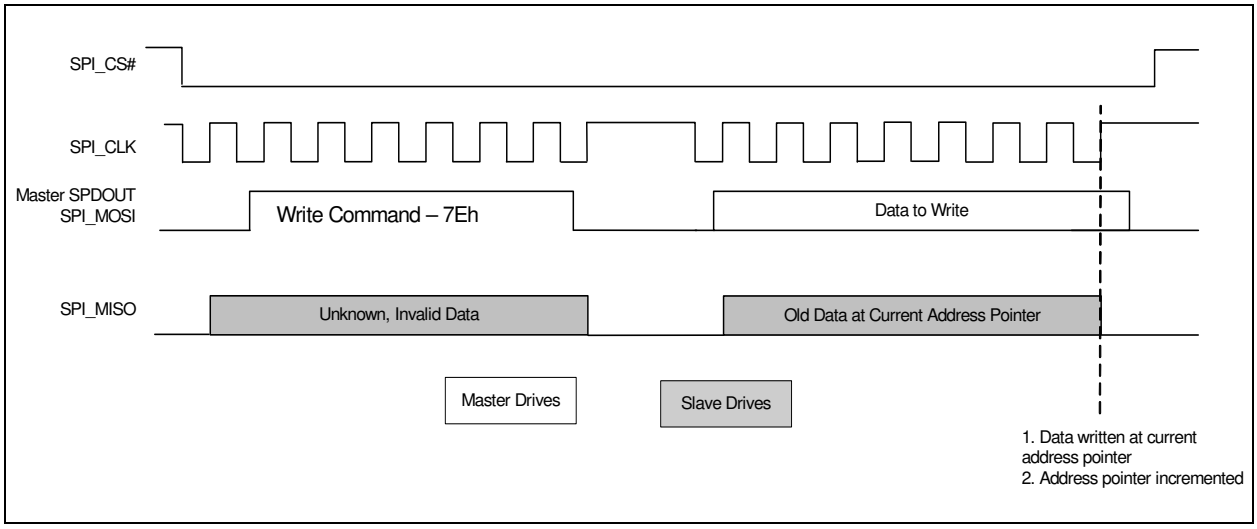
FIGURE 4-5: *SPI Set Address Pointer Command - Normal Mode*



4.6.3 WRITE DATA

The Write Data protocol updates the contents of the register referenced by the address pointer. As the command is processed, the data to be read is fetched and loaded into the internal output buffer but not transmitted. Then, the register is updated with the data to be written. Finally, the address pointer is incremented.

FIGURE 4-6: *SPI Write Command - Normal Mode*



4.6.4 READ DATA

The Read Data protocol is used to read data from the device. During the normal mode of operation, while the device is receiving data, the CAP1166 is simultaneously transmitting data to the host. For the Set Address commands and the Write Data commands, this data may be invalid and it is recommended that the Read Data command is used.

FIGURE 4-7: *SPI Read Command - Normal Mode*

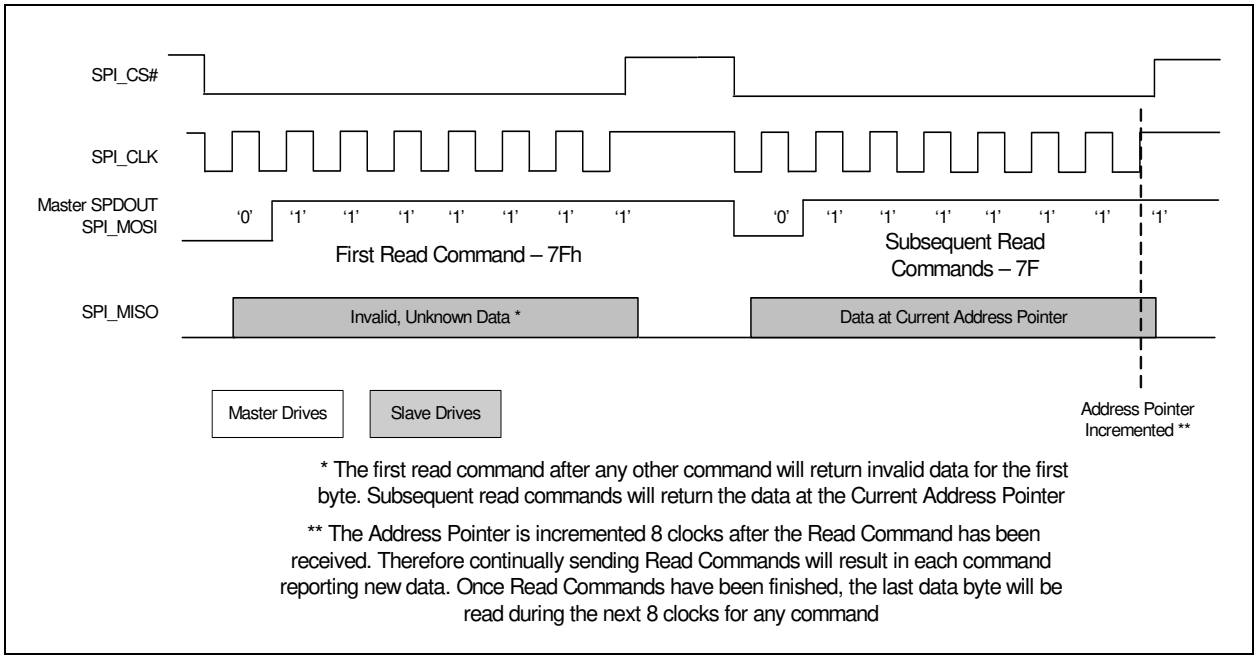
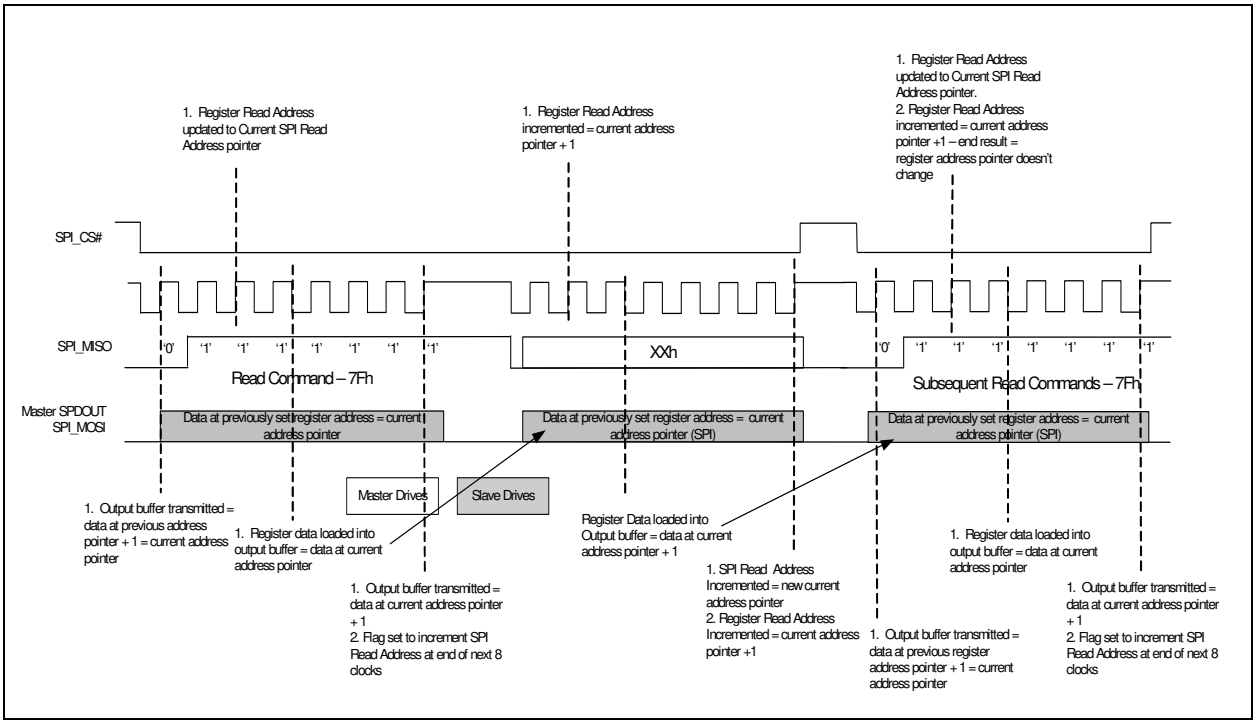


FIGURE 4-8: *SPI Read Command - Normal Mode - Full*

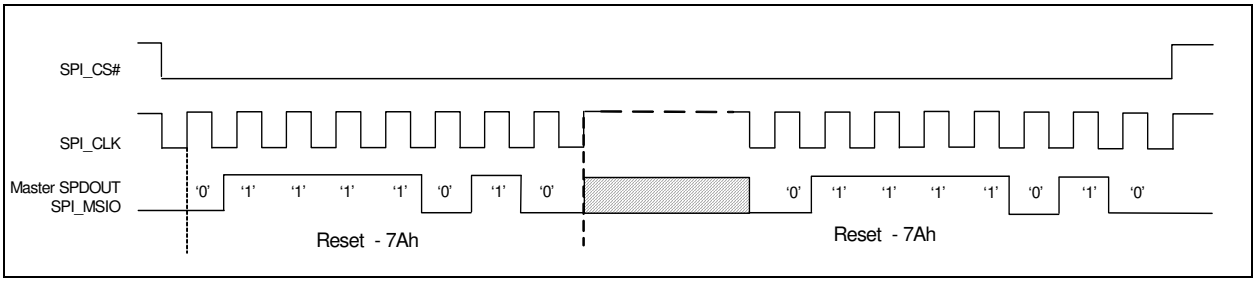


4.7 Bi-Directional SPI Protocols

4.7.1 RESET INTERFACE

Resets the Serial interface whenever two successive 7Ah codes are received. Regardless of the current phase of the transaction - command or data, the receipt of the successive reset commands resets the Serial communication interface only. All other functions are not affected by the reset operation.

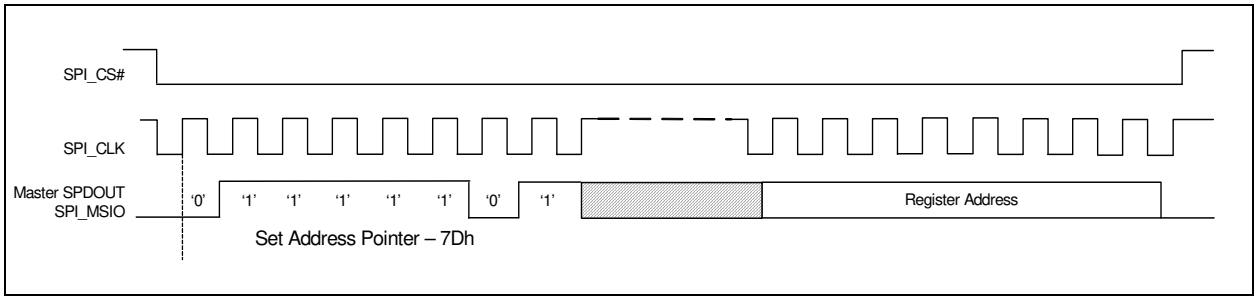
FIGURE 4-9: *SPI Reset Interface Command - Bi-directional Mode*



4.7.2 SET ADDRESS POINTER

Sets the address pointer to the register to be accessed by a read or write command. This command overrides the auto-incrementing of the address pointer.

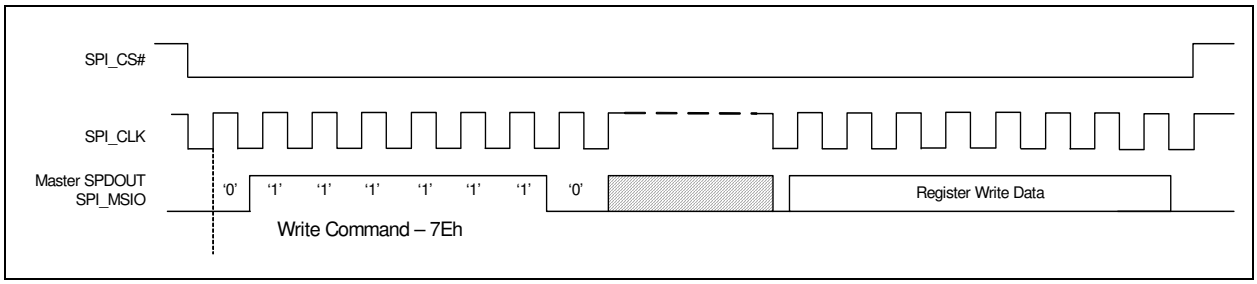
FIGURE 4-10: *SPI Set Address Pointer Command - Bi-directional Mode*



4.7.3 WRITE DATA

Writes data value to the register address stored in the address pointer. Performs auto increment of address pointer after the data is loaded into the register.

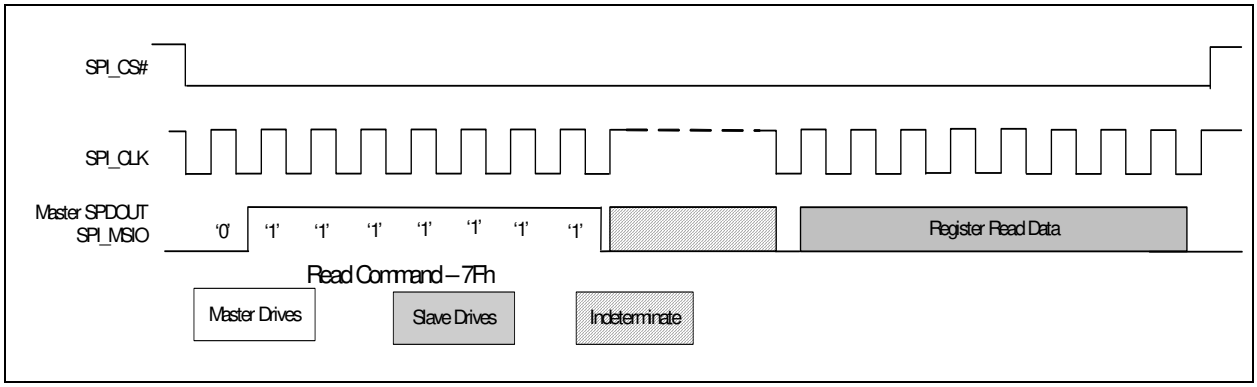
FIGURE 4-11: *SPI Write Data Command - Bi-directional Mode*



4.7.4 READ DATA

Reads data referenced by the address pointer. Performs auto increment of address pointer after the data is transferred to the Master.

FIGURE 4-12: *SPI Read Data Command - Bi-directional Mode*



4.8 BC-Link Interface

The BC-Link is a proprietary bus developed to allow communication between a host controller device to a companion device. This device uses this serial bus to read and write registers and for interrupt processing. The interface uses a data port concept, where the base interface has an address register, data register and a control register, defined in the 8051's SFR space.

Refer to documentation for the BC-Link compatible host controller for details on how to access the CAP1166 via the BC-Link Interface.

5.0 GENERAL DESCRIPTION

The CAP1166 is a multiple channel Capacitive Touch sensor with multiple power LED drivers. It contains six (6) individual capacitive touch sensor inputs with programmable sensitivity for use in touch sensor applications. Each sensor input automatically recalibrates to compensate for gradual environmental changes.

The CAP1166 also contains six (6) low side (or push-pull) LED drivers that offer full-on / off, variable rate blinking, dimness controls, and breathing. Each of the LED drivers may be linked to one of the sensor inputs to be actuated when a touch is detected. As well, each LED driver may be individually controlled via a host controller.

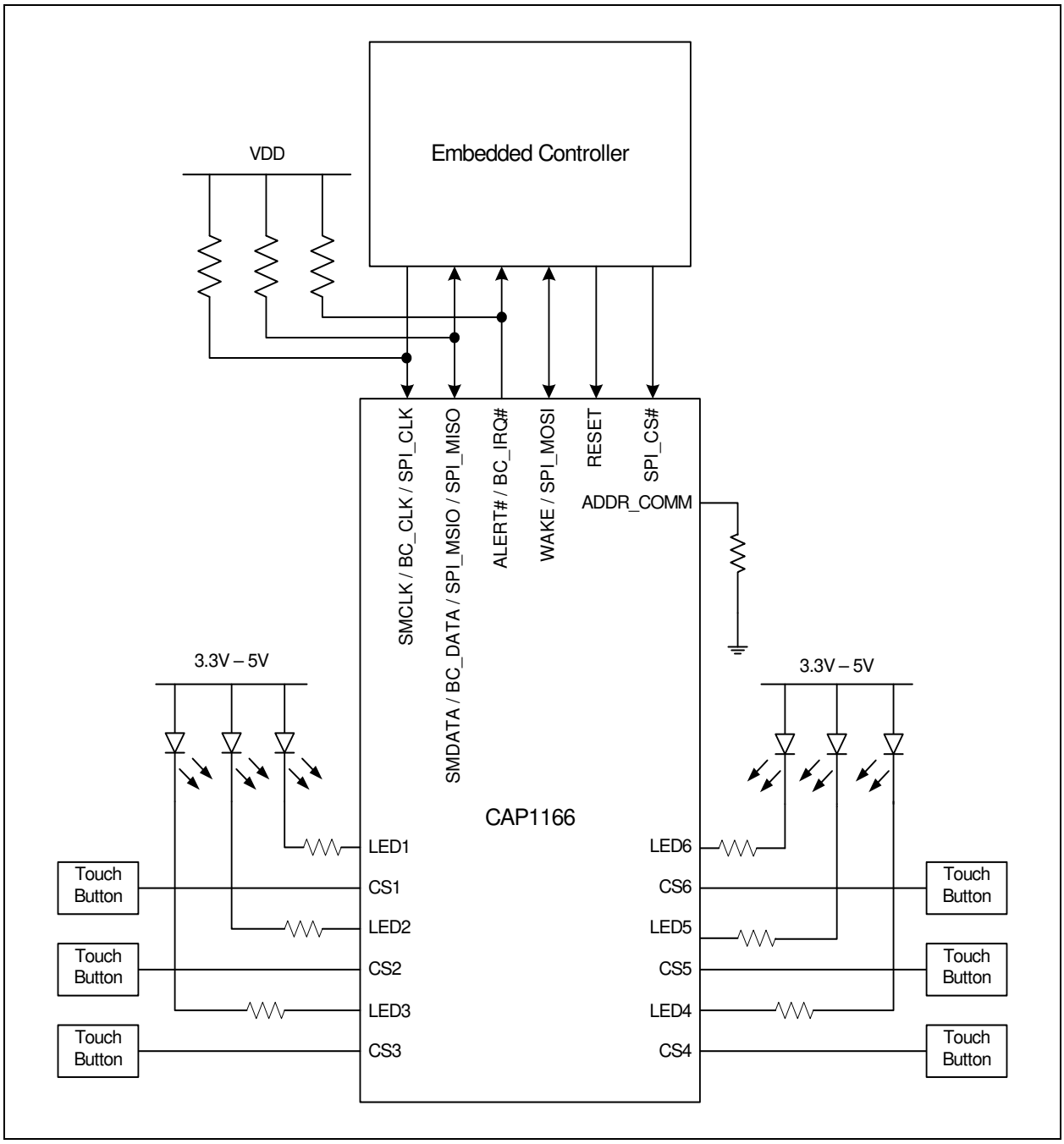
Finally, the device contains a dedicated RESET pin to act as a soft reset by the system.

The CAP1166 offers multiple power states. It operates at the lowest quiescent current during its Deep Sleep state. In the low power Standby state, it can monitor one or more channels and respond to communications normally. The device contains a wake pin (WAKE/SPI_MOSI) output to wake the system when a touch is detected in Standby and to wake the device from Deep Sleep.

The device communicates with a host controller using the SPI bus, or via SMBus / I^2C. The host controller may poll the device for updated information at any time or it may configure the device to flag an interrupt whenever a touch is detected on any sensor pad.

A typical system diagram is shown in Figure 5-1.

FIGURE 5-1: *System Diagram for CAP1166*



5.1 Power States

The CAP1166 has three operating states depending on the status of the STBY and DSLEEP bits. When the device transitions between power states, previously detected touches (for inactive channels) are cleared and the status bits reset.

1. Fully Active - The device is fully active. It is monitoring all active capacitive sensor inputs and driving all LED channels as defined.
2. Standby - The device is in a lower power state. It will measure a programmable number of channels using the Standby Configuration controls (see Section 6.20 through Section 6.22). Interrupts will still be generated based on the active channels. The device will still respond to communications normally and can be returned to the Fully