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# CAR3012TE series front-end

**Input: 90Vac to 264Vac; Output: 12Vdc @ 3000W; 3.3 or 5Vdc @ 4A Standby**

RoHS Compliant


## Applications

- 12Vdc distributed power architectures
- Routers/ VoIP/Soft and other Telecom Switches
- Mid to high-end Servers, ATE Equipment

## Features

- Efficiency: meets 80plus "Titanium" criteria
- Universal input with PFC
- Constant power characteristic
- 2 front panel LEDs: 1-input;2-[PG, fault, warning]
- ON/OFF control of the 12Vdc output
- Remote sense on the 12Vdc output
- No minimum load requirements
- Active load sharing (single wire)
- Hot Plug-ability
- Standby orderable either as 3.3Vdc or 5Vdc @ 4A
- Auto recoverable OC & OT protection
- Operating temperature: -10 - 60°C (de-rated above 50
- Digital status & control: dual/redundant PMBus™ seri bus
- EN/IEC/UL/CSA C22.2 60950-1 2nd edition +A1, CCC
- CE mark§
- Meets FCC part 15, EN55022 Class A standards
- Meets EN61000 immunity and transient standards
- Shock & vibration: Meets IPC 9592 Class II standards
- Front to back or reversed airflow w/air speed control

## Description

The CAR3012TE Front-End provides highly efficient isolated power from worldwide input mains in a compact 1U industry standard form factor. This power supply is ideal for applications where mid to light load efficiency is of key importance in order to reduce system power consumption during 'typical' operational conditions.

The high-density, front-to-back, or reversed, airflow is designed for minimal space utilization and is highly expandable for future growth. Dual/redundant, industry standard, PMBus™ compliant I²C communications busses offer a full range of control and monitoring capabilities with sequential control from two independent sources

* UL is a registered trademark of Underwriters Laboratories, Inc.
† CSA is a registered trademark of Canadian Standards Association.
‡ VDE is a trademark of Verband Deutscher Elektrotechniker e.V.
§ Intended for integration into end-user equipment. All the required procedures for CE marking of end-user equipment should be followed. (The CE mark is placed on selected products.)
** ISO is a registered trademark of the International Organization of Standards.
\+ PMBus name and logo are registered trademarks of the System Management Interface Forum (SMIF)

imagination at work

## Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation is not implied in excess of the operations section. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

| Parameter | Symbol | Min | | |
|---|---|---|---|---|
| Input Voltage: Continuous | $V_{IN}$ | 0 | 264 | $V_{AC}$ |
| Operating Ambient Temperature | $T_A$ | -10 | 70[1] | °C |
| Storage Temperature | Tstg | -40 | 85 | °C |
| I/O Isolation voltage to Frame (100% factory Hi-Pot tested) | | | 2121 | $V_{DC}$ |

## Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, load, and temperature conditions.

**INPUT**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operational Range | $V_{IN}$ | 85 | 115/230 | 264 | $V_{AC}$ |
| Frequency Range (ETSI 300-132-1 recommendation) | $F_{IN}$ | 47 | 50/60 | 63 | Hz |
| Main Output Turn OFF | $V_{IN}$ | 70 | | 80 | $V_{AC}$ |
| Main Outptut Turn ON | | 75 | | 85 | |
| Hysteresis between turn OFF and turn ON | | 5 | | | |
| Maximum Input Current ($V_O$= $V_{O, set}$, $I_O$=$I_{O, max}$) $V_{IN}$= 100$V_{AC}$<br>$V_{IN}$= 208$V_{AC}$ | $I_{IN}$ | | | 16.3<br>15.9 | $A_{AC}$ |
| Cold Start Inrush Current (Excluding x-caps, 25°C, <10ms, per ETSI 300-132) | $I_{IN}$ | | | 40 | $A_{PEAK}$ |
| Efficiency[2] ($T_{amb}$=25°C, $V_O$= 12V) $V_{IN}$<br>100% load<br>50% load<br>20% load<br>10% load | η | **115V/230V/230V$_{80+}$**<br>92/93/91<br>92.5/94/96<br>87/93/94<br>75/88/90 | | | % |
| Power Factor ($V_{IN}$=115/230$V_{AC}$), $I_O$= 50% $I_{O, max}$<br>$I_O$= $I_{O, max}$ | PF | | 0.98<br>0.99 | | |
| Holdup time (Vout≥ 10.8$V_{DC}$, Tamb 25°C, $I_O$=$I_{O, max}$) $V_{in}$= 230$V_{AC}$<br>$V_{IN}$= 100$V_{AC}$ | T | 10 | 12<br>20 | | ms |
| Early warning prior to output falling below regulation[3] | | 2 | | | |
| Ride through | T | | 10 | | |
| Leakage Current ($V_{IN}$= 250$V_{AC}$, $F_{IN}$ = 60Hz) | $I_{IN}$ | | | 3 | $mA_{RMS}$ |
| Isolation Input/Output | | 3000 | | | $V_{AC}$ |
| Input/Frame | | 2121 | | | $V_{DC}$ |
| Output/Frame | | 100 | | | $V_{DC}$ |

**12V$_{dc}$ MAIN OUTPUT**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Power 180 – 264 / 90-132 Vac | W | 0 | - | 3000/1400 | W |
| $V_{AC}$≤ 90$V_{AC}$ | | 0 | - | 1200 | W |
| Factory Set default set point | $V_O$ | 11.9 | 12.00 | 12.1 | $V_{DC}$ |
| Overall regulation (load, temperature) | | -2 | | +2 | % |

[1] Power derated above 50°C, see environmental section

[2] 80+ Titanium standard test method: 25°C, Standby @ NL, fan powered externally. Standard test method: 25°C, Standby @ FL, fan powered internally

[3] Measured by the PG# signal going LO prior to the output decaying below 10.8Vdc

**$12V_{dc}$ MAIN OUTPUT (continued)**

| Parameter[4] | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Ripple and noise | | | | 120 | $mV_{P-P}$ |
| Turn-ON overshoot | | | | +5 | % |
| Turn-ON delay | T | | | 3 | sec |
| ON/OFF delay time | | | 100 | | ms |
| Turn-ON rise time (10 – 90% of $V_{out}$) | | | | 50 | ms |
| External capacitance capability | | | | 10,000 | µF |
| Transient response 50% step [10%-60%, 50% - 100%] (dI/dt – 1A/µs, recovery 300µs) | $V_O$ | -5 | | +5 | $\%V_O$ |
| Programmable range (hardware & software) | | 10.8 | | 13.2 | $V_{DC}$ |
| Overvoltage protection, latched $V_O \leq 12.6V$<br>(recover cycling 12V output OFF/ON) $V_O > 12.6V$ | | 13.3<br>13.8 | 13.9<br>14.8 | 14.5<br>15.8 | $V_{DC}$ |
| Output current $180 \geq V_{IN} \geq 264$<br>$90 \geq V_{IN} \geq 132$ | $I_O$ | 0 | | 250<br>117 | $A_{DC}$ |
| Current limit, Hiccup (programmable level) | | 105 | | 130 | % of FL |
| Active current share | | -5 | | +5 | % of FL |

**STANDBY OUTPUT**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Set point | $V_O$ | | 3.3 / 5.0 | | $V_{DC}$ |
| Overall regulation (load, temperature, aging) | $V_O$ | -5 | | +5 | % |
| Ripple and noise | | | | 50 | $mV_{P-P}$ |
| Output current | $I_O$ | 0 | | 4 | $A_{DC}$ |
| Overload protection - | | 110 | | 150 | % of FL |
| Isolation Output/Frame | | 100 | | | $V_{DC}$ |

## General Specifications

| Parameter | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|
| Reliability, 25°C<br>50°C | | 320,000<br>100,000 | | Hrs | Full load, ; MTBF per SR232 Reliability protection for electronic equipment, method I, case III, |
| Service Life | | 10 | | Yrs | Full load, excluding fans |
| Weight | | | | | |

## Feature Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions. See Control and Status for additional information. $V_{DD} = 3.3V_{DC}$

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ON/OFF (An internal pull-up resistor is provided) | | | | | |
| Logic High (Module ON) | $I_{IH}$ | | — | 20 | µA |
| | $V_{IH}$ | $0.7V_{DD}$ | — | 12 | $V_{DC}$ |
| Logic Low (Module OFF) | $I_{IL}$ | — | — | 4 | mA |
| | $V_{IL}$ | 0 | — | 0.8 | $V_{DC}$ |

[4] Ripple and transient response measured across 5 x 22µf and 1 x 0.1µf ceramic capacitors in parallel. 20MHz bandwidth.

## Feature Specifications (continued)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Output Voltage programming** (Vprog) | | | | | |
| Equation: Vout = 10.8 + (Vprog * 0.96) | | | | | |
| Vprog range | $V_{prog}$ | 0 | — | 2.5 | $V_{DC}$ |
| Programmed output voltage range | Vo | 10.8 | — | 13.2 | $V_{DC}$ |
| Voltage adjustment resolution | Vo | — | 10 | — | $mV_{DC}$ |
| Output configured to 13.2Vdc | $V_{prog}$ | 2.5 | | 3.0 | $V_{DC}$ |
| Output configured to the 12Vdc set-point | $V_{prog}$ | 3.0 | — | — | $V_{DC}$ |
| **Interlock** [short pin controlling presence of the 12$V_{DC}$ output] (pulled up internally to $V_{DD}$ by a 10kΩ resistor) | | | | | |
| 12V output OFF | $V_I$ | 2.42 | — | 3.46 | $V_{DC}$ |
| 12V output ON | $V_I$ | 0 | — | 0.4 | $V_{DC}$ |
| **PG#** (pulled up internally to $V_{DD}$ by a 10kΩ resistor) | | | | | |
| Logic High (Output voltage is present; $V_{OUT} \geq$ 10.7Vdc) | $I_{OH}$ | | — | 20 | μA |
| | $V_{OH}$ | 2.42 | — | 3.46 | $V_{DC}$ |
| Logic Low (Output voltage is not present; $V_{OUT} \leq$ 10.2$V_{DC}$) | $I_{OL}$ | — | — | 4 | mA |
| | $V_{OL}$ | 0 | — | 0.4 | $V_{DC}$ |
| **OTW#** (pulled up internally to $V_{DD}$ by a 10kΩ resistor) | | | | | |
| Logic High (temperature within normal range) | $I_{OH}$ | | — | 20 | μA |
| | $V_{OH}$ | 2.42 | — | 3.46 | $V_{DC}$ |
| Logic Low (temperature is too high) | $I_{OL}$ | — | — | 4 | mA |
| | $V_{OL}$ | 0 | — | 0.4 | $V_{DC}$ |
| Delayed shutdown after Logic Low transition | Tdelay | 10 | | | sec |
| **Fault#** (pulled up internally to $V_{DD}$ by a 10kΩ resistor) | | | | | |
| Logic High (No fault is present) | $I_{OH}$ | | — | 20 | μA |
| | $V_{OH}$ | 2.42 | — | 3.46 | $V_{DC}$ |
| Logic Low (Fault is present) | $I_{OL}$ | — | — | 4 | mA |
| | $V_{OL}$ | 0 | — | 0.4 | $V_{DC}$ |
| **PS Present** [internally connected to Logic_GRD] | | | | | |
| (Needs to be pulled HI via an external resistor) | | | | | |
| Logic High (Power supply is not plugged in) | | | | | |
| Logic Low (Power supply is present) | $V_{IL}$ | 0 | — | 0.1 | $V_{DC}$ |
| **8V_INT** (no components should be connected to this pin) | | | | | |
| **SCL, SDA** (internally pulled up to 3.3V by a 51kΩ resistor) | | | | | |
| Logic High | $V_{IH}$ | 0.7$V_{DD}$ | | $V_{DD}$ | $V_{DC}$ |
| Logic Low | $V_{OL}$ | 0 | | 0.4 | |
| Bias supply voltage | $V_{DD}$ | | 3.3 | | |
| **SMBAlert#** (no internal pull up provided, ref: Logic_GRD) | | | | | |
| Voltage tolerance on signal pin | $V_{IN}$ I | | | 5 | $V_{DC}$ |
| Sink current capability | $V_{OL}$ | | | 5 | $mA_{DC}$ |
| Logic Low | | | | 0.4 | $V_{DC}$ |

## Digital Interface Specifications

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **PMBus Signal Interface Characteristics**[5] | | | | | | |
| Input Logic High Voltage (CLK, DATA) | | $V_{IH}$ | $0.7V_{DD}$ | | 3.6 | V |
| Input Logic Low Voltage (CLK, DATA) | | $V_{IL}$ | 0 | | 0.8 | V |
| Input high sourced current (CLK, DATA) | | $I_{IH}$ | 0 | | 10 | μA |
| Output Low sink Voltage (CLK, DATA, ALERT#) | $I_O$=5mA | $V_{OL}$ | | | 0.4 | V |
| Output Low sink current (CLK, DATA, ALERT#) | | $I_{OL}$ | | | 5 | mA |
| Output High open drain leakage current (CLK,DATA, ALERT#) | $V_O$=3.6V | $I_{OH}$ | 0 | | 10 | μA |
| PMBus Operating frequency range | Slave Mode | $F_{PMB}$ | 10 | | 400 | kHz |
| **Measurement System Characteristics** | | | | | | |
| Clock stretching | | $t_{STRETCH}$ | | | 25 | ms |
| $I_{OUT}$ measurement range | Linear | $I_{RNG}$ | 0 | | 242 | A |
| $I_{OUT}$ measurement accuracy 25°C | | $I_{OUT}$ | -2.5 | | +2.5 | % of FL |
| $V_{OUT}$ measurement range | Linear | $V_{OUT(rng)}$ | 0 | | 14 | V |
| $V_{OUT}$ measurement accuracy | | $V_{OUT(acc)}$ | -1 | | +1 | % |
| Temp measurement range | Linear | $Temp_{(rng)}$ | 0 | | 125 | °C |
| Temp measurement accuracy[6] | | $Temp_{(acc)}$ | -3 | | +3 | °C |
| $I_{IN}$ measurement range | Linear | $I_{IN(rng)}$ | 0 | | 18 | $A_{AC}$ |
| $I_{IN}$ measurement accuracy - standard measurement @ 25°C | | $I_{in(acc)}$ | -4 | | +4 | % of FL |
| $V_{IN}$ measurement range | Linear | $V_{IN(rng)}$ | 0 | | 320 | $V_{AC}$ |
| $V_{IN}$ measurement accuracy | | $V_{IN(acc)}$ | -2 | | +2 | % |
| $P_{IN}$ measurement range | Linear | $P_{N(rng)}$ | 0 | | 3000 | W |
| $P_{IN}$ measurement accuracy – standard measurement @ 25°C | > 350W<br>< 350W | $P_{in(acc)}$ | -5<br>-50 | | +5<br>50 | %<br>W |
| Fan Speed measurement range | Linear | | 0 | | 30k | RPM |
| Fan Speed measurement accuracy | | | -10 | | 10 | % |
| Fan speed control range | Linear | | 0 | | 100 | % |

[5] Clock, Data, and Alert need to be pulled up to $V_{DD}$ externally.

[6] Temperature accuracy reduces non-linearly with decreasing temperature

## Environmental Specifications

| Parameter | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|
| Ambient Temperature<br>Normal airflow<br>Reverse airflow Vin > 180Vac<br>Reverse airflow Vin > 90Vac | -10[7] | | 50<br>35<br>47 | °C | |
| Storage Temperature | -40 | | 85 | °C | |
| Operating Altitude | | | 2250/7382 | m/ft | |
| Non-operating Altitude | | | 8200/26900 | m / ft | |
| Power Derating with Temperature<br>Normal airflow<br>Reverse airflow Vin > 180Vac<br>Reverse airflow Vin > 90Vac | | | 4<br>2.5<br>4 | %/°C | 50°C to 60°C<br>35°C to 50°C<br>47°C to 50°C |
| Power Derating with Altitude | | | 2.0 | °C/301 m<br>°C/1000 ft | Above 1524 m/5000 ft |
| Acoustic noise | | 55<br>45 | | dbA | Full load<br>Half load |
| Over Temperature Protection | | 78/70 | | °C | Shutdown / restart |
| Humidity<br>Operating<br>Storage | 5<br>5 | | 95<br>95 | % | Relative humidity, non-condensing |
| Shock and Vibration | Meet IPC 9592 Class II, Section 5 requirements | | | | |

## EMC Compliance

| Parameter | Function | Standard | Level | Criteria | Test |
|---|---|---|---|---|---|
| AC input | Conducted emissions | EN55022, FCC part 15<br>EN61000-3-2 | A | | 0.15 – 30MHz<br>0 – 2 KHz |
| | Radiated emissions** | EN55022 | A | | 30 – 10000MHz |
| AC input immunity | Voltage dips | EN61000-4-11 | | A | -30%, 10ms |
| | | | | B | -60%, 100ms |
| | | | | B | -100%, 5sec |
| | Voltage surge | EN61000-4-5 | | A | 4kV, 1.2/50µs, common mode |
| | | | | A | 2kV, 1.2/50µs, differential mode |
| | Fast transients | EN61000-4-4 | | A | 5/50ns, 2kV (common mode) |
| Enclosure immunity | Conducted RF fields | EN61000-4-6 | A | | 130dBµV, 0.15-80MHz, 80% AM |
| | Radiated RF fields | EN61000-4-3 | A | | 10V/m, 80-1000MHz, 80% AM |
| | | ENV 50140 | A | | |
| | ESD | EN61000-4-2 | B | | 4kV contact, 8kV air |

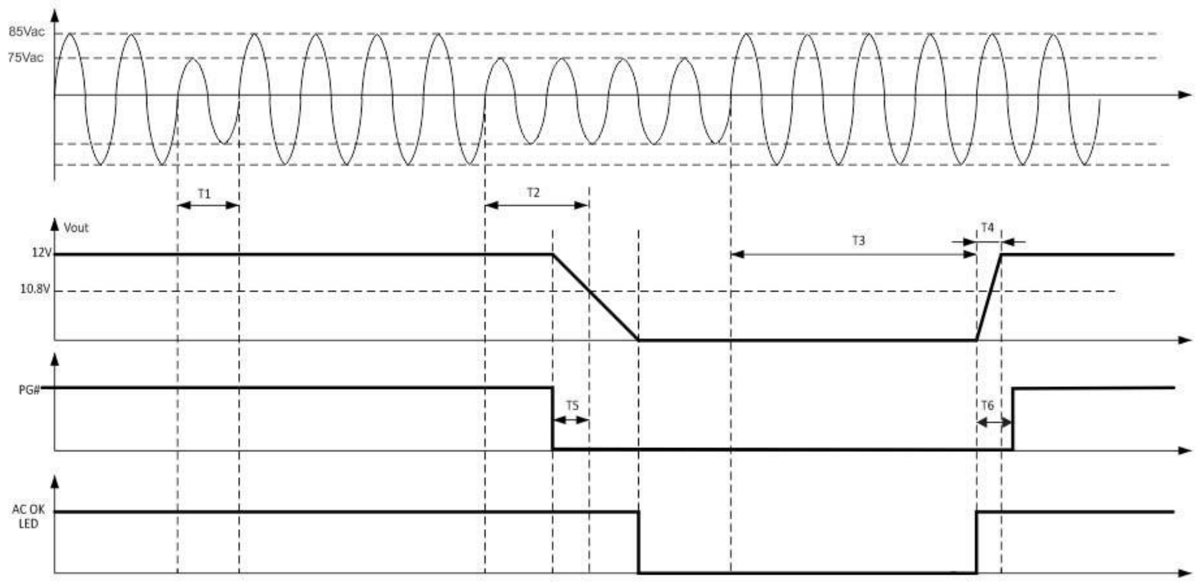
** Radiated emissions compliance is contingent upon the final system configuration.

| Criteria | Performance |
|---|---|
| A | No performance degradation |
| B | Temporary loss of function or degradation not requiring manual intervention |
| C | Temporary loss of function or degradation that may require manual intervention |
| D | Loss of function with possible permanent damage |

[7] Designed to start at an ambient down to -40°C; meet spec after ≅ 30 min warm up period, may not meet operational limits below -10°C.

## Timing Diagrams

### Response to input fluctuations




T1 - ride through time - typically 0.5 cycles [10 ms] Vout remains within regulation. Actual performance depends on output load

T2 - hold up time - 12ms @ 230Vac, 20ms @ 100Vac; Vout stays above 10.8Vdc under all loading conditions

T3 - delay time - > 2ms from the time AC returns within regulation to when the out starts rising

T4 - rise time - 50ms max. to within regulation

T5 - power good (PG#) - 2ms minimum warning indicated by the PG# signal going LO before Vout falls below 10.8Vdc

AC OK LED: Blinking when AC input falls below approx, 75Vac as long as bias power is available

T6 > T4 - The PG# signal de-asserts after the output is within regulation

## Control and Status

**Control hierarchy:** Some features, such as output voltage, can be controlled both through hardware and firmware. For example, the output voltage is controlled both by a signal pin (Vprog) and firmware (Vout_command; 0x21).

Using output voltage as an example, the Vprog signal pin voltage level sets the output voltage if its value is < $3V_{DC}$. (see the Vprog section). When the programming signal Vprog is either a no connect or > $3V_{DC}$, the output voltage is set at the default value of $54V_{DC}$.

The signal pin controls the feature it is configuring until a firmware command is executed. However, once the firmware command has been executed, the signal pin is ignored. In the above example, the rectifier will no longer 'listen' to the Vprog pin if the Vout_command has been executed.

In summary, signals such as Vprog are utilized for setting the initial default value and for varying the value until firmware based control takes over. Once firmware control is executed, hardware based control is relinquished so the processor can clearly decide who has control.

**Analog controls:** Details of analog controls are provided in this data sheet under Feature Specifications.

**Common ground:** All signals and outputs are referenced to Output return (power) including the Logic_GRD (signal).

## Control Signals

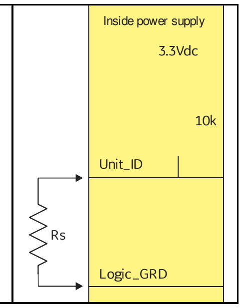
**Protocol:** This signal pin defines the communications mode setting of the power supply. Two different states can be configured. State #1 is the I²C application in which case the protocol pin should be left a no-connect. State #2 is the RS485 mode application in which case a resistor value between 1kΩ and 5kΩ should be present between this pin and Vout ( - ).

**Device address in I²C mode:** Address bits A3, A2, A1, A0 set the specific address of the µP in the power supply. With these four bits, up to sixteen (16) power supplies can be independently addressed on a single I²C bus. These four bits are configured by two signal pins, Unit_ID and Rack_ID. The least significant bit x (LSB) of the address byte is set to either **write [0]** or ***read [1]***. A ***write*** command instructs the power supply. A ***read*** command accesses information from the power supply.

| Device | Address | Address Bit Assignments (Most to Least Significant) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MCU | Cx or Dx | 1 | 1 | 0 | A3 | A2 | A1 | A0 | R/W |
| Broadcast | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | MSB | | | | | | | LSB |

**Unit_ID:** Up to 10 different units are selectable.

A voltage divider between 3.3V and Logic_GRD configures Unit_ID. Internally a 10kΩ resistor is pulled up to 3.3VDC. A pull down resistor Rs needs to be connected between pin Unit_ID and Logic_GRD.

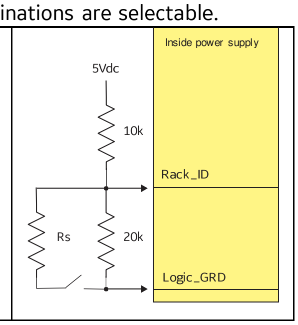



| Unit_ID | Voltage level | $R_S$ (± 0.1%) |
|---|---|---|
| Invalid | 3.30 | |
| 1 | 3.00 | 100k |
| 2 | 2.67 | 45.3k |
| 3 | 2.34 | 24.9k |
| 4 | 2.01 | 15.4k |
| 5 | 1.68 | 10.5k |
| 6 | 1.35 | 7.15k |
| 7 | 1.02 | 4.99k |
| 8 | 0.69 | 2.49k |
| 9 | 0.36 | 1.27k |
| 10 | 0 | 0 |

**Rack_ID:** Up to 8 different combinations are selectable.

A voltage divider between $5V_{DC}$ and Logic_GRD configures Rack_ID .

The 10k-20kΩ divider sets the initial voltage level to 3.3VDC. A switch between each RS value changes the Rack_ID level according to the table below.




| Rack_ID | Voltage level | $R_S$ (± 0.1%) |
|---|---|---|
| 1 | 3.3 | open |
| 2 | 2.8 | 35.2k |
| 3 | 2.3 | 15k |
| 4 | 1.8 | 8k |
| 5 | 1.4 | 4.99k |
| 6 | 1 | 2.87k |
| 7 | 0.5 | 1.27k |
| 8 | 0 | 0 |

**Configuration of the A3 – A0 bits:** The power supply will determine the configured address based on the Unit_ID and Rack_ID voltage levels as follows (the order is A3 – A0):

| | | Unit_ID | | | | |
|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 |
| Rack_ID | 1 | 0000 | 0001 | 0010 | 0011 | **0000** |
| | 2 | 0100 | 0101 | 0110 | 0111 | **0000** |
| | 3 | 1000 | 1001 | 1010 | 1011 | **0000** |
| | 4 | 1100 | 1101 | 1110 | 1111 | **0000** |
| | 5 | **0000** | **0000** | **0000** | **0000** | **0000** |
| | 6 | 0000 | 0001 | 0010 | 0011 | 0100 |
| | 7 | 0101 | 0110 | 0111 | 1000 | 1001 |
| | 8 | 1010 | 1011 | 1100 | 1101 | 1110 |

**Unit x Rack: 4 x 4 and 5 x 3**

| | | Unit_ID | | | | |
|---|---|---|---|---|---|---|
| | | 6 | 7 | 8 | 9 | 10 |
| Rack_ID | 1 | 0000 | 0001 | **0000** | **0000** | **0000** |
| | 2 | 0010 | 0011 | **0000** | **0000** | **0000** |
| | 3 | 0100 | 0101 | **0000** | **0000** | **0000** |
| | 4 | 0110 | 0111 | 0000 | 0001 | 0010 |
| | 5 | 1000 | 1001 | 0011 | 0100 | 0101 |
| | 6 | 1010 | 1011 | 0110 | 0111 | 1000 |
| | 7 | 1100 | 1101 | 1001 | 1010 | 1011 |
| | 8 | 1110 | 1111 | 1100 | 1101 | 1110 |

**Unit x Rack: 2 x 8 and 3 x 5**

**Device address in RS485 mode:** The power supply is configured for a static, single, address internally. This mode of operation is used only for factory testing.

**Global Broadcast:** This is a powerful command because it instruct all power supplies to respond simultaneously. A ***read*** instruction should never be accessed globally. The power supply should issue an 'invalid command' state if a 'read' is attempted globally.

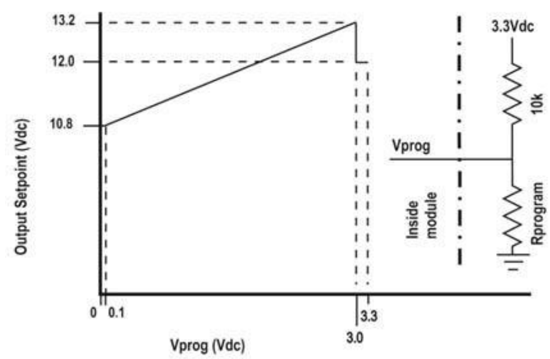
For example, changing the 'system' output voltage requires the global broadcast so that all paralleled power supplies change their output simultaneously. This command can also turn OFF the 'main' output or turn ON the 'main' output of all power supplies simultaneously. Unfortunately, this command does have a side effect. Only a single power supply needs to pull down the ninth *acknowledge* bit. To be certain that each power supply responded to the global instruction, a *READ* instruction should be executed to each power supply to verify that the command properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

**Voltage programming ($V_{prog}$):** Hardware voltage programming controls the output voltage until a software issued command to change the output voltage is executed. Software voltage programming permanently overrides the hardware $V_{prog}$ setting and the power supply no longer listens to the hardware setting until power to the controller is interrupted, for example if input power or bias power is recycled.

When bias power is recycled to the controller the controller restarts into its default configuration, programmed to set the output as instructed by the $V_{prog}$ pin. Again, subsequent software commanded settings permanently override the margin setting. As an example, adding a resistor between $V_{prog}$ and Logic_GRD is an effective way of changing the factory set point of the power supply to whatever voltage level is desired by the user during initial start-up.

The Vprog pin level should be set by a divider from 3.3Vdc to Logic_GRD external to the power supply as shown in the graph. Programming can be accomplished either by a resistor divider or by a voltage source injecting a precision voltage level into the Vprog pin. Above 3Vdc the power supply sets the output to its default state.

An analog voltage on this signal can vary the output voltage ± 10% from 10.8Vdc to 13.2Vdc.




**Load share ($I_{share}$):** This is a single wire analog signal that is generated and acted upon automatically by power supplies connected in parallel. $I_{share}$ pins should be connected to each other for power supplies, if active current share among the power supplies is desired. No resistors or capacitors should get connected to this pin.

**Remote ON/OFF:** Controls the presence of the main 12Vdc output voltage. This is an open collector signal that needs to be pulled HI externally through a resistor. A logic HI turns ON the main output.

A turn OFF command either through this signal (Remote ON/OFF) or firmware commanded would turn OFF the 12V output.

**Interlock:** This is a short signal pin that controls the presence of the 12Vdc main output. This pin should be connected to 'Logic_GRD' on the system side of the output connector. This short pin ensures that no arcing or contact damage occurs to the connector during the hot insertion/extraction process.

**8V_INT:** Provides the ability to back_bias a front-end that lost input power thus maintaining the ability to communicate with a remote controller. This pin should be interconnected among units in a system.

## Status signals

**PS Present:** This signal notifies the system controller that a power supply is physically present in the slot. This signal pin is pulled down to Output_return by the power supply.

**PG#:** A TTL compatible status signal representing whether the output voltage is present. This signal needs to be pulled HI externally through a resistor.

**Fault#:** This signal goes LO for any failure that requires power supply replacement. These faults may be due to:

- Fan failure
- Over-temperature shutdown
- Over-voltage shutdown
- Internal Power supply Fault

**Over Temperature Warning (OTW#):** A TTL compatible status signal representing whether an over temperature exists. This signal needs is pulled HI internally through a resistor.

If an over temperature should occur, this signal would pull LO for approximately 10 seconds prior to shutting down the power supply. In its default configuration, the unit would restart if internal temperatures recover within normal operational levels. At that time the signal reverts back to its open collector (HI) state.

## Serial Bus Communications

The I²C interface facilitates the monitoring and control of various operating parameters within the unit and transmits these on demand over an industry standard I²C Serial bus.

All signals are referenced to 'Logic_GRD'.

**Pull-up resistors:** The clock, data lines include a 51kΩ internal weak pull up. SMBusAlert# does not have an internal pull-up resistor inside the power supply. The user is responsible for ensuring that the transmission impedance of the communications lines complies with I²C and SMBus standards.

**Serial Clock (SCL):** The clock pulses on this line are generated by the host that initiates communications across the I²C Serial bus. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I²C /SMBus specifications.

**Serial Data (SDA):** This line is a bi-directional data line. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I²C /SMBus specifications.

**SMBUSAlert#:** This hardware signal pin is normally HI. When asserted (logic LO) it signifies to the system controller that the state of the power supply has changed or that communication errors occurred.

The SMBusAlert# line exciting the power supply combines the Alert# functions of power supply control and dual_bus_control.

## Digital Feature Descriptions

**PMBus™ compliance:** The power supply is fully compliant to the Power Management Bus (PMBus™) rev1.2 requirements. This Specification can be obtained from www.pmbus.org.

'Manufacturer Specific' commands are used to support additional instructions that are not in the PMBus™ specification.

All communication over the PMBus interface must support the Packet Error Checking (PEC) scheme. The PMBus master must generate the correct PEC byte for all transactions, and check the PEC byte returned by the power supply.

Non-volatile memory is used to store configuration settings. Not all settings programmed into the device are automatically saved into this non-volatile memory. Only those specifically identified as capable of being stored can be saved. (see the Table of Commands for which command parameters can be saved to non-volatile storage).

**Non-supported commands:** Non supported commands are flagged by setting the appropriate STATUS bit and issuing an Alert# to the 'host' controller.

If a non-supported read is requested the power supply will return 0x00h for data.

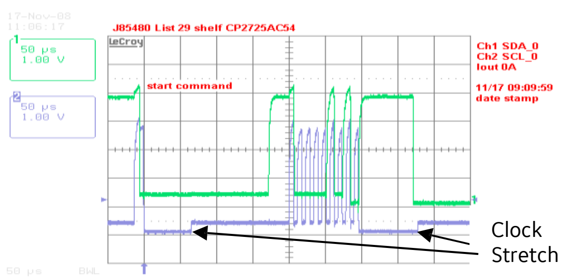
**Data out-of-range:** The power supply validates data settings and sets the data out-of-range bit and Alert# if the data is not within acceptable range.

**Master/Slave:** The 'host controller' is always the MASTER. Power supplies are always SLAVES. SLAVES cannot initiate communications or toggle the Clock. SLAVES also must respond expeditiously at the command of the MASTER as required by the clock pulses generated by the MASTER.

**Clock stretching:** The 'slave' µController inside the power supply may initiate clock stretching if it is busy and it desires to delay the initiation of any further communications. During the clock stretch the 'slave' may keep the clock LO until it is ready to receive further instructions from the host controller. The maximum clock stretch interval is 25ms.

The host controller needs to recognize this clock stretching, and refrain from issuing the next clock signal, until the clock line is released, or it needs to delay the next clock pulse beyond the clock stretch interval of the power supply.

Note that clock stretching can only be performed after completion of transmission of the 9th ACK bit, the exception being the START command.




**Example waveforms showing clock stretching.**

**I²C Bus Lock-Up detection:** The device will abort any transaction and drop off the bus if it detects the bus being held low for more than 35ms.

**Communications speed:** Both 100kHz and 400kHz clock rates are supported. The power supplies default to the 100kHz clock rate. The minimum clock speed specified by SMBus is 10 kHz.

**Packet Error Checking (PEC):** The power supply will not respond to commands without the trailing PEC because the integrity of communications is compromised without packet error correction deployment.

PEC is a CRC-8 error-checking byte, based on the polynomial $C(x) = x^8 + x^2 + x + 1$, in compliance with PMBus™ requirements. The calculation is performed on all message bytes, including the originating write address and command bytes preceding read instructions. The PEC is appended to the message by the device that supplied the last byte.

**Alert#:** The power supply can issue Alert# driven from either its internal micro controller (µC) or from the I²C bus master selector stage. That is, the Alert# signal of the internal µC funnels through the master selector stage that buffers the Alert# signal and splits the signal to the two Alert# signal pins exiting the power supply. In addition, the master selector stage signals its own Alert# request to either of the two Alert# signals when required.

The µC driven Alert# signal informs the 'master/host' controller that either a STATE or ALARM change has occurred. Normally this signal is HI. The signal will change to its LO level if the power supply has changed states and the signal will be latched LO until the power supply receives a 'clear_faults' instruction.

The signal will be triggered for any state change, including the following conditions;

- VIN under or over voltage
- Vout under or over voltage
- IOUT over current
- Over Temperature warning or fault
- Fan Failure
- Communication error
- PEC error
- Invalid command
- Internal faults
- Both Alert#_0 and -1 are asserted during power up to notify the master that a new power supply has been added to the bus.

The power supply will clear the Alert# signal (release the signal to its HI state) upon the following events:

- Receiving a CLEAR_FAULTS command
- Bias power to the processor is recycled

The power supply will re-assert the Alert line if the internal state of the power supply has changed, even if that information cannot be reported by the status registers until a clear_faults is issued by the host. If the Alert asserts, the host should respond by issuing a clear_faults to retire the alert line (this action also provides the ability to change the status registers). This action triggers another Alert assertion because the status registers changed states to report the latest state of the power supply. The host is now able to read the latest reported status register information and issue a clear_faults to retire the Alert signal.

**Re-initialization:** The I²C code is programmed to re-initialize if no activity is detected on the bus for 5 seconds. Re-initialization is designed to guarantee that the I²C µController does not hang up the bus. Although this rate is longer than the timing requirements specified in the SMBus specification, it had to be extended in order to ensure that a re-initialization would not occur under normal transmission rates. During the few µseconds required to accomplish re-initialization the I²C µController may not recognize a command sent to it. (i.e. a start condition).

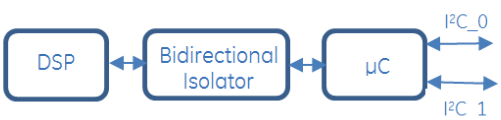
**Read back delay:** The power supply issues the Alert# notification as soon as the first state change occurred. During an event a number of different states can be transitioned to before the final event occurs. If a read back is implemented rapidly by the host a successive Alert# could be triggered by the transitioning state of the power supply. In order to avoid successive Alert# s and read back and also to avoid reading a transitioning state, it is prudent to wait more than 2 seconds after the receipt of an Alert# before executing a read back. This delay will ensure that only the final state of the power supply is captured.

**Successive read backs:** Successive read backs to the power supply should not be attempted at intervals faster than every one second. This time interval is sufficient for the internal processors to update their data base so that successive reads provide fresh data.

## Dual Master Control:

Two independent I²C lines provide true communications bus redundancy and allow two independent controllers to sequentially control the power supply. For example, a short or an open connection in one of the I²C lines does not affect communications capability on the other I²C line. Failure of a 'master' controller does not affect the power supplies and the second 'master' can take over control at any time.

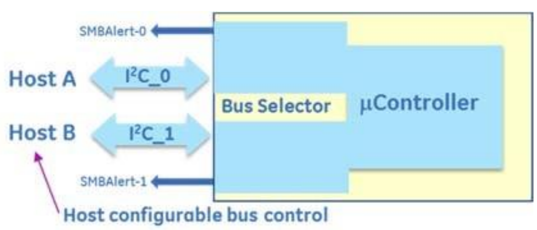
Conceptually a Digital Signal Processor (DSP) referenced to Vout(-) of the power supply provides secondary control. A Bidirectional Isolator provides the required isolation between power GRD, Vout(-) and signal GRD (Logic_GRD). A secondary micro controller provides instructions to and receives operational data from the DSP. The secondary micro controller also controls the communications over two independent I2C lines to two independent system controllers.




The secondary micro controller is designed to default to I²C_0 when powered up. If only a single system controller is utilized, it should be connected to I²C_0. In this case the I²C_1 line is totally transparent as if it does not exist.

If two independent system controllers are utilized, then one of them should be connected to I2C_0 and the other to I2C_1.

At power up the master connected to I2C_0 has control of the bus. See the section on Dual Master Control for further description of this feature.




**Conceptual representation of the dual I²C bus system.**

## PMBus$^{TM}$ Commands

**Standard instruction:** Up to two bytes of data may follow an instruction depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is optional and includes the address and data fields.

| 1 | 8 | | 1 | 8 | 1 |
|---|---|---|---|---|---|
| S | Slave address | Wr | A | Command Code | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| Low data byte | A | High data byte | A | PEC | A | P |

☐ Master to Slave ⬚ Slave to Master
SMBUS annotations; S – Start , Wr – Write, Sr – re-Start, Rd – Read,
A – Acknowledge, NA – not-acknowledged, P – Stop

**Standard READ:** Up to two bytes of data may follow a READ request depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

| 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|
| S | Slave address | Wr | A | Command Code | A |

| 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|
| Sr | Slave Address | Rd | A | LSB | A |

| 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|
| MSB | A | PEC | No-ack | P |

**Block communications:** When writing or reading more than two bytes of data at a time BLOCK instructions for WRITE and READ commands are used instead of the Standard Instructions above to write or read any number of bytes greater than two.

Block write format:

| 1 | 7 | 1 | 1 | | 8 | 1 |
|---|---|---|---|---|---|---|
| S | Slave address | Wr | A | | Command Code | A |

| 8 | 1 | 8 | 1 | 8 | | 1 |
|---|---|---|---|---|---|---|
| Byte count = N | A | Data 1 | A | Data 2 | | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| ……… | A | Data N ≤ 48 | A | PEC | A | P |

Block read format:

| 1 | 7 | 1 | 1 | | 8 | 1 |
|---|---|---|---|---|---|---|
| S | Slave address | Wr | A | | Command Code | A |

| 1 | 7 | 1 | 1 |
|---|---|---|---|
| Sr | Slave Address | Rd | A |

| 8 | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|
| Byte count = N | A | Data 1 | A | Data 2 | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| ……… | A | Data N ≤ 48 | A | PEC | NoAck | P |

**Linear Data Format:** The definition is identical to Part II of the PMBus Specification. All standard PMBus values, with the exception of output voltage related functions, are represented by the linear format described below. Output voltage functions are represented by a 16 bit mantissa. The value of the exponent for output voltage functions is listed in the Vout_mode command.

The Linear Data Format is a two byte value with an 11-bit, two's complement mantissa and a 5-bit, two's complement exponent or scaling factor, its format is shown below.

| | Data Byte High | | | | | | | | Data Byte Low | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | Exponent (E) | | | | | Mantissa (M) | | | | | | | | | | |

The relationship between the Mantissa, Exponent, and Actual Value (V) is given by the following equation:

$$V = M * 2^E$$

Where:

V is the value
M is the 11-bit, two's complement mantissa
*E* is the 5-bit, two's complement exponent

## Standard features

The commands below are 'read only'. They cannot be modified.

| Command | Comments |
|---|---|
| ON_OFF_CONFIG (0x02) | Both the CNTL pin, enabling or disabling the output, and the OPERATION command are supported. Other options are not supported. |
| Vout_OV_fault_response (0x41) | Only latched (0x80) is supported |
| CAPABILITY (0x19) | 400KHz, ALERT |
| PMBus revision (0x98) | 1.2 |

**Status and Alarm registers:** The registers are updated with the latest operational state of the power supply. For example, whether the output is ON or OFF is continuously updated with the latest state of the power supply. However, alarm information is maintained until a clear_faults command is received from the host. For example, the shutdown or OC_fault bits stay in their alarmed state until the host clears the registers.

A clear_faults clears all registers. If a fault still persists after the clear_faults is commanded, the register bit annunciating the fault is reset again

## PMBus™ Command set:

Non-supported commands are annunciated.

| Command | Hex Code | Data Field | Non-volatile memory storage[8] & default |
|---|---|---|---|
| Operation | 0x01 | 1 | yes |
| Clear_Faults | 0x03 | 0 | |
| Write _Protect | 0x10 | 1 | no |
| Restore_default_all | 0x12 | 0 | |
| Restore_default_code | 0x14 | 1 | |
| Store_user_code | 0x17 | 1 | yes |
| Restore_user_code | 0x18 | 1 | |
| Vout_mode | 0x20 | 1 | yes |
| Vout_command | 0x21 | 2 | yes |
| Vin_ON | 0x35 | 2 | no |
| Vin_OFF | 0x36 | 2 | no |
| Fan_config_1_2 | 0x3A | 1 | yes |
| Fan_command_1 | 0x3B | 2 | |
| Vout_OV_fault_limit | 0x40 | 2 | yes |
| Vout_OV_fault_response | 0x41 | 1 | yes |
| Vout_OV_warn_limit | 0x42 | 2 | yes |
| Vout_UV_warn_limit | 0x43 | 2 | yes |
| Vout_UV_fault_limit | 0x44 | 2 | yes |
| Vout_UV_fault_response[9] | 0x45 | 1 | yes |
| Iout_OC_fault_limit | 0x46 | 2 | yes |
| Iout_OC_fault_response[10] | 0x47 | 1 | yes |
| Iout_OC_LV_fault_limit | 0x48 | 2 | yes |
| Iout_OC_warn_limit | 0x4A | 2 | yes |
| OT_fault_limit | 0x4F | 2 | yes |
| OT_fault_response | 0x50 | 1 | Yes/C0 |
| OT_warn_limit | 0x51 | 2 | yes |
| Vin_OV_fault_limit | 0x55 | 2 | yes |
| Vin_OV_fault-response | 0x56 | 1 | yes |
| Vin_OV_warn_limit | 0x57 | 2 | yes |
| Vin_UV_warn_limit | 0x58 | 2 | yes |
| Vin_UV_fault_limit | 0x59 | 2 | yes |
| Vin_UV_fault_response | 0x5A | 1 | yes |
| | | | |
| Status_byte | 0x78 | 1 | |
| Status_word (+ byte) | 0x79 | 1 | |
| Status_Vout | 0x7A | 1 | |
| Status_Iout | 0x7B | 1 | |
| Status_Input | 0x7C | 1 | |
| Status_temperature | 0x7D | 1 | |
| Status_CML | 0x7E | 1 | |
| Status_fan_1_2 | 0x81 | 1 | |
| | | | |

[8] Yes – indicates that the data can be changed by the user
[9] Only latched (0x80) or restart (0xC0) are supported
[10] Only latched (0xC0) or hiccup (0xF8) are supported

| Command | Hex Code | Data Field | Non-volatile memory storage & default |
|---|---|---|---|
| Read_Vin | 0x88 | 2 | |
| Read_Iin | 0x89 | 2 | |
| Read_Vout | 0x8B | 2 | |
| Read_Iout | 0x8C | 2 | |
| Read_temp_PFC | 0x8D | 2 | |
| Read_temp_dc_primary | 0x8E | 2 | |
| Read_temp_dc_secondary | 0x8F | 2 | |
| Read_fan_speed_1 | 0x90 | 2 | |
| Read_fan_speed_2 | 0x91 | 2 | |
| Read_Pin | 0x97 | 2 | |
| Mfr_ID | 0x99 | 6 | Yes |
| Mfr_model | 0x9A | 16 | Yes |
| Mfr_revision | 0x9B | 8 | |
| Mfr_serial | 0x9E | 16 | yes |
| | | | |
| Status_summary | 0xD0 | 11 | |
| Status_unit | 0xD1 | 2 | |
| Status_alarm | 0xD2 | 3 | |
| Read_fan_speed | 0XD3 | 6 | |
| Read_input | 0xD4 | 5 | |
| Read_firmware_rev | 0xD5 | 6 | |
| Read_run_timer | 0xD6 | 3 | |
| Status_bus | 0xD7 | 1 | |
| Take over bus control | 0xD8 | | |
| EEPROM Record | 0xD9 | ≤64 | yes |
| Read_temp_exhaust | 0xDA | 2 | |
| Read_ temp_inlet | 0xDB | 2 | |
| Reserved for factory use | 0XDC | | |
| Reserved for factory use | 0XDD | | |
| Reserved for factory use | 0XDE | | |
| Test Function | 0xDF | 1 | |
| | | | |
| **Upgrade commands** | | | |
| Password | 0xE0 | 4 | |
| Target_list | 0xE1 | 4 | |
| Compatibility_code | 0xE2 | 32 | |
| Software_version | 0xE3 | 7 | |
| Memory_capability | 0xE4 | 7 | |
| Application_status | 0xE5 | 1 | |
| Boot_loader | 0xE6 | 1 | |
| Data_transfer | 0xE7 | ≤32 | |
| Product comcode | 0xE8 | 11 | |
| | | | |
| Upload_black_box | 0xF0 | ≤32 | |

## Command set adjustment range

If a command is received for a value setting that is outside the range defined below, the module should not change the present setting. The module could NACK the command and set the invalid/unsupported data bit of the status_cml (0x7E) register.

| Command | Hex Code | Default HL (LL) | Adjustment range Low | Adjustment range High |
|---|---|---|---|---|
| Vout_command | 0x21 | 12 | 10.8 | 13.2 |
| Fan_command_1 | 0x3B | - | 0 | 100 |
| Vout_OV_fault_limit | 0x40 | 14.8 | 10.8 | 13.2 |
| Vout_OV_warn_limit | 0x42 | 13.8 | 10.8 | 13.2 |
| Vout_UV_warn_limit | 0x43 | 10.8 | 10.8 | 13.2 |
| Vout_UV_fault_limit | 0x44 | 10 | 10 | 13.2 |
| Iout_OC_fault_limit | 0x46 | 270 | 0 | 270 |
| Iout_OC_LV_fault_limit | 0x48 | 7 | 7 | 13.2 |
| Iout_OC_warn_limit | 0x4A | 260 | 0 | 260 |
| OT_fault_limit | 0x4F | 130 | 0 | 150 |
| OT_warn_limit | 0x51 | 125 | 0 | 150 |
| Vin_OV_warn_limit | 0x57 | 265 | 85 | 265 |
| Vin_UV_warn_limit | 0x58 | 84 | 84 | 265 |

## Command Descriptions

**Operation (0x01):** By default the Power supply is turned **ON** at power up as long as *Power ON/OFF* signal pin is active HI. The Operation command is used to turn the Power Supply ON or OFF via the PMBus. The data byte below follows the OPERATION command.

| FUNCTION | DATA BYTE |
|---|---|
| Unit ON | 80 |
| Unit OFF | 00 |

To **RESET** the power supply cycle the power supply OFF, wait at least 2 seconds, and then turn back ON. All alarms and shutdowns are cleared during a restart.

**Clear_faults (0x03):** This command clears all STATUS and FAULT registers and resets the Alert# line of both the power supply and I$^2$C bus STATUS register.

If a fault, or a STATUS needing attention, still persists after the issuance of the clear_faults command, the specific registers indicating the fault are reset and the specific Alert# line is activated again.

**WRITE_PROTECT register (0x10):** Used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. All supported command parameters may have their parameters read, regardless of the write_protect settings. The contents of this register can be stored to non-volatile memory using the Store_default_code command. The default setting of this register is enable_all_writes 0x00h.

| FUNCTION | DATA BYTE |
|---|---|
| Enable all writes | 00 |
| Disable all writes except write_protect | 80 |
| Disable all writes except write_protect and OPERATION | 40 |

**Restore_Default_All (0x12):** Restores all register values and responses to the default parameters set in the power supply. The factory default cannot be changed.

**Restore_default_code (0x14):** Restore only a specific register parameter to the factory default parameters set in the power supply.

**Store_user_code (0x17):** Changes the user default setting of a single register. In this fashion some protection is offered to ensure that only those registers that are desired to be changed are in fact changed.

**Restore_user_code (0x18):** Restores the user default setting of a single register.

**Vout_mode (0x20):** This is a 'read only' register. The upper three bits specify the supported data format, in this case Linear mode. The lower five bits specify the exponent of the data in two's complement binary format for output voltage related commands, such as Vout_command. These commands have a 16 bit mantissa. The exponent is fixed by the module and is returned by this command.

| Mode | Bits [7:5] | Bits [4:0] (exponent) |
|---|---|---|
| Linear | 000b | xxxxxb |

**Vout_Command (0x21) :** Used to dynamically change the output voltage of the power supply. This command can also be used to change the factory programmed default set point of the power supply by executing a store-user instruction that changes the user default firmware set point.

The default set point can be overridden by the Vprog signal pin which is designed to override the firmware based default setting during turn ON.

In parallel operation, changing the output voltage should be performed simultaneously to all power supplies using the Global Address (Broadcast) feature. If only a single power supply is instructed to change its output, it may attempt to source all the required power which can cause either a power limit or shutdown condition.

Software programming of output voltage permanently overrides the set point voltage configured by the **Vprog** signal pin. The program no longer looks at the '**Vprog** pin' and will not respond to any hardware voltage settings. If power is removed from the µController it will reset itself into its default configuration looking at the **Vprog** signal for output voltage control. In many applications, the **Vprog** pin is used for setting initial conditions, if different that the factory setting. Software programming then takes over once $I^2C$ communications are established.

To properly hot-plug a power supply into a live backplane, the system generated voltage should get re-configured into either the factory adjusted firmware level or the voltage level reconfigured by the Vprog pin. Otherwise, the voltage state of the plugged in power supply could be significantly different than the powered system.

Voltage margin range: 10.8Vdc – 13.2 Vdc.

**Vin_ON (0x35):** This is a 'read only' register that informs the controller at what input voltage level the power supply turns ON. The default value is tabulated in the data section. The value is contingent on whether the power supply operates in the low_line or high_line mode.

**Vin_OFF (0x36):** This is a 'read only' register that informs the controller at what input voltage level the power supply turns OFF. The default value is tabulated in the data section. The value is contingent on whether the power supply operates in the low_line or high_line mode.

**Fan_config_1_2 (0x3A) :** This command allows the controller to define whether the fan speed command is in duty cycle or RPM. Both fans must be commanded simultaneously, either by duty cycle or RPM. Mixing controls will result in a 'data error'. The tachometer pulses per revolution is not used.

**Fan_command_1 (0x3B):** This command instructs the power supply to increase the speed of the fan. The transmitted data byte represents the hex equivalent of the duty cycle in percentage, i.e. 100% = 0x64. The command can only increase fan speed, it cannot instruct the power supply to reduce the fan speed below what the power supply requires for internal control.

Sending 00h tells the power supply to revert back to its internal control.

**Vout_OV_fault_limit (0x40):** Sets the value at which the main output voltage will shut down. The default OV_fault value is set at 60Vdc.

**Vout_OV_fault_response (0x41):** This is a 'read only' register. The only allowable state is a latched state after three retry attempts.

An overvoltage shutdown is followed by three attempted restarts, each successive restart delayed 1 second. If within a 1 minute window three attempted restarts failed, the unit will latch OFF. If less than 3 shutdowns occur within the 1 minute window then the count for latch OFF resets and the 1 minute window starts all over again. This performance cannot be changed.

**Restart after a latched state:** Either of four restart mechanisms is available;

- The hardware pin **ON/OFF** may be cycled OFF and then ON**.**
- The unit may be commanded to restart via i2c through the *Operation* command by first turning OFF then turning ON .
- The third way to restart is to remove and reinsert the unit.
- The fourth way is to turn OFF and then turn ON ac power to the unit.

A successful restart clears all STATUS and ALARM registers.

A power system that is comprised of a number of power supplies could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual power supplies. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

- Issuing a GLOBAL OFF and then a GLOBAL ON command to all power supplies

- Toggling Off and then ON the **ON/OFF** signal, if this signal is paralleled among the power supplies.
- Removing and reapplying input commercial power to the entire system.

The power supplies should be OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual power supplies.

**Vout_OV_warn_limit (0x42):** Sets the value at which a warning will be issued that the output voltage is too high.. Exceeding the warning value will set the Alert# signal.

**Vout_UV_warn_limit (0x43):** Sets the value at which a warning will be issued that the output voltage is too low. Reduction below the warning value will set the Alert# signal.

**Vout_UV_fault_limit (0x44):** Sets the value at which the power supply will shut down if the output gets below this level. This register is masked if the UV is caused by interruption of the input voltage to the power supply.

**Vout_UV_fault_response (0x45):** Sets the response if the output voltage falls below the UV_fault_limit. The default UV_fault_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0

**Iout_OC_fault_limit (0x46):** Sets the value at which the power supply will shut down. (The value is contingent on whether the power supply operates in the low_line or high_line mode).

**Iout_OC_fault_response (0x47):** Sets the response if the output overload exceeds the OC_Fault_limit value. The default OC_fault_response is hiccup (0xF8). The only two allowable states are latched (0xC0) or hiccup. The response is the same for both low_line and high_line operations.

**Iout_OC_warn_limit (0x4A):** Sets the value at which the power supply issues a warning that the output current is getting too close to the shutdown level. Which level is changed is contingent on the input voltage applied to the power supply at the time the change takes place.

**OT_fault_limit (0x4F):** Sets the value at which the power supply responds to an OT event, sensed by the dc-sec sensor. The response is defined by the OT_fault_response register.

**OT_fault_response (0x50):** Sets the response if the output overtemperature exceeds the OT_Fault_limit value. The default OT_fault_response is hiccup (0xC0). The only two allowable states are latched (0x80) or hiccup.

**OT_warn_limit (0x51):** Sets the value at which the power supply issues a warning when the dc-sec temperature sensor exceeds the warn limit.

**Vin_OV_fault_limit (0x55):** Sets the value at which the power supply shuts down because the input voltage exceeds the allowable operational limit.

**Vin_OV_fault_response (0x56):** Sets the response if the input voltage level exceeds the Vin_OV_fault_limit value. The default Vin_OV_fault_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0).

**Vin_UV_warn_limit (0x58):** This is another warning flag indicating that the input voltage is decreasing dangerously close to the low input voltage shutdown level.

**Vin_UV_fault_limit (0x59):** Sets the value at which the power supply shuts down because the input voltage falls below the allowable operational limit.

**Vin_UV_fault_response (0x5A):** Sets the response if the input voltage level falls below the Vin_UV_fault_limit value. The default Vin_UV_fault_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0).

**STATUS_BYTE (0x78) :** Returns one byte of information with a summary of the most critical device faults.

| Bit Position | Flag | Default Value |
|---|---|---|
| 7 | Unit is busy | 0 |
| 6 | OUTPUT OFF | 0 |
| 5 | VOUT Overvoltage Fault | 0 |
| 4 | IOUT Overcurrent Fault | 0 |
| 3 | VIN Undervoltage Fault | 0 |
| 2 | Temperature Fault or Warning | 0 |
| 1 | CML (Comm. Memory Fault) | 0 |
| 0 | None of the above | 0 |

**STATUS_WORD (0x79):** Returns status_byte as the low byte and the following high_byte.

| Bit Position | Flag | Default Value |
|---|---|---|
| 7 | VOUT Fault or Warning | 0 |
| 6 | IOUT Fault or Warning | 0 |
| 5 | INPUT Fault or Warning | 0 |
| 4 | MFR SPECIFIC | 0 |
| 3 | POWER_GOOD# (is negated) | 0 |
| 2 | FAN Fault or Warning | 0 |
| 1 | OTHER | 0 |
| 0 | UNKNOWN Fault or Warning | 0 |

**STATUS_VOUT (0X7A):** Returns one byte of information of output voltage related faults.

| Bit Position | Flag | Default Value |
|---|---|---|
| 7 | VOUT OV Fault | 0 |
| 6 | VOUT_OV_WARNING | 0 |
| 5 | VOUT_UV_WARNING | 0 |
| 4 | VOUT UV Fault | 0 |
| 3 - 0 | Not supported | 0 |

**STATUS_IOUT (0X7B):** Returns one byte of information of output current related faults.

| Bit Position | Flag | Default Value |
|---|---|---|
| 7 | IOUT OC Fault | 0 |
| 6 | IOUT OC LV Fault | 0 |
| 5 | IOUT OC Warning | 0 |
| 4 | X | 0 |
| 3 | CURRENT SHARE Fault | 0 |
| 2 | IN POWER LIMITING MODE | 0 |
| 1 - 0 | X | 0 |

**STATUS_INPUT (0X7C):** Returns one byte of information of input voltage related faults.

| Bit Position | Flag | Default Value |
|---|---|---|
| 7 | VIN_OV_Fault | 0 |
| 6 | VIN_OV_Warning | 0 |
| 5 | VIN_UV_ Warning | 0 |
| 4 | VIN_UV_Fault | 0 |
| 3 | Unit OFF for low input voltage | 0 |
| 2 | IIN_OC_Fault | 0 |
| 1 - 0 | Not supported | 0 |

**STATUS_TEMPERATURE (0x7D):** Returns one byte of information of temperature related faults.

| Bit Position | Flag | Default Value |
|---|---|---|
| 7 | OT Fault | 0 |
| 6 | OT Warning | 0 |
| 5 - 0 | Not supported | 0 |

**STATUS_CML (0x7E):** Returns one byte of information of communication related faults.

| Bit Position | Flag | Default Value |
|---|---|---|
| 7 | Invalid/Unsupported Command | 0 |
| 6 | Invalid/Unsupported Data | 0 |
| 5 | Packet Error Check Failed | 0 |
| 4 - 2 | Not supported | 0 |
| 1 | Other Communication Fault | 0 |
| 0 | Not supported | 0 |

**STATUS_FAN_1_2 (0x81) :** Returns one byte of information with a summary of the most critical device faults.

| Bit Position | Flag | Default Value |
|---|---|---|
| 7 | Fan 1 Fault | 0 |
| 6 | Fan 2 Fault | 0 |
| 5 - 4 | Not supported | 0 |
| 3 | Fan 1 speed overwritten | 0 |
| 2 | Fan 2 speed overwritten | 0 |
| 1 - 0 | Not supported | 0 |

## Read back Descriptions

**Single parameter read back:** Functions can be read back one at a time using the read_word_protocol with PEC.

Analog data is always transmitted LSB followed by MSB. A NA following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

| 1 | 8 | | 1 | 8 | 1 |
|---|---|---|---|---|---|
| S | Slave address | Wr | A | Command Code | A |

| 1 | 8 | | 1 |
|---|---|---|---|
| Sr | Slave address | Rd | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| LSB | A | MSB | A | PEC | NA | P |

**Read back error:** If the μC does not have sufficient time to retrieve the requested data, it has the option to return all FF's instead of incorrect data.

**Read_fan_speed 1 & 2 (0x90, 0x91):** Reading the fan speed is in Linear Mode returning the RPM value of the fan.

**Read_FRU_ID (0x99,0x9A, 0x9E):** Returns FRU information. Must be executed one register at a time.

| 1 | 8 | | 1 | 8 | 1 |
|---|---|---|---|---|---|
| S | Slave address | Wr | A | Command 0x9x | A |

| 1 | 8 | | 1 | 8 | 1 |
|---|---|---|---|---|---|
| Sr | Slave address | Rd | A | Byte count = x | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|
| Byte_1 | A | Byte | A | Byte_x | A | PEC | NA | P |

**Mfr_ID (0x99):** Manufacturer in ASCII – 6 characters maximum,
General Electric – Critical Power represented as: GE-CP

**Mfr_MODEL (0x9A):** Manufacturer model-number in ASCII – 16 characters, for this unit: CAR3012TEBXXZ01A

**Mfr_revision (0x9B):** Total 8 bytes, this is the product series taking the form X:YZ. Each byte is in ASCII format. The series number is read from left to right, scanned from the series number bar code on the power supply. Unused characters are filled at the end with null

**Mfr_serial (0x9E):** Product serial number includes the manufacturing date, manufacturing location in up to 15 characters. For example:
13KZ51018193xxx, is decoded as;
13 – year of manufacture, 2013
KZ – manufacturing location, in this case Matamoros
51 – week of manufacture
018193xxx – serial #, mfr choice

## Manufacturer-Specific PMBus™ Commands

Many of the manufacturer-specific commands read back more than two bytes. If more than two bytes of data are returned, the standard SMBus™ Block read is utilized. In this process, the Master issues a Write command followed by the data transfer from the power supply. The first byte of the Block Read data field sends back in hex format the number of data bytes, exclusive of the PEC number, that follows. Analog data is always transmitted LSB followed by MSB. A No-ack following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

**Mfr_Specific Status and alarm registers:** The content and partitioning of these registers is significantly different than the standard register set in the PMBus™ specification. More information is provided by these registers and they are either accessed rapidly, at once, using the 'multi parameter' read back scheme of this document, or in batches of two STATUS and two ALARM registers.

**Status_summary (0xD0) :** This 'manufacturer specific' command is the basic read back returning STATUS and ALARM register data, output voltage, output current, and internal temperature data in a single read. Internal temperature should return the temperature that is closest to a shutdown level.

| 1 | 8 | | 1 | 8 | 1 |
|---|---|---|---|---|---|
| S | Slave address | Wr | A | Command Code | A |

| 1 | 8 | | 1 | 8 | 1 |
|---|---|---|---|---|---|
| Sr | Slave address | Rd | A | Byte count = 11 | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|
| Status-2 | A | Status-1 | A | Alarm-3 | A | Alarm-2 | A |

| 8 | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|
| Alarm-1 | A | Voltage LSB | A | Voltage MSB | A |

| 8 | 1 | 8 | 1 |
|---|---|---|---|
| Current-LSB | A | Current-MSB | A |

| 8 | 1 | 8 | 1 |
|---|---|---|---|
| Temperature-LSB | A | Temperature-MSB | A |

| 8 | 1 | 1 |
|---|---|---|
| PEC | No-Ack | P |

**Status_unit(0xD1):** This command returns the STATUS-2 and STATUS-1 register values using the standard 'read' format.

**Status-2**

| Bit Position | Flag | Default Value |
|---|---|---|
| 7 | PEC Error | 0 |
| 6 | OC [hiccup=1,latch=0] | 1 |
| 5 | Invalid_Instruction | 0 |
| 4 | Power_Capacity [HL = 1] | x |
| 3 | OR'ing Test Failed | 0 |
| 2 | n/a | 0 |
| 1 | Data_out_of_range | 0 |
| 0 | Remote ON/OFF [HI = 1] | x |

**Oring fault:** Triggered either by the host driven or'ing test or by the repetitive testing of this feature within the power supply. A destructive fault would cause an internal shutdown. Success of the host driven test depends on whether the system is N+1 configured.. Thus a non-destructive or'ing fault does not trigger a shutdown.

**Status-1**

| Bit Position | Flag | Default Value |
|---|---|---|
| 7 | OT [Hiccup=1, latch=0] | 1 |
| 6 | OR'ing_Test_OK | 0 |
| 5 | Internal_Fault | 0 |
| 4 | Shutdown | 0 |
| 3 | Service LED ON | 0 |
| 2 | External_Fault | 0 |
| 1 | LEDs_Test_ON | 0 |
| 0 | Output ON (ON = 1) | x |

**Status_alarm (0xD2):** This command returns the ALARM-3 - ALARM-1 register values.

**Alarm-3**

| Bit Position | Flag | Default Value |
|---|---|---|
| 7 | Interlock open | 0 |
| 6 | Fuse fail | 0 |
| 5 | PFC-DC communications fault | 0 |
| 4 | DC-$I^2C$ communications fault | 0 |
| 3 | AC monitor communications fault | 0 |
| 2 | x | 0 |
| 1 | x | 0 |
| 0 | Or'ing fault | 0 |

**Alarm-2**

| Bit Position | Flag | Default Value |
|---|---|---|
| 7 | FAN_Fault | 0 |
| 6 | No_Primary | 0 |
| 5 | Primary_OT | 0 |
| 4 | DC/DC_OT | 0 |
| 3 | Vo lower than BUS | 0 |
| 2 | Thermal sensor filed | 0 |
| 1 | Stby_out_of_limits | 0 |
| 0 | Power_Delivery | 0 |

**Power Delivery:** If the internal sourced current to the current share current is > 10A, a fault is issued.

### Alarm-1

| Bit Position | Flag | Default Value |
|---|---|---|
| 7 | POWER LIMIT | 0 |
| 6 | PRIMARY Fault | 0 |
| 5 | OT_Shutdown | 0 |
| 4 | OT_Warning | 0 |
| 3 | IN OVERCURRENT | 0 |
| 2 | OV_Shutdown | 0 |
| 1 | VOUT_out_of_limits | 0 |
| 0 | VIN_out_of_limits | 0 |

**Over temperature warning:** This flag is set approximately 5°C prior to the commencement of an over temperature shutdown.

**Read_Fan_speed (0 x D3) :** Returns the commanded speed in percent and the measured speed in RPM. If a fan does not exist, or if the command is not supported the unit return 0x00.

| 1 | 8 | | 1 | 8 | 1 |
|---|---|---|---|---|---|
| S | Slave address | Wr | A | Command 0xE1 | A |

| 1 | 8 | | 1 | 8 | 1 |
|---|---|---|---|---|---|
| Sr | Slave address | Rd | A | Byte count = 6 | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|
| Adj%-LSB | A | Adj%-MSB | A | Fan1-LSB | A | Fan1-MSB | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| Fan2-LSB | A | Fan2-MSB | A | PEC | No-Ack | P |

**Read input string (0xD4):** Reads back the input voltage and input power consumed by the power supply.

| 1 | 7 | 1 | 1 | 8 |
|---|---|---|---|---|
| S | Slave address | Wr | A | Command Code 0xDC |

| 1 | 1 | 7 | 1 | 1 |
|---|---|---|---|---|
| A | Sr | Slave Address | Rd | A |

| 8 | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|
| Byte Count = 4 | A | Voltage - LSB | A | Voltage - MSB | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| Power - LSB | A | Power - MSB | A | PEC | No-ack | P |

**Read_firmware_rev [0 x D5]:** Reads back the firmware revision of all three µC in the power supply.

| 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|
| S | Slave address | Wr | A | Command Code 0xDD | A |

| 1 | 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|
| A | Sr | Slave Address | Rd | A | Byte Count = 6 | A |

| 8 | 1 | 8 | 1 |
|---|---|---|---|
| Primary major rev | A | Primary minor rev | A |

| 8 | 1 | 8 | 1 |
|---|---|---|---|
| Secondary major rev | A | Secondary minor rev | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| I²C major rev | A | I²C revision | A | PEC | No-ack | P |

**Read_run_timer [0xD6]:** This command reads back the recorded operational ON state of the power supply in hours. The operational ON state is accumulated from the time the power supply is initially programmed at the factory. The power supply is in the operational ON state both when in standby and when it delivers main output power.

Recorded capacity is approximately 10 years of operational state.

| 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|
| S | Slave address | Wr | A | Command Code 0xDE | A |

| 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|
| Sr | Slave Address | Rd | A | Byte count = 3 | A |

| 8 | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|
| Time - LSB | A | Time | A | Time - MSB | A |

| 8 | 1 | 1 |
|---|---|---|
| PEC | No-ack | P |

**Status_bus (0xD7):** Bus_Status is a single byte read back. The command can be executed by either master at any time independent of who has control.

The µC may issue a clock stretch, as it can for any other instruction, if it requires a delay because it is busy with other activities.

Automatically resetting into the default state requires the removal of bias supply from the controllers.

| Bit Position | Flag | Default Value |
|---|---|---|
| 7 | Bus 1 command error | 0 |
| 6 | Bus 1 Alert# enabled | 0 |
| 5 | Bus 1 requested control | 0 |
| 4 | Bus 1 has control of the PS | 0 |
| 3 | Bus 0 command error | 0 |
| 2 | Bus 0 Alert# enabled | 0 |
| 1 | Bus 0 requested control | 0 |
| 0 | Bus 0 has control of the PS | 1 |

**Command Execution:** The master not in control can issue two commands on the bus, take_over_bus_control and clear_faults

**Take_over_Bus_Control (0xD8):** This command instructs the internal µC to switch command control over to the 'master' that initiated the request.

Actual transfer is controlled by the I²C selector section of the µC. A bus transfer only occurs during an idle state when the 'master' currently in control (in the execution process of a control command) has released the bus by issuing a STOP command. Control can be transferred at any time if the 'master' being released is executing a read instruction that does not affect the transfer of command control. Note; The µC can handle read instructions from both busses simultaneously.

The command follows PMBus™ standards and it is not executed until the trailing PEC is validated.

**Status Notifications:** Once control is transferred both Alert# lines should get asserted by the I²C selector section of the µC. The released 'master' is notified that a STATUS change occurred and he is no longer in control. The connected 'master' is notified that he is in control and he can issue commands to the power supply. Each master must issue a clear_faults command to clear his Alert# signal.

If the Alert# signal was actually triggered by the power supply and not the I²C selector section of the µC, then only the 'master' in control can clear the power supply registers.

Incomplete transmissions should not occur on either bus.

**EEPROM record (0xD9):** The µC contains 64 bytes of reserved EEPROM space for customer use. After the command code, the starting memory location must be entered followed by a block write, and terminated by the PEC number;

| 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|
| S | Slave address | Wr | A | Command Code 0xD9 | A |

| 8 | 1 | 8 | 1 |
|---|---|---|---|
| Start location | A | Byte count | A |

| 8 | 1 | | 8 | 1 |
|---|---|---|---|---|
| first_byte | A | ........................................ | last - byte | A |

| 8 | 1 | 1 |
|---|---|---|
| PEC | A | P |

To read contents from the EEPROM space

| 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|
| S | Slave address | Wr | A | Command 0xD9 | A |

| 8 | 1 | 8 | 1 |
|---|---|---|---|
| Memory location | A | Byte count ≤ 32 | A |

| 1 | 7 | 1 | 1 |
|---|---|---|---|
| Sr | Slave address | Rd | A |

| 8 | 1 | | 8 | 1 |
|---|---|---|---|---|
| Byte 1 | A | ........................................ | Byte ≤ 32 | A |

| 8 | 1 | 1 |
|---|---|---|
| PEC | No-ack | P |

**Test Function (0xDF):** This command can be used to exercise the LEDs of the power supply and verify the functionality of the output Or'ing feature of the power supply.

| Bit | Function | State |
|---|---|---|
| 7 | 25ms stretch for factory use | 1= stretch ON |
| 5 - 6 | reserved | |
| 4 | Or'ing test | 1=ON, 0=OFF |
| 2 - 3 | reserved | |
| 1 | reserved | |
| 0 | LED test | 1=ON, 0=OFF |

**LEDS test ON:** Will turn-ON simultaneously the front panel LEDs of the Power supply sequentially 7 seconds ON and 2 seconds OFF until instructed to turn OFF. The intent of this function is to provide visual identification of the power supply being talked to and also to visually verify that the LEDs operate and driven properly by the micro controller.

**LEDS test OFF:** Will turn-OFF simultaneously the four front panel LEDs of the Power supply.

**OR'ing Test:** This command verifies functioning of output OR'ing. At least two paralleled power supplies are required. The host should verify that N+1 redundancy is established. If N+1 redundancy is not established the test can fail. Only one power supply should be tested at a time.

Verifying test completion should be delayed for approximately 30 seconds to allow the power supply sufficient time to properly execute the test.

Failure of the isolation test is not considered a power supply FAULT because the N+1 redundancy requirement cannot be verified. The user must determine whether a true isolation fault indeed exists.

## General performance descriptions

**Default state:** Power supplies are programmed in the default state to automatically restart after a shutdown has occurred. The default state can be reconfigured by changing non-volatile memory (Store_user_code).

**Delayed overcurrent shutdown during startup:** Power supplies are programmed to stay in a constant current state for up to 20 seconds during power up. This delay has been introduced to permit the orderly application of input power to a subset of paralleled power supplies during power up. If the overload persists beyond the 20 second delay, the power supply will revert back into its programmed state of overload protection.

**Unit in Power Limit or in Current Limit:** When output voltage is > $10V_{DC}$ the Output LED will continue blinking. When output voltage is < $10V_{DC}$, if the unit is in the RESTART mode, it goes into hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output LED is OFF.

**Restart after a latchoff:** **PMBus™** fault_response commands can be configured to direct the power supply to remain latched off for over_voltage, over_temperature and over_current.

To restart after a latch off either of five restart mechanisms are available.

1. The hardware pin **ON/OFF** may be cycled OFF and then ON**.**
2. The unit may be commanded to restart via $I^2C$ through the *Operation* command by cycling the output OFF followed by ON.
3. Remove and reinsert the unit.
4. Turn OFF and then turn ON AC power to the unit.
5. Changing firmware from **latch off** to **restart.**

Each of these commands must keep the power supply in the OFF state for at least 2 seconds, with the exception of changing to **restart**.

A successful restart shall clear all alarm registers, set the **restarted successful** bit of the ***Status_2*** register.

A power system that is comprised of a number of power supplies could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual power supplies. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all power supplies,
2. Toggling Off and then ON the ON/OFF (ENABLE) signal
3. Removing and reapplying input commercial power to the entire system.

The power supplies should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual power supplies.

**Auto_restart:** Auto-restart is the default configuration for over-current and over-temperature shutdowns. These features are configured by the **PMBus™** fault_response commands

An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again

## Fault management

Certain transitionary states can occur before a final state is reached. The STATUS and ALARM registers will not be frozen into a notification state until the final state is reached. Once a final state is reached the Alert# signal is set and the STATUS and ALARM registers will not get reinstated until a clear_faults is issued by the master. The only exception is that additional state changes may be added to the original list if further changes are noted.

All fault information is sticky. If the fault still persists after a clear_faults has been issued, then the fault state will reassert. All operational state information is not sticky.

The power supply differentiates between **internal faults** that are within the power supply and **external faults** that the power supply protects itself from, such as overload or input voltage out of limits. The FAULT LED, FAULT PIN or i2c alarm is not asserted for EXTERNAL FAULTS. Every attempt is made to annunciate External Faults. Some of these annunciations can be observed by looking at the input LEDs. These fault categorizations are predictive in nature and therefore there is a likelihood that a categorization may not have been made correctly.

**Input voltage out of range:** The Input LED will continue blinking as long as sufficient power is available to power the LED. If the input voltage is completely gone the Input LED is OFF.

## State change definition

A **state_change** is an indication that an event has occurred that the MASTER should be aware of. The following events shall trigger a **state_change**;

- Initial power-up of the system when AC gets turned ON . This is the indication from the power supply that it has been turned ON.
- Whenever the power supply gets hot-plugged into a working system. This is the indicator to the system (MASTER) that a new power supply is on line.
- Any changes in the bit patterns of the STATUS and ALARM registers are a STATUS change which triggers the ALERT# flag.

Note that a host-issued command such as turning the output OFF will not trigger an Alert# even though the STATUS registers will change to indicate the latest state of the power supply.

## Communications during hot plug

Careful system control is recommended when hot plugging a power supply into a live system. It takes about 15 seconds for a power supply to configure its address on the bus based on the analog voltage levels present on the backplane. If communications are not stopped during this interval, multiple power supplies may respond to specific instructions because the address of the hot plugged power supply always defaults to xxxx000 (depending on which device is being addressed within the power supply) until the power supply configures its address.
The recommended procedure for hot plug is the following: The system controller should poll the module_present signal to verify when a power supply is inserted into the system. When a new module is detected the system controller should cease any communications with the power system for 15 seconds. At the end of the time out all communications can resume. Note that although hot-plug should not affect ongoing communications, if a discrepancy should arise the error should get picked up by the PEC calculation. Ofcourse the system controller could always use the module_present signal as an indicator to ignore communications that are currently taking place.

## Failure Predictions

Alarm warnings that do not cause a shutdown are indicators of potential future failures of the power supply. For example, if a thermal sensor failed, a warning is issued but an immediate shutdown of the power supply is not warranted.

Another example of potential predictive failure mechanisms can be derived from information such as fan speed when multiple fans are used in the same power supply. If the speed of the fans varies by more than 20% from each other, this is an indication of an impending fan wear out.

The goal is to identify problems early before a protective shutdown would occur that would take the power supply out of service.

**Information only alarms:** The following alarms are for information only, they do not cause a shutdown

- Over temperature warning
- $V_{out}$ out-of-limits
- Output voltage lower than bus
- Unit in Power Limit
- Thermal sensor failed
- Or'ing (Isolation) test failure
- Power delivery
- Stby out of limits
- Communication errors

## LEDs

Two LEDs are located on the front faceplate. The AC_OK LED provides visual indication of the INPUT signal function. When the LED is ON GREEN the power supply input is within normal design limits.

The second LED DC/FLT is a dual-state LED. When GREEN there are no faults and DC output is present. When 'blinking' a fault condition exists but the power supply may still provide some output power. When RED , a fault condition exists and the power supply has been shut down, it does not provide any output power.

## Remote upgrade

This section describes at a high-level the recommended re-programming process for the three internal micro controllers inside the power supply when the re-programming is implemented in live, running, systems.

The process has been implemented in visual basic by GE Critical Power for controller based systems positioned primarily for the telecommunications industry. GE Critical Power will share its development with customers who are interested to deploy the re-programming capability into their own controllers.

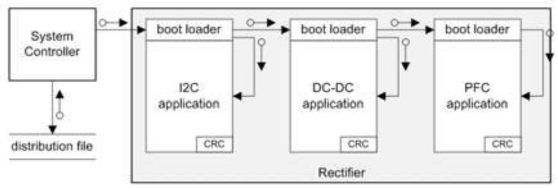
For some customers' internal system re-programming is either not feasible or not desired. These customers may obtain a re-programming kit from GE Critical Power. This kit contains a turn-key package with the re-program firmware.

### In-system remote upgrade

**Conceptual Description:** The power supply contains three independent μControllers. The boost (PFC) section is controlled by the primary μController. The secondary DC-DC converter is controlled by the secondary μController, and $I^2C$ communications are being handled by the $I^2C$ Interface μController.

Each of the μControllers contains a **boot loader** section and an **application** section in memory. The purpose of the boot loader section is to facilitate the upgrading capability described here. All the commands for upgrading and memory space required for incrementally changing the application code are in this section. The application section contains the running code of the power supply.

The system controller receives the upgrade package. It should first check whether an upgrade is required followed by upgrading those processors, one at a time, that are required to be upgraded. Each processor upgrade needs to be validated and once the upgrade is successfully completed the boot loader within each processor will permit the application to run after a reset. If the validation fails the boot loader will stay in its section. The system controller can attempt another upgrade session to see if it would complete successfully.




**The Upgrade Package:** This package contains the following files;

- **Manifest.txt** - The manifest describes the contents of the upgrade package and any incidental information that may be useful, for example, what this upgrade contains or why is this upgrade necessary

  This file contains the version number and the compatibility code of the upgraded program for each of the three processors

- **Program.bin** - The upgraded program contents are located here. Each processor to be upgraded will have its own file.

Below is an example of an upgrade package

- Contents of the upgrade are in a zip file
  CAR3012TExxxZ01A.zip

- Unzipping the contents shows the following files
  CAR3012TExxxZ01A.pfc.bin
  CAR3012TExxxZ01A.sec.bin
  CAR3012TEXXXZ01A.iic.bin
  manifest.txt

- Opening manifest.txt shows the following
  # Upgrade manifest file
  # Targets: CAR3012TExxxZ01A PFC and SEC
  # Date: Tue 01/14/2014 14:25:09.37
  # Notes:

  >p,CAR3012TE_P01, CAR3012TExxxZ01A _PFC.bin,1.18
  >s,CAR3012TE_S01, CAR3012TExxxZ01A _SEC.bin,1.1
  >i, CAR3012TE_I01, CAR3012TExxxZ01A _IIC.bin,2.5

  compatibility code, new program, revision number

**Upgrade Status Indication:** The FAULT LED is utilized for indicating the status of the re-programming process.

| Status | Fault LED | Description |
|---|---|---|
| Idle | OFF | Normal state |
| In boot block | Wink | Application is good |
| Upgrading | Fast blink | Application is erased or programming in progress |
| Fault | ON | Erase or re-program failed |

Wink: 0.25 seconds ON, 0.75 seconds OFF
Fast Blink: 0.25 seconds ON. 0.25 seconds OFF

## Upgrade procedure

1. Initialization: To execute the re-programming/upgrade in the system, the power supply to be re-programmed must first be taken OFF-line prior to executing the upgrade.

   **Note: If the power supply is not taken OFF-line by the system controller, the boot loader will turn OFF the output prior to continuing with the re-programming operation.**

   **Make sure that sufficient power is provided by the remaining on-line power supplies so that system functionality is not jeopardized.**
2. Unzip the distribution file
3. Unlock upgrade execution protection by issuing the command below;

**Password(0xE0):** This command unlocks the upgrade commands feature of the power supply by sending the characters 'UPGD'.

| 1 | 8 | | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|
| S | Slave addr | Wr | A | Cmd – 0xE0 | A | Byte count - 4 | A |

| 8 | 1 |
|---|---|
| Byte 0 - U | A |

…………

| 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|
| Byte 4 - D | A | PEC | A | P |

4. None of the upgrade commands in a processor can be executed until that processor is placed into boot block mode. To enter boot block mode, the Boot Loader (0xE6) command must be executed next with the instruction for the processor to enter boot block – data: 1=enter boot block.

   The sequence for the upgrade is as follows:
   - enter the processor into boot block
   - erase the application
   - execute the upgrade
   - exit from the processor boot block

   This sequence needs to be repeated for each processor. The sequence of upgrade does not matter if all processors are properly upgraded. The following instructions describe each of the commands.

   Perform the checks and balances, status verifications, sequence verifications, and validation error checking.

**Boot loader (0xE6):** This command manages the upgrade process starting with entering the sector, erasing the present application, indicating completion of the upload and finally exiting from the boot sector, thereby turning over control to the uploaded application.

| 1 | 7 | 7 | 7 | 8 | | 8 | |
|---|---|---|---|---|---|---|---|
| S | Slave addr | Wr | A | Cmd – 0xE6 | | Target-x | |

| 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|
| Data | A | PEC | A | P |

Data:
1=enter boot block (software reboot)
2=erase
3=done
4=exit[11] boot block (watchdog reboot)

**Notes: During this process if the output of the power supply was not turned OFF the boot loader will turn OFF the output.**

**Entering boot loader must be a sequential set of instructions. The iic processor must be entered first, followed by entering the boot loader of the secondary processor and finally the primary processor. Both the iic and the secondary processor must be maintained in boot loader while communicating to the primary processor.**

**Entering the primary or secondary boot loaders is not needed if only the iic processor is being upgraded.**

Wait at least 1 second after issuing an *erase* command to allow the μC to complete its task.

Use command 0xE5 to verify that the PFC μC is erased. The returned status byte should be 0x81.

Use the Data Transfer command to update the application of the target μC.

5. Obtain a list of upgradable processors (optional)

**Target list(0xE1) :** This command returns the upgradable processors within the power supply. The byte word is the ASCII character of the processor (p, s, and i). The command is optional to the user for information only.

| 1 | 8 | | 1 | 8 | 1 |
|---|---|---|---|---|---|
| S | Slave addr | Wr | A | Cmd – 0xE1 | A |

| 1 | 8 | | 1 | 8 | 1 |
|---|---|---|---|---|---|
| Sr | Slave addr | Rd | A | Byte count - n | A |

| 8 | 1 | | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|
| Byte 0 | A | ………… | Byte n | A | PEC | No-Ack | P |

Potential target processors are the following:

p – primary (PFC)
s – secondary (DC-DC)
i – $I^2C$

6. Verify upgrade compatibility by matching the upgrade compatibility code in the manifest.txt file to the power supply compatibility code of the target processor.

**Compatibility code (0xE2):** The compatibility code consists of up to 32 characters defining the hardware configuration. To read the compatibility codes of each processor in the module execute the following read:

| 1 | 8 | | 1 | 8 | | 8 | |
|---|---|---|---|---|---|---|---|
| S | Slave addr | Wr | A | Cmd – 0xE2 | | Target-x | / |

| 1 | 8 | | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|
| Sr | Slave addr | Rd | A | Byte count = 32 | A | Byte 0 | A |

| | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|
| …………… | Byte 31 | A | PEC | No-Ack | P |

Where Target-x is an ASCII character pointing to the processor to be updated;

p – primary (PFC)
s – secondary (DC-DC)
i – $I^2C$

7. Check the software revision number of the target processor in the power supply and compare it to the revision in the upgrade. If the revision numbers are the same, or the power supply has a higher revision number then no upgrade is required for the target processor.

**Software revision(0xE3):** This command returns the software revision of the target.

| 1 | 8 | | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|
| S | Slave addr | Wr | A | Cmd – 0xE3 | A | Target-x | A |

| 1 | 8 | | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|
| Sr | Slave addr | Rd | A | Byte count=7 | A | Major revision | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|
| Minor revision | A | month | A | day | A | year[12] | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| hrs | A | min | A | PEC | No-Ack | P |

[11] The 'exit boot block' command is only successful if all applications are valid, otherwise, control remains in the boot block

[12] Last two digits

8. Verify the capability of each processor

**Memory capability (0xE4):** Provides the specifics of the capability of the device to be reprogrammed

| 1 | 8 | | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|
| S | Slave addr | Wr | A | Cmd – 0xE4 | A | Target-x | A |

| 1 | 8 | | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|
| Sr | Slave addr | Rd | A | Byte count=7 | A | Max bytes | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|
| ET-LSB | A | ET-MSB | A | BT-LSB | A | BT-MSB | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| App_CRC_LSB | A | App_CRC_MSB | A | PEC | No-Ack | P |

Where the fields definition are shown as below:

| | |
|---|---|
| **Max Bytes** | Maximum number of bytes in a data packet |
| **ET** | Erase time for entire application space (in mS) |
| **BT** | Data packet write execution time (uS) |
| **APP_CRC** | returns the application CRC-16 calculation. |

This information should be used by the host processor to determine the max data packet size and add appropriate delays between commands.

9. Determine the status of the upgrade: The Application status command is used to verify the present state of the boot loader.

**Application status (0xE5):** Returns the Boot Loader's present status

| 1 | 8 | | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|
| S | Slave addr | Wr | A | Cmd – 0xE5 | A | Target-x | A |

| 1 | 8 | | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|
| Sr | Slave addr | Rd | A | Status | A | PEC | No-Ack | P |

Status bits:

| | |
|---|---|
| 0x00 Processor is available<br>0x01 Application erased<br>0x02 CRC-16 invalid<br>0x04 Sequence out of order<br>0x08 Address out of range | 0x10 Reserved<br>0x20 Reserved<br>0x40 Manages downstream µC<br>0x80 In boot loader |

Status of the application should be checked after the execution of successive commands to verify that the commands have been properly executed.

**Data transfer (0xE7):** The process starts with uploading data packets with the first sequence number (0x0000). Both the write and read commands need to include the target-x processor.

### Data transfer [write]

| 1 | 8 | | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|
| S | Slave addr | Wr | A | Cmd - 0xE7 | A | Target-x | A |

| 8 | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|
| Seq-LSB | A | Seq-MSB | A | Byte Count = n | A |

| 8 | 1 | | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|
| Byte 0 | A | ............ | Byte n-1 | A | PEC | A | P |

After completion of the first data packet upload the Boot loader increments the sequence number. A subsequent read to the boot loader will return the incremented sequence number and a STATUS byte. This is a validity check to ensure that the sequence number is properly kept. The returned STATUS byte is the same as the application status response. It is appended here automatically to save the execution of another command. It should be checked to ensure that no errors are flagged by the boot loader during the download. If an error occurred, terminate the download load and attempt to reprogram again.

### Data transfer [read]

**Note: Reading the sequence number needs to be delayed approximately 150ms after uploading a data packet in order to allow the processor to update the sequence number field.**

| 1 | 8 | | 1 | 8 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|
| S | Slave addr | Wr | A | Cmd - 0xE7 | A | Target-x | A |

| 1 | 8 | | 1 |
|---|---|---|---|
| Sr | Slave addr | Rd | A |

| 1 | 8 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|
| Seq-LSB | A | Seq-MSB | A | Status | A | PEC | No-Ack | P |

The returned Status byte is defined in the Application Status command (0 x E5).

Sequence number validation should take place after each data block transfer. The next data block transfer starts with the sequence number received from the boot loader.

The host keeps track of the upload and knows when the upload is completed.

10. Execute a Boot loader command to tell the µC that the transfer is done.

At the completion signal, the µC should calculate the PEC value of the entire application. The last two bytes of the loaded application were the CRC-16 based PEC calculation.

Wait for at least 1 second to allow time for the µC to calculate the error checking value.

11. Execute an Application status command to verify that the error check is valid. The returned status should be 0x80.