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Kind regards,

Team Nexperia

# CBTD3384

10-bit level shifting bus switch with 5-bit output enables

Rev. 8 — 12 December 2012

Product data sheet

## 1. General description

The CBTD3384 provides ten bits of high-speed TTL-compatible bus switching. The low ON resistance of the switch allows connections to be made with minimal propagation delay.

The CBTD3384 device is organized as two 5-bit bus switches with two separate output enable (1OE, 2OE) inputs. When nOE is LOW, the switch is on and port A is connected to the B port. When nOE is HIGH, each switch is disabled.

The CBTD3384 is characterized for operation from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

## 2. Features and benefits

- Designed to be used in 5 V to 3.3 V level shifting applications with internal diode
- $5\ \Omega$  switch connection between two ports
- TTL-compatible control input levels
- Multiple package options
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ CDM JESD22-C101C exceeds 1000 V

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
CBTD3384D	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
CBTD3384DB	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
CBTD3384DK	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SSOP24 <sup>[1]</sup>	plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT556-1
CBTD3384PW	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

[1] Also known as QSOP24 package



## 4. Functional diagram

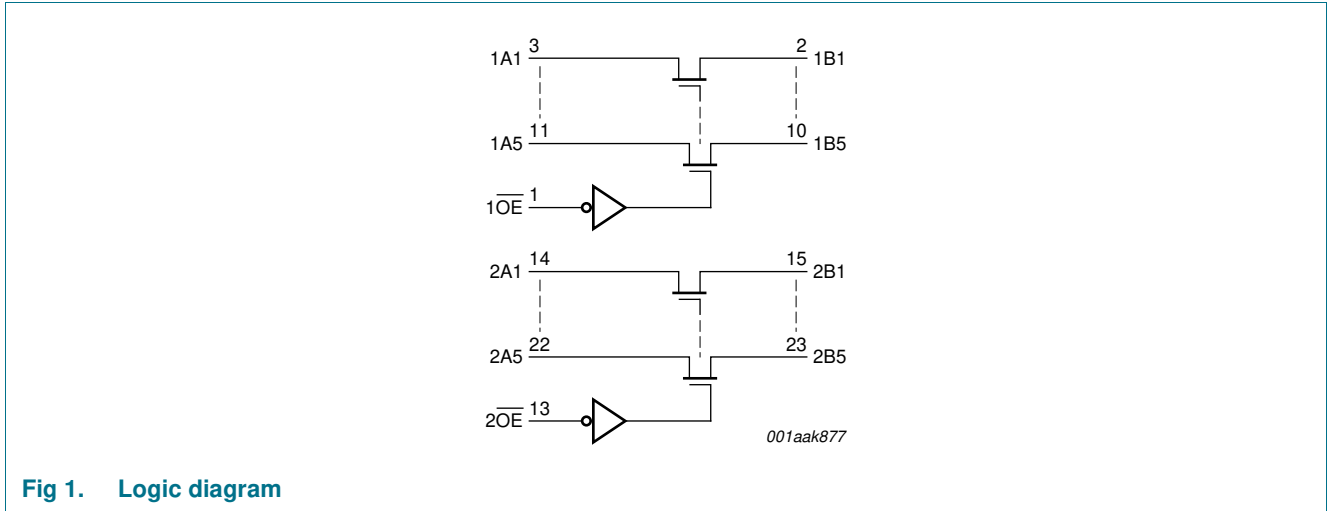


Fig 1. Logic diagram

## 5. Pinning information

### 5.1 Pinning

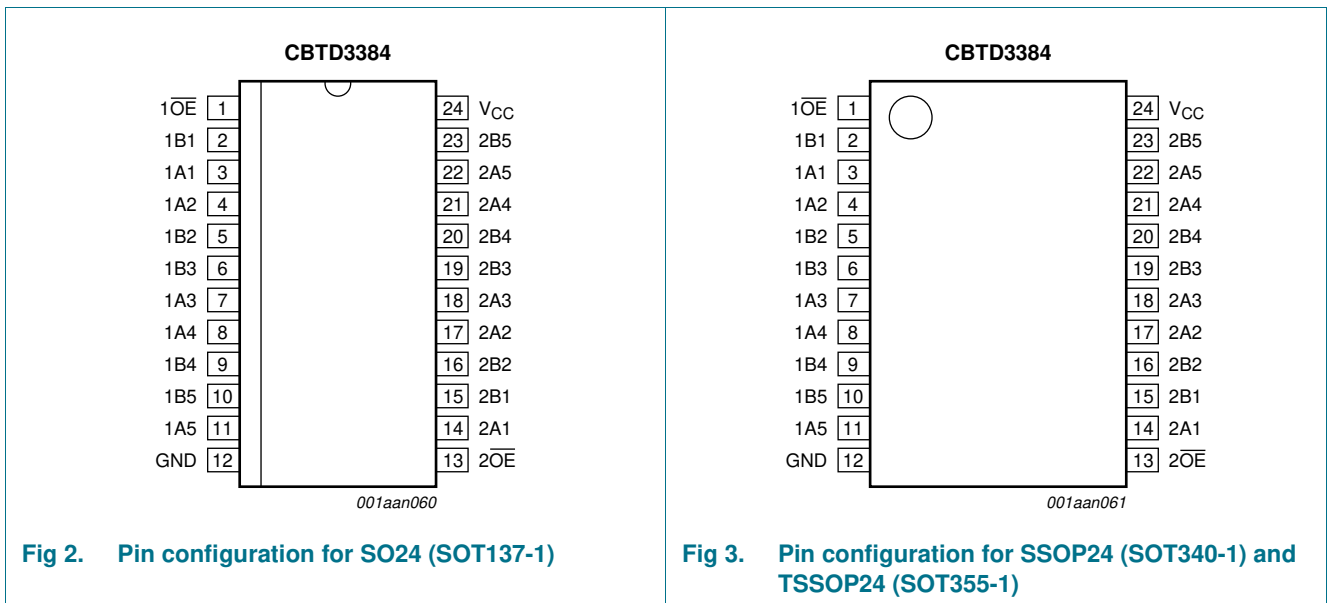


Fig 2. Pin configuration for SO24 (SOT137-1)

Fig 3. Pin configuration for SSOP24 (SOT340-1) and TSSOP24 (SOT355-1)

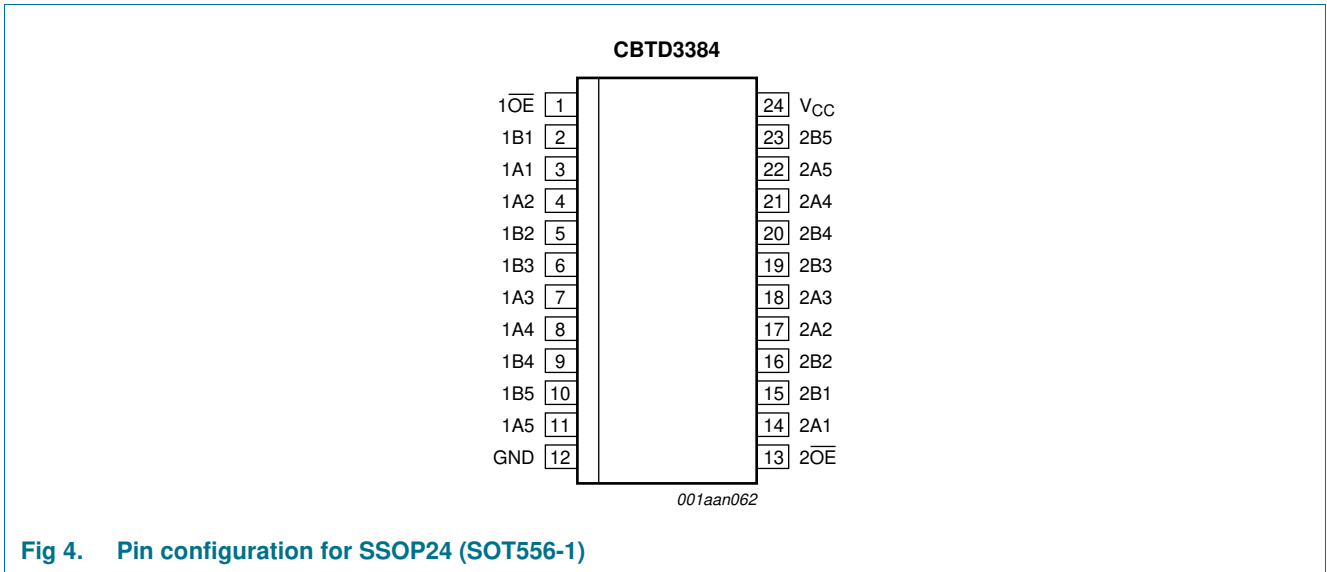


Fig 4. Pin configuration for SSOP24 (SOT556-1)

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 13	output enable input (active LOW)
1A1 to 1A5	3, 4, 7, 8, 11	data input/output (A port)
2A1 to 2A5	14, 17, 18, 21, 22	data input/output (A port)
1B1 to 1B5	2, 5, 6, 9, 10	data input/output (B port)
2B1 to 2B5	15, 16, 19, 20, 23	data input/output (B port)
GND	12	ground (0 V)
VCC	24	positive supply voltage

## 6. Functional description

Table 3. Function selection<sup>[1]</sup>

Input		Input/output	
1OE	2OE	1An, 1Bn	2An, 2Bn
L	L	1An = 1Bn	2An = 2Bn
L	H	1An = 1Bn	Z
H	L	Z	2An = 2Bn
H	H	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).<sup>[1]</sup>

$T_{amb} = -40\text{ °C to }+85\text{ °C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		<sup>[2]</sup> -0.5	+7.0	V
$I_O$	output current	$V_O < 0\text{ V}$	-	$\pm 128$	mA
$I_{IK}$	input clamping current	$V_{I/O} = 0\text{ V}$	-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Section 8](#), is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	-	5.5	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$T_{amb}$	ambient temperature	operating in free air	-40	-	+85	°C

## 9. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

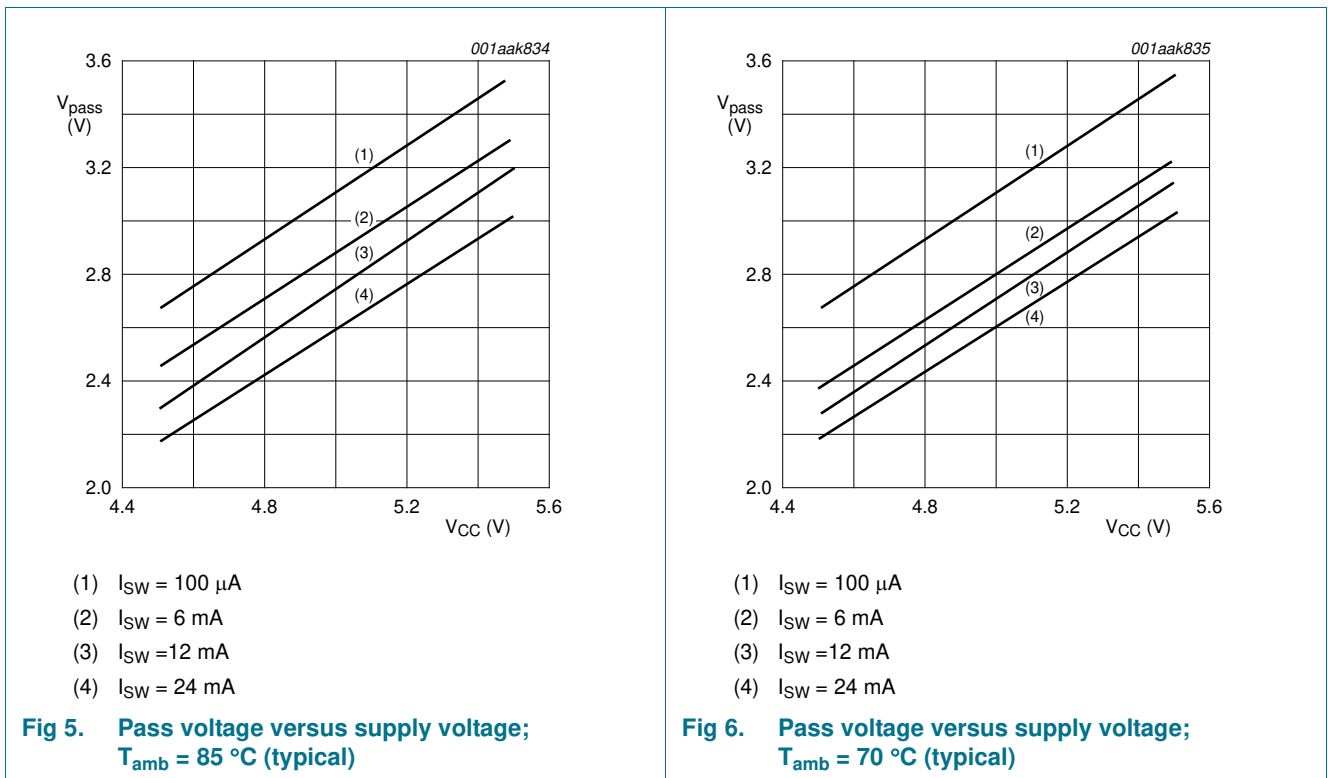
Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			Unit
			Min	Typ <sup>[1]</sup>	Max	
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5\text{ V}; I_I = -18\text{ mA}$	-	-	-1.2	V
$I_I$	input leakage current	$V_{CC} = 5.5\text{ V}; V_I = \text{GND or } 5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{CC}$	supply current	$V_{CC} = 5.5\text{ V}; I_O = 0\text{ mA};$ $V_I = V_{CC}\text{ or GND}$	-	-	1.5	mA
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 5.5\text{ V}$ ; one input at 3.4 V, other inputs at $V_{CC}$ or GND	<sup>[2]</sup> -	-	2.5	mA
$V_{pass}$	pass voltage	see <a href="#">Figure 5</a> to <a href="#">Figure 9</a>	-	-	-	V
$C_I$	input capacitance	control pins; $V_I = 3\text{ V or } 0\text{ V}$	-	3.2	-	pF
$C_{io(off)}$	off-state input/output capacitance	port off; $V_I = 3\text{ V or } 0\text{ V}; \overline{nOE} = V_{CC}$	-	6.0	-	pF

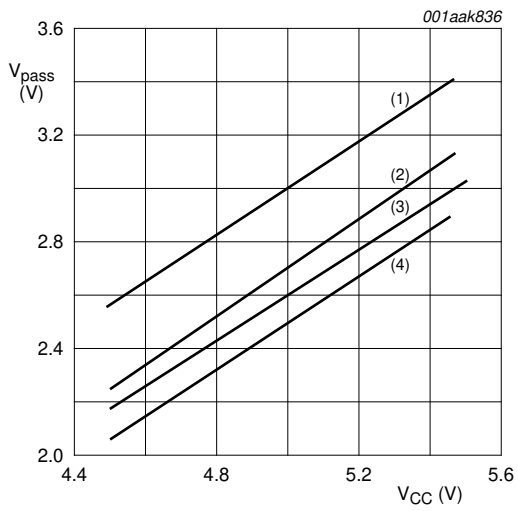
**Table 6. Static characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
R <sub>ON</sub>	ON resistance	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 64 mA <sup>[3]</sup>	-	5	7	Ω
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 30 mA <sup>[3]</sup>	-	5	7	Ω
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 2.4 V; I <sub>I</sub> = -15 mA <sup>[3]</sup>	-	17	50	Ω

- [1] All typical values are at V<sub>CC</sub> = 5 V, T<sub>amb</sub> = 25 °C.
- [2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.
- [3] Measured by the voltage drop between the nAn and the nBn terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (nAn or nBn) terminals.

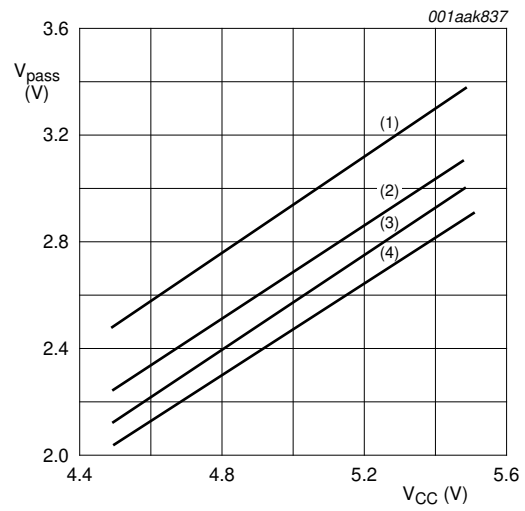
### 9.1 Typical pass voltage graphs





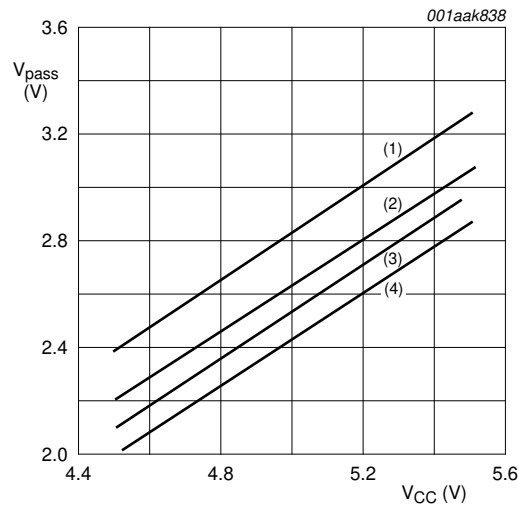
- (1) I<sub>SW</sub> = 100 μA
- (2) I<sub>SW</sub> = 6 mA
- (3) I<sub>SW</sub> = 12 mA
- (4) I<sub>SW</sub> = 24 mA

Fig 7. Pass voltage versus supply voltage; T<sub>amb</sub> = 25 °C (typical)



- (1) I<sub>SW</sub> = 100 μA
- (2) I<sub>SW</sub> = 6 mA
- (3) I<sub>SW</sub> = 12 mA
- (4) I<sub>SW</sub> = 24 mA

Fig 8. Pass voltage versus supply voltage; T<sub>amb</sub> = 0 °C (typical)



- (1) I<sub>SW</sub> = 100 μA
- (2) I<sub>SW</sub> = 6 mA
- (3) I<sub>SW</sub> = 12 mA
- (4) I<sub>SW</sub> = 24 mA

Fig 9. Pass voltage versus supply voltage; T<sub>amb</sub> = -40 °C (typical)



## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

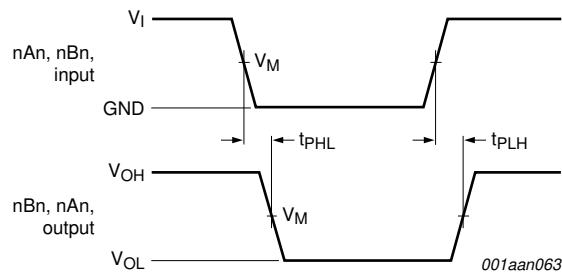
Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ	Max	
t <sub>pd</sub>	propagation delay	nAn, nBn to nBn, nAn; see <a href="#">Figure 10</a> <sup>[1][2]</sup> V <sub>CC</sub> = 5.0 V ± 0.5 V	-	-	0.25	ns
t <sub>en</sub>	enable time	nOE to nAn or nBn; see <a href="#">Figure 11</a> <sup>[2]</sup> V <sub>CC</sub> = 5.0 V ± 0.5 V	1.2	4.3	7.0	ns
t <sub>dis</sub>	disable time	nOE to nAn or nBn; see <a href="#">Figure 11</a> <sup>[2]</sup> V <sub>CC</sub> = 5.0 V ± 0.5 V	1.7	3.0	5.3	ns

[1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
 t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
 t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

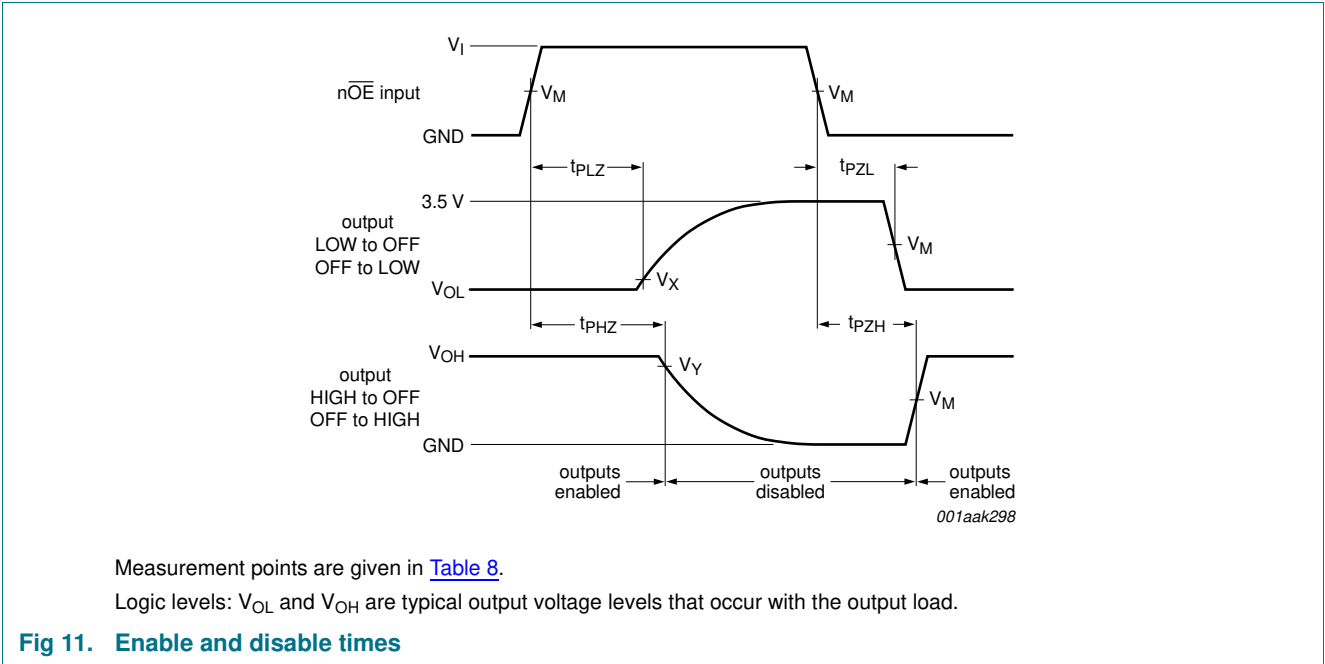
## 11. Waveforms



Measurement points are given in [Table 8](#).

Logic levels: V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage levels that occur with the output load.

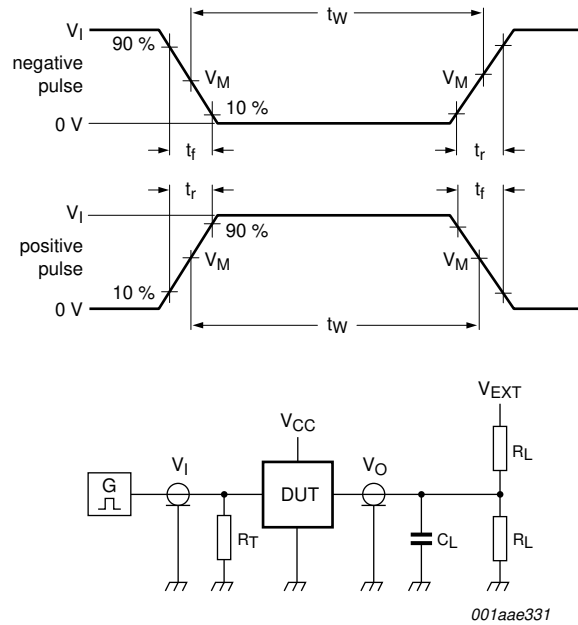
**Fig 10. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times**



**Table 8. Measurement points**

Supply voltage	Input		Output		
$V_{CC}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	GND to 3.0 V	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

12. Test information



Test data is given in [Table 9](#).

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z<sub>o</sub> = 50 Ω.

The outputs are measured one at a time with one transition per measurement.

Definitions for test circuit:

R<sub>L</sub> = Load resistance.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to output impedance Z<sub>o</sub> of the pulse generator.

V<sub>EXT</sub> = External voltage for measuring switching times.

Fig 12. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V <sub>EXT</sub>		
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>
V <sub>CC</sub> = 5.0 V ± 0.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

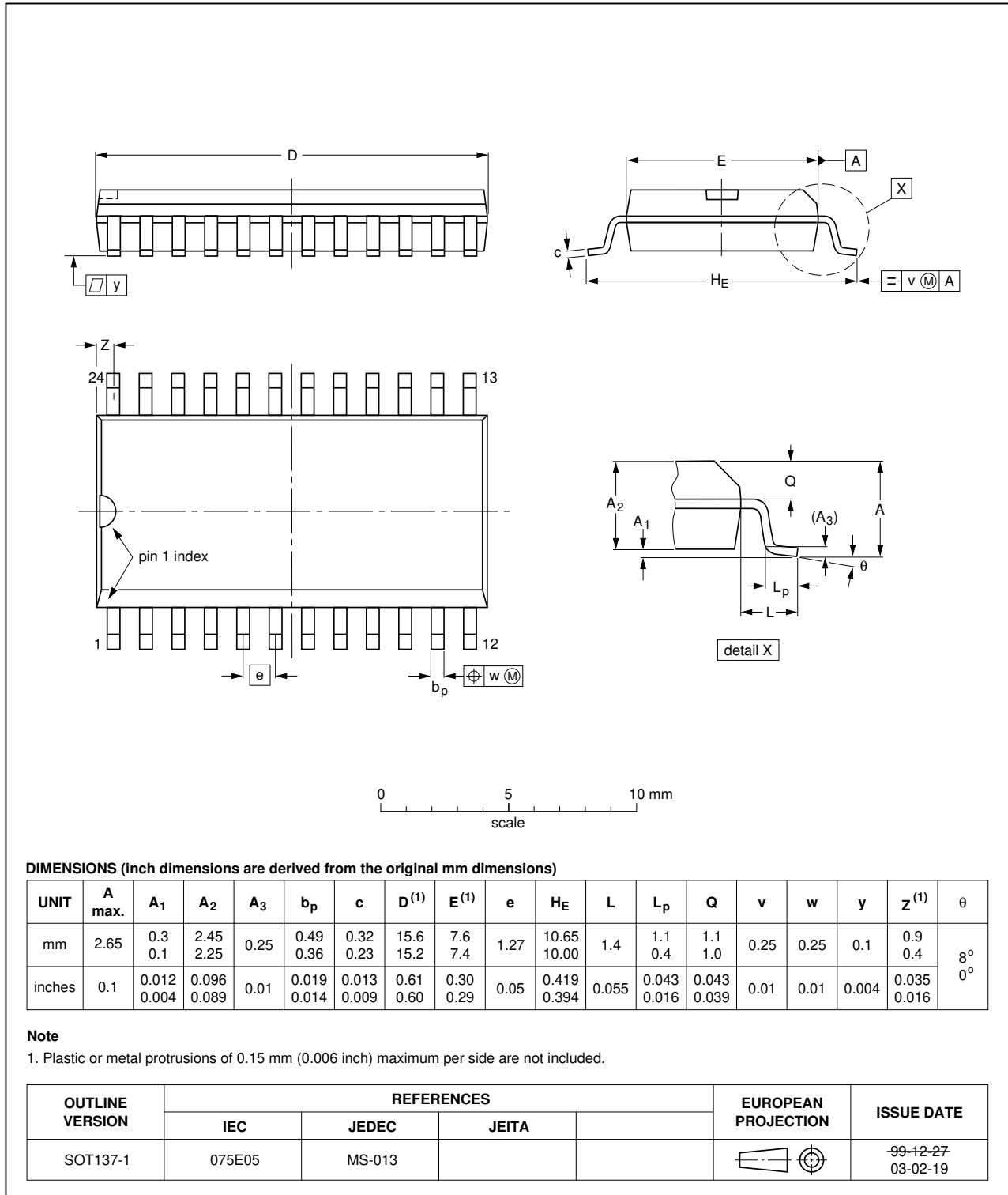


Fig 13. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

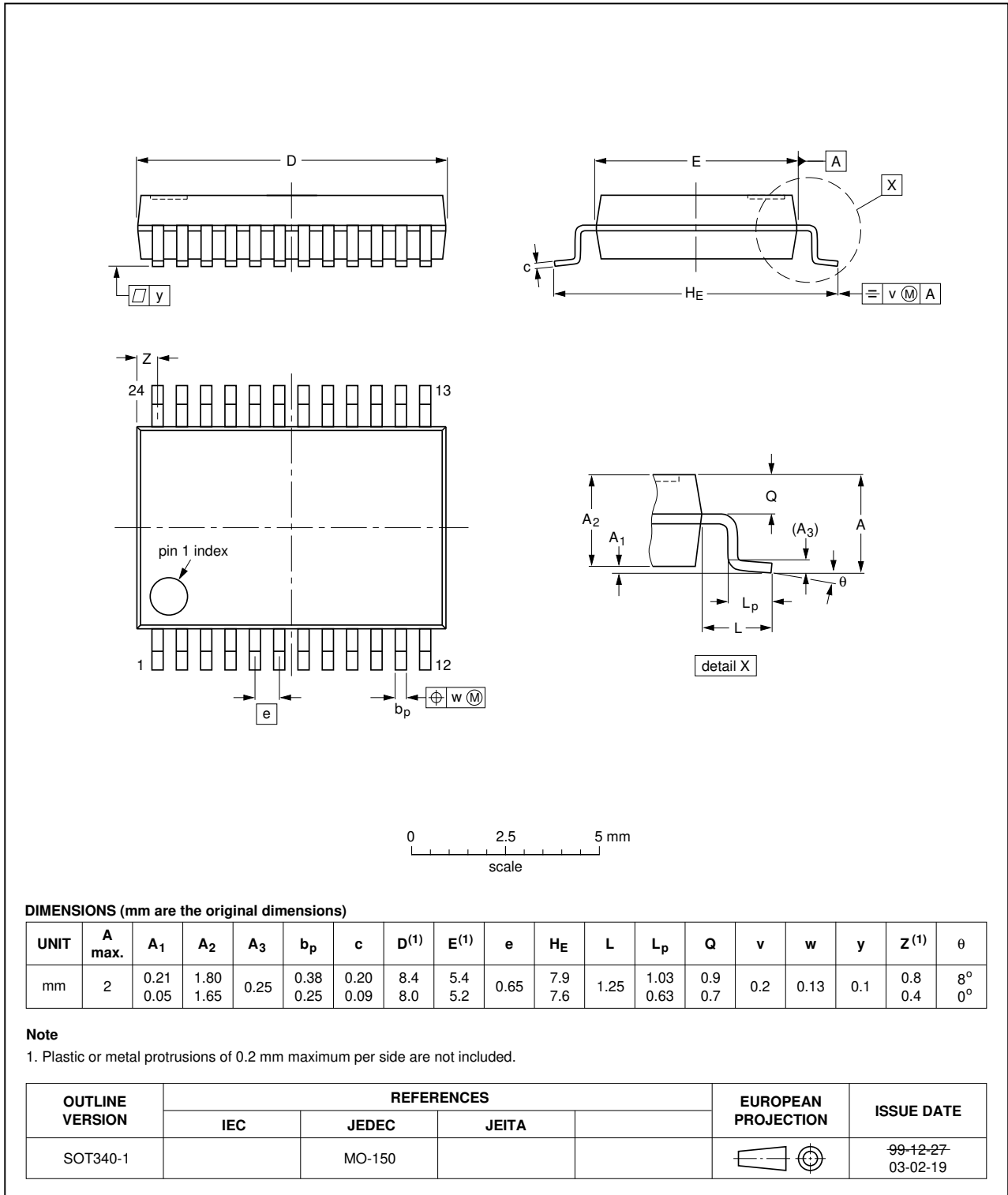


Fig 14. Package outline SOT340-1 (SSOP24)

SSOP24: plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm SOT556-1

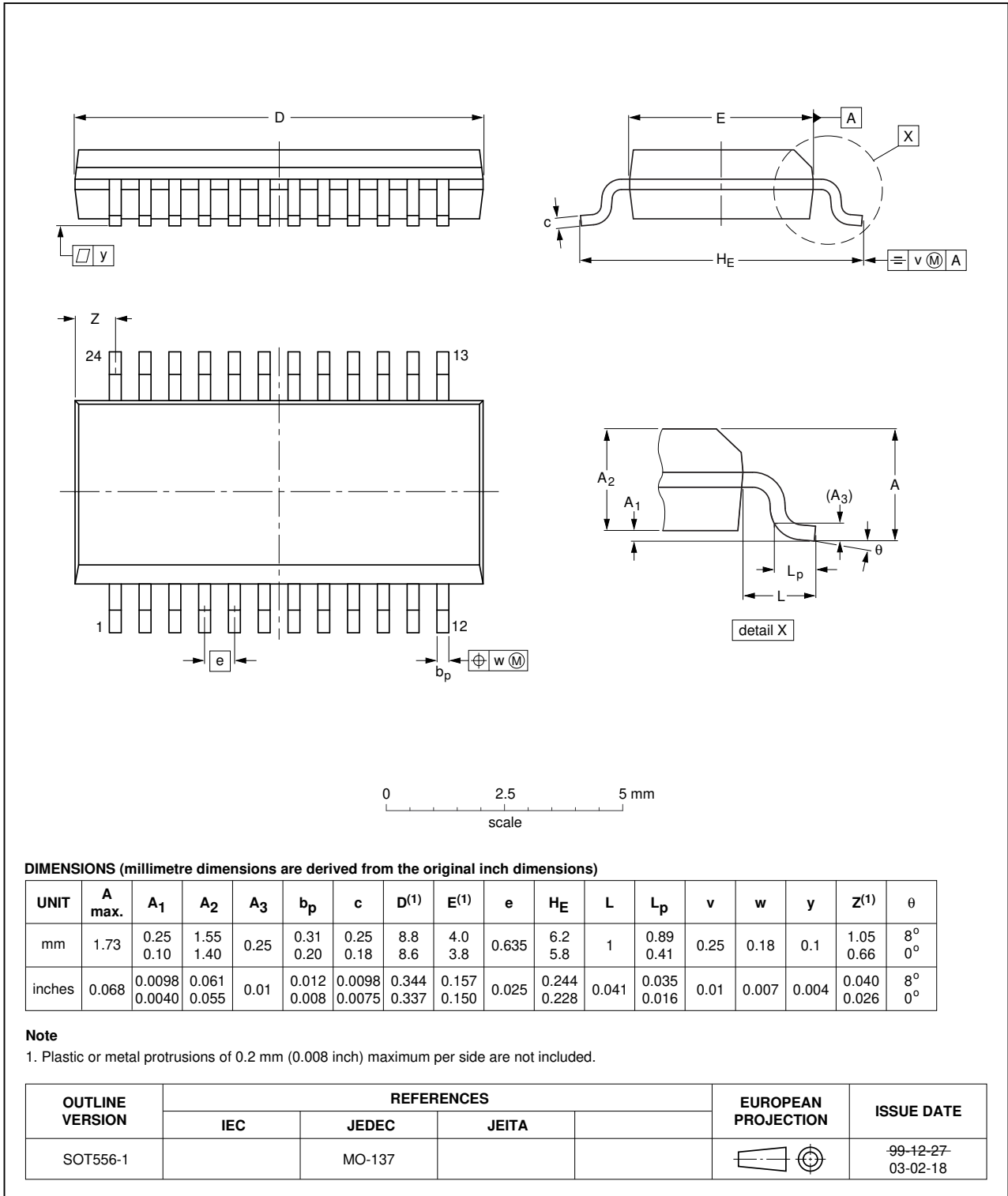


Fig 15. Package outline SOT556-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

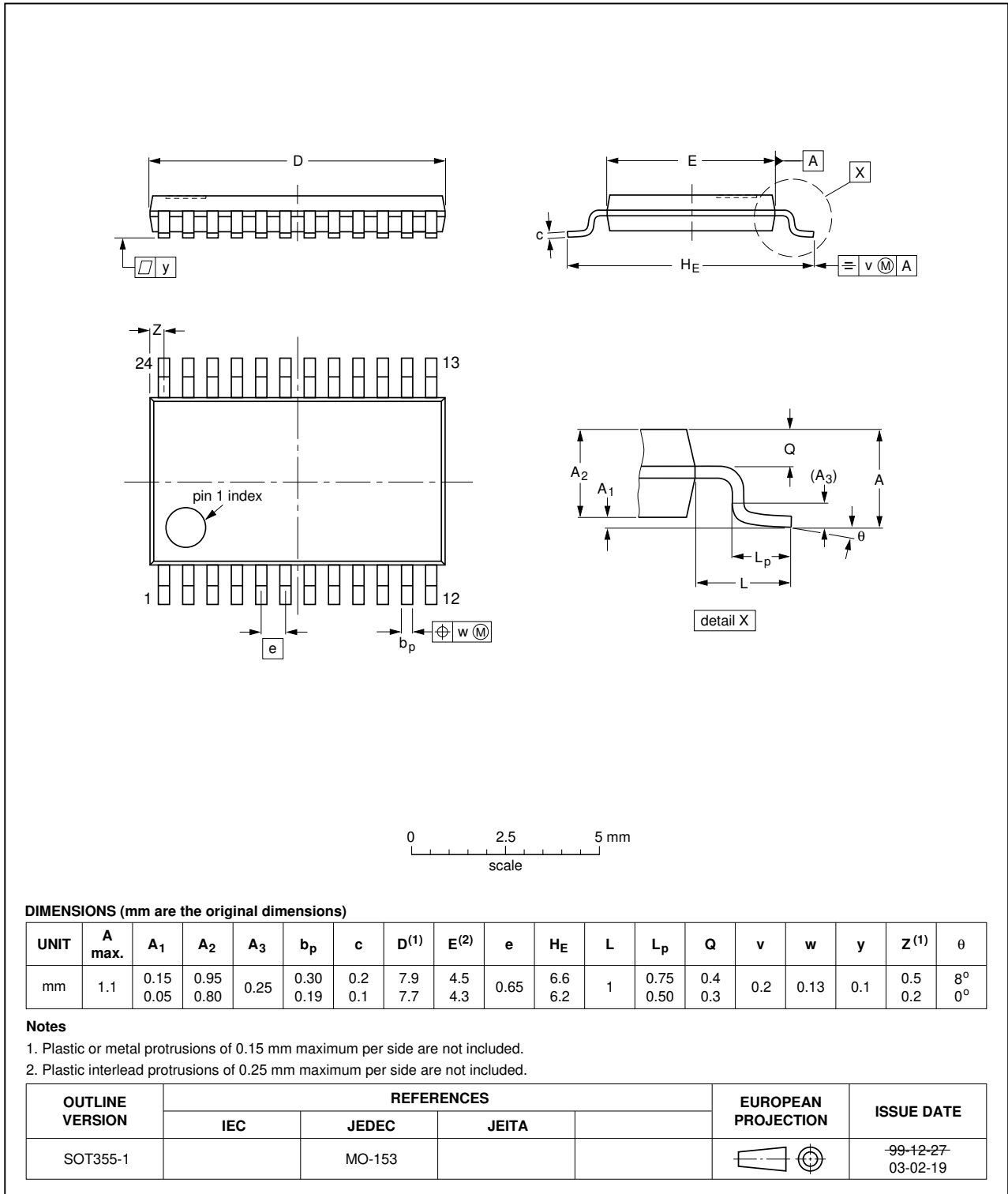


Fig 16. Package outline SOT355-1 (TSSOP24)

## 14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTD3384 v.8	20121212	Product data sheet	-	CBT3384 v.7
Modifications:	<ul style="list-style-type: none"> <li>Table 1: changed +125 °C into +85 °C (errata).</li> </ul>			
CBTD3384 v.7	20121119	Product data sheet	-	CBT3384 v.6
Modifications:	<ul style="list-style-type: none"> <li>Table 1: changed +85 °C into +125 °C (errata).</li> </ul>			
CBTD3384 v.6	20111121	Product data sheet	-	CBTD3384 v.5
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
CBTD3384 v.5	20101119	Product data sheet	-	CBTD3384 v.4
CBTD3384 v.4	20011220	Product specification		CBTD3384 v.3
CBTD3384 v.3	20000830	Product specification	-	CBTD3384 v.2
CBTD3384 v.2	20000830	Product specification	-	-



## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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## 18. Contents

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