Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CBTL08GP053

USB Type-C High performance Crossbar Switch IC

Rev. 2 — 1 August 2016 Product data sheet

1. General description

CBTL08GP053 is a USB Type-C High Performance Crossbar Switch IC meant to be used for Type-C connector interface high speed passive switching applications. It provides switching of high speed differential signals that correspond to various interface standards: USB3.1 (10 Gbps), DP1.3 (8.1 Gbps), PCI Express 3.0 (8 Gbps), etc. It supports switching of single ended signals over Type-C interface. In addition, side band switching of AUX and other dedicated signals for transport over SBU1 and SBU2.

It provides the I^2C-bus interface for switch control, configuration and status update. It operates from a single platform power supply V_{DD}.

This IC is targeted for a wide range of platforms (PCs, tablets, convertibles, smart phones) and PC accessories (e.g. docks, monitors, etc.) applications.

CBTL08GP053 is available in a small footprint package option: VFBGA40 4.75 mm × 3.25 mm, 0.5 mm pitch.

2. Features and benefits

2.1 High speed switch features

- Supports the following interface standards: USB3.1, DP1.3, DP++, PCIe 3.0
- Supports signaling rates up to 10 Gbps
- Performs multiplexing or switching of high speed differential signals or single ended signals
- All switches are direction agnostic
- Design based on both patented and patent pending high performance switch technology
- Target performance specification
  - Differential signaling (peak to peak) of 1.4 V and common mode level over 0 V to 2.2 V
  - 1.8 V single ended rail to rail signaling
  - R_{on}: 7 Ω (typ)
  - Insertion loss: 1.2 dB at 2.7 GHz, 1.8 dB at 5.4 GHz, 3dB at 8.5 GHz (typ)
  - Isolation: 23 dB at 2.7 GHz, 16.5 dB at 5.4 GHz (typ)
  - Cross talk: 32 dB at 2.7 GHz, 24 dB at 5.4 GHz (typ)
  - Return loss: 20 dB at 2.7 GHz, 16 dB at 5.4 GHz (typ)
- Very low intra pair skew
- Very low propagation delay (80 ps typical) and inter pair skew (35 ps typical)

- Switch paths selectable through the I²C-bus interface (registers for atomic and sequential switch selection)

2.2 Sideband auxiliary crossbar switch features

- Single ended 2:1 multiplexing/switching with single ended cross bar switching of both differential AUX or single ended UART or I2C or miscellaneous signals
- Switches are direction agnostic
- Switches are 5.5 V tolerant
- Target performance specification (typical values)
  - R_{on} 8 Ω (typ) at V_{cm} = 0.5 V to 2.65 V
- Very low intra pair skew
- Very low propagation delay (80 ps typical)
- Switch paths selectable through the I²C-bus interface (registers for atomic and sequential switch selection)

2.3 General

- Supports I2C slave interface Standard mode (100 kbit/s) and Fast mode (400 kbit/s)
- I2C slave address programmable up to 4 values
- Back current protection on control pins and exposed connector side I/O pins
- Single 3.3V power supply
- Current consumption
  - Active mode (all switches are functional): 300 μA (typ)
  - Standby mode (all switches in Hi-Z): 15 μA (max)
- Operating temperature: −40 to 105 °C
- ESD 2 kV HBM, 500 V CDM
- Package: VFBGA40 4.75 mm × 3.25 mm, 0.5 mm pitch

3. Applications

- PC platforms: notebook PCs, desktop PCs, ultrabooks
- Tablets, 2:1 convertibles, smartphones and portable devices
- PC accessories/peripherals: multi-function monitors, etc.

4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
CBTL08GP053EV[1]	GP053	VFBGA	plastic, very fine-pitch ball grid array package; body 4.75 mm × 3.25 mm × 0.92 mm; 0.5 mm pitch	SOT1439-1

[1] Total height after printed-circuit board mounting ≤1 mm (maximum)

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
CBTL08GP053EV	CBTL08GP053EVY	VFBGA	Reel 13" Q1/T1 *standard mark SMD DP	5000	T_{amb} = −40 °C to +85 °C

5. Block diagram

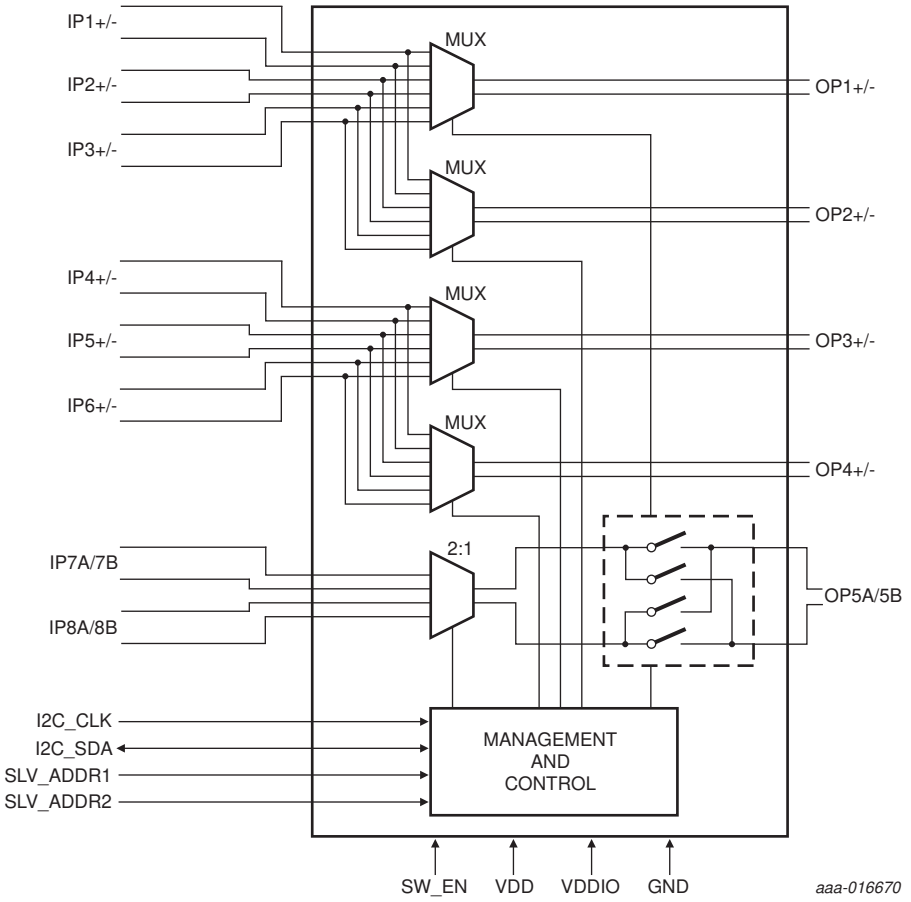


Fig 1. CBTL08GP053 functional block diagram

6. Pinning information

6.1 Pinning

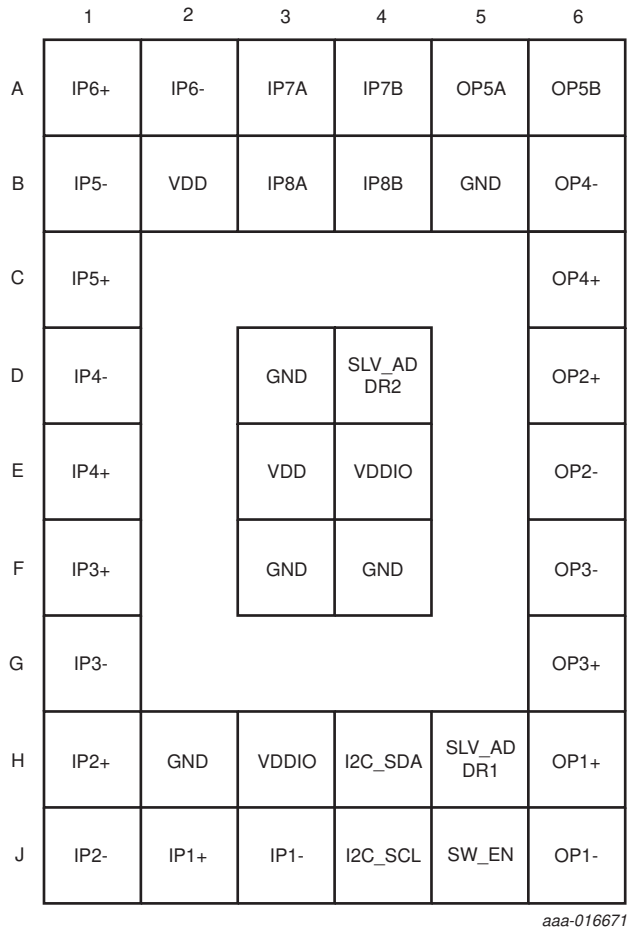


Fig 2. CBTL08GP053 pinning diagram (transparent top view)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
IP1+	J2	Differential I/O	Six high-speed differential pairs for DisplayPort, PCI Express, USB3 on system side
IP1-	J3	Differential I/O	
IP2+	H1	Differential I/O	
IP2-	J1	Differential I/O	
IP3+	F1	Differential I/O	
IP3-	G1	Differential I/O	
IP4+	E1	Differential I/O	
IP4-	D1	Differential I/O	
IP5+	C1	Differential I/O	
IP5-	B1	Differential I/O	
IP6+	A1	Differential I/O	
IP6-	A2	Differential I/O	
OP1+	H6	Differential I/O	Four high-speed differential pairs for DisplayPort, PCI Express, USB3 on connector side
OP1-	J6	Differential I/O	
OP2+	D6	Differential I/O	
OP2-	E6	Differential I/O	
OP3+	G6	Differential I/O	
OP3-	F6	Differential I/O	
OP4+	C6	Differential I/O	
OP4-	B6	Differential I/O	
IP7A	A3	I/O	Differential or Single ended signals on system side
IP7B	A4	I/O	
IP8A	B3	I/O	
IP8B	B4	I/O	
OP5A	A5	I/O	
OP5B	A6	I/O	
I2C_SCL	J4	Control IN	I2C slave address signal
I2C_SDA	H4	Control I/O	I2C slave data signal
SLV_ADDR1	H5	Control IN	Binary valued address selection pin for I2C slave address
SW_EN	J5	Control IN	Switch enable control input
VDD	B2, E3	Power	Supply pin

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
VDDIO	H3, E4	I/O power	I/O supply pin
GND	B5, D3, F3,F4, H2		Ground
SLV_ADDR2	D4	Control I/O	Binary valued address selection pin for I2C slave address

7. Functional description

CBTL08GP053 is a highly integrated Type-C switch targeting Type-C applications. All high speed signal paths are implemented using high-bandwidth pass-gate technology and are non-directional. The side band switches are designed to support 5.5 V tolerance. No clock or reset signal is needed for the multiplexer to function. The switching paths for all the switches can be selected using the I^2C-bus interface.

CBTL08GP053 functionality can be categorized under three portions:

- High speed switch
  - This has four sub networks of switches corresponding to four I/Os (OPx) connected to Type-C connector interface
  - Each sub network consist of a multiplexer of three high speed I/Os (IPx) on the system side interface
  - All switch paths handles differential signaling or 1.8 V rail to rail single ended signals
  - All switch paths support up to 10 Gbps signaling
  - All multiplexers I/Os are selectable through the I^2C-bus interface
  - The connector side I/Os can be put in Hi-Z through the I^2C-bus interface. Default for the I/O is Hi-Z
- Sideband Auxiliary crossbar switch
  - This has a 2:1 multiplexer followed by single ended selectable crossbar function
  - Switch handles both 3.3 V single ended and differential signals
  - Switch I/Os are 5.5 V tolerant
  - Switch handles 5 V rail to rail signaling
  - Crossbar function (normal or reversible) is selectable through the I^2C-bus interface
  - The connector side I/Os can be put in Hi-Z through the I^2C-bus interface. Default for the I/O is Hi-Z

At power on, all switches are in Hi-Z condition. After the host platform identifies Type-C interface (including Alternate mode support), it configures the switches. Each individual switch output can be selectively activated and specific switch paths can be selected. Each switch output can also remain in Hi-Z individually.

The SW_EN pin is used to enable or disable the switch paths only but the I2C register contents are not reset when SW_EN toggles LOW. When SW_EN is HIGH, the switches can be enabled and if it is LOW, the switches remain in Hi-Z condition irrespective of the register contents. This pin can toggle dynamically in real time in the application.

Table 4. Truth table for SW_EN and I2C register contents

SW_EN	SWITCH_EN SYS_CTRL[7]	I2C register settings	Switch output	Power consumption condition
LOW	0	Remain unchanged	Hi-Z	Standby
LOW	1	Remain unchanged	Hi-Z	Standby
HIGH	0	Remain unchanged	Hi-Z	Standby
HIGH	1	Remain unchanged	Output (based on register settings)	Active

7.1 CBTL08GP053 - Use case view

CBTL08GP053 is a versatile high performance switch with flexibility and programmability to route various signals on to Type-C connector interface. It is designed to work over a range of product categories, platform applications, use cases and usage modes. With its configurability, it can serve the needs of both general and custom applications.

The following subsections cover the use case illustrations of CBTL08GP053.

7.1.1 System application examples

7.1.1.1 CBTL08GP053 in Notebook/Ultrabook PC or Tablet - USB3, DP use

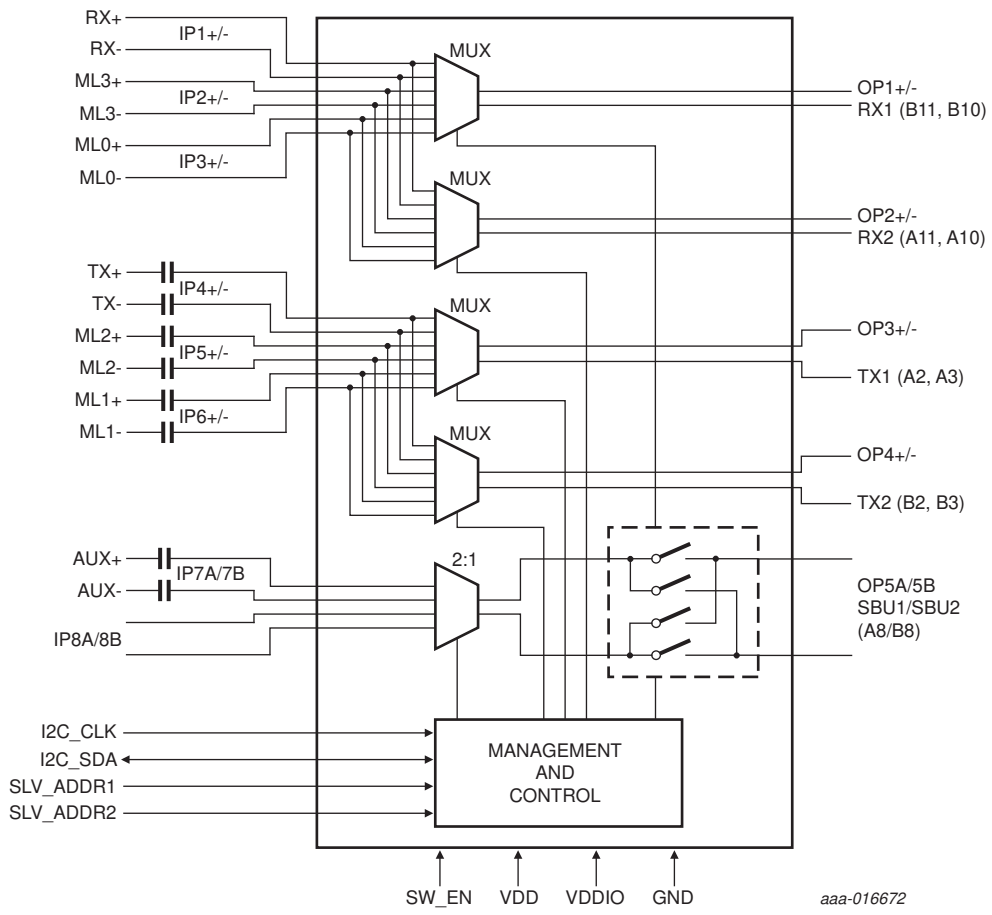


Fig 3. Illustrative diagram of USB3 and DP use case (Source case C, D, E and F support)

7.1.1.2 CBTL08GP053 in display monitor use case

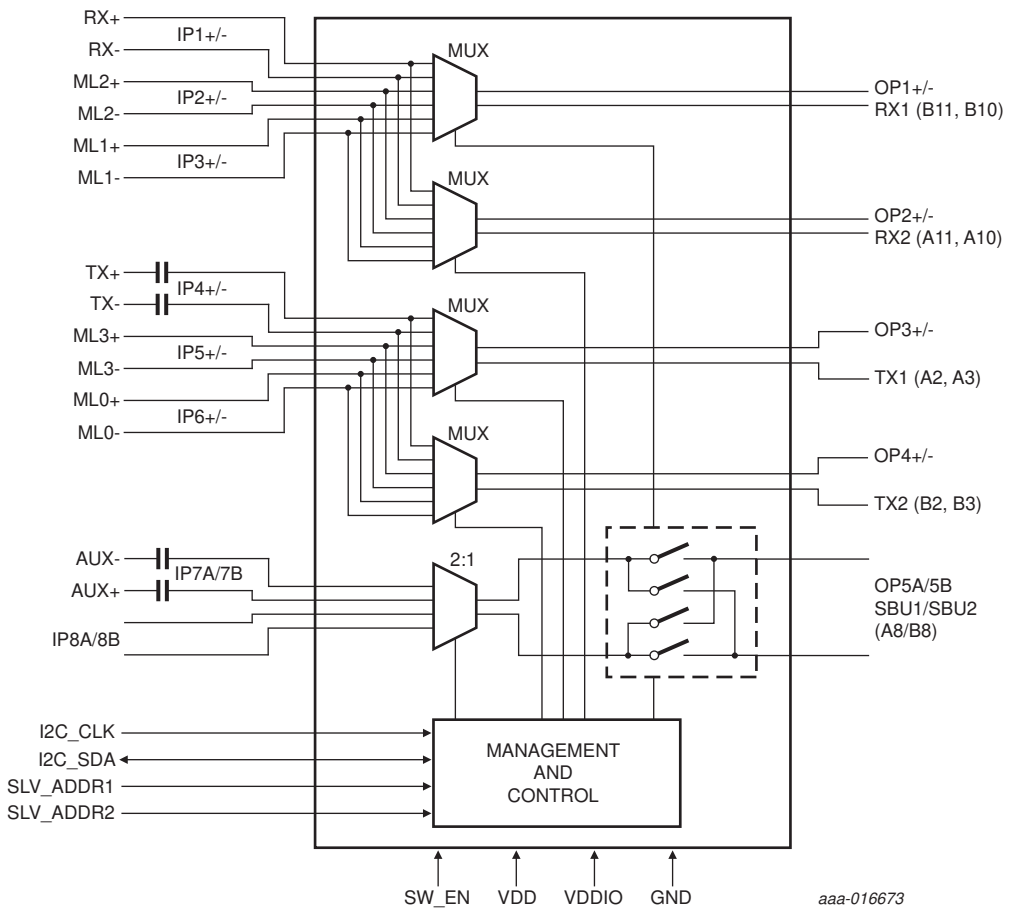


Fig 4. Illustrative diagram of USB3 and DP sink use case (Sink cases C and D support)

Other similar use cases can be constructed as well.

7.2 Host interface

The host interface of CBTL08GP053 consists of following data/control signals:

- SLV_ADDR1, SLV_ADDR2
- I2C_SCL
- I2C_SDA

CBTL08GP053 implements I^{2}C-bus slave interface and the host processor can issue commands, monitor status and receive response through this bus. A detailed description of the I^{2}C-bus specification, with applications, is given in UM10204, "I^{2}C-bus specification and user manual" [3]. It supports I^{2}C-bus data transfers in both Standard-mode (100kbit/s)) and Fast-mode (400 kbit/s).

As an exception to the I^{2}C-bus specification, CBTL08GP053 does not support the I^{2}C-bus "General Call" address (and therefore does not issue an Acknowledge), clock stretching, Software Reset command, nor 10-bit address.

The various registers, address offsets and bit definition, as defined in this section and subsections later.

Referring to I^{2}C-bus protocol, CBTL08GP053 positively acknowledges all 256 register offset addresses. CBTL08GP053 I^{2}C-bus interface implements a special "Auto-Increment" feature that facilitates higher throughput realization by the host system. With this feature, the address wraps back to 0x00 from 0xFF on continuous reads and writes.

CBTL08GP053 supports up to a maximum of four I^{2}C-bus slave address options. The address is selected through SLV_ADDR1 and SLV_ADDR2 pins. Table 5 shows the different I^{2}C-bus device address options selectable based on pin values.

Please refer to the *CBTL08GP053 Programming Guide* (AN11663) for more details.

Table 5. Device slave address

SLV_ADDR2	SLV_ADDR1	I^{2}C-bus device address
LOW	LOW	0x60/0x61
LOW	HIGH	0x64/0x65
HIGH	LOW	0x68/0x69
HIGH	HIGH	0x6C/0x6D

Table 6. Register bit map overview

Address	Register name	Access[1]	Default POR value	Bit							
				7	6	5	4	3	2	1	0
0x01	SYS_CTRL	RW	b'00000000	SWITCH_EN							
0x02	OP1 CTRL	RW	b'00000000						IP3	IP2	IP1
0x03	OP2 CTRL	RW	b'00000000						IP3	IP2	IP1
0x04	OP3 CTRL	RW	b'00000000			IP6	IP5	IP4			
0x05	OP4 CTRL	RW	b'00000000			IP6	IP5	IP4			
0x06	OP5 CTRL	RW	b'00000000	IP8	IP7						
0x07	CROSS5_ CTRL	RW	b'00000001							CROSS	PASS
0x08	SW_CTRL	W	b'00000000			X5_SET	OP5_SET	OP4_SET	OP3_SET	OP2_SET	OP1_SET
0x09	REVISION	R	b'10100000	REVISION ID							
0x0A to 0xFF	Reserved	-	b'XXXXXXXX	RESERVED							

[1] 'R' Read only register, 'W' Write only register, 'RW' Read/Write register

7.2.1 SYS_CTRL register

Table 7. SYS_CTRL register (address 0x01) bit description

Default: b'00000000

Bit	Symbol	Access	Value	Description
7	SWITCH_EN	R/W	1	CBTL08GP053 is in functional mode. The host shall write a '1' into this bit to put the device into functional mode.
			0	CBTL08GP053 is in Shutdown mode. After POR, the device enters and remains in shutdown mode. To put the device into shutdown mode, this host shall write a '0' into this register bit.
6:0	RESERVED	R/W	XXXXXXX	Reserved bit fields. Reads will be zeros and writes do not have any effect.

7.2.2 OP1_CTRL register

Table 8. OP1_CTRL register (address 0x02) bit description

Default: b'00000000

Bit	Symbol	Access	Value	Description
7:3	RESERVED	R/W	XXXXX	Reserved bit fields. Reads will be zeros and writes do not have any effect.
2	IP3	R/W	0	Switch inputs IP3+/- are not selected
			1	Switch inputs IP3+/- are selected for connection to OP1+/-
1	IP2	R/W	0	Switch inputs IP2+/- are not selected
			1	Switch inputs IP2+/- are selected for connection to OP1+/-
0	IP1	R/W	0	Switch inputs IP1+/- are not selected
			1	Switch inputs IP1+/- are selected for connection to OP1+/-

[1] The only valid bit values are b'XXXXX001, b'XXXXX010 and b'XXXXX100. Any other bit combination of LS 3 bits will result in Hi-Z at the outputs OP1+/-.

7.2.3 OP2_CTRL register

Table 9. OP2_CTRL register (address 0x03) bit description

Default: b'00000000

Bit	Symbol	Access	Value	Description
7:3	RESERVED	R/W	XX	Reserved bit fields. Reads will be zeros and writes do not have any effect.
2	IP3	R/W	0	Switch inputs IP3+/- are not selected
			1	Switch inputs IP3+/- are selected for connection to OP2+/-
1	IP2	R/W	0	Switch inputs IP2+/- are not selected
			1	Switch inputs IP2+/- are selected for connection to OP2+/-
0	IP1	R/W	0	Switch inputs IP1+/- are not selected
			1	Switch inputs IP1+/- are selected for connection to OP2+/-

[1] The only valid bit values are b'XXXXX001, b'XXXXX010 and b'XXXXX100. Any other bit combination of LS 3 bits will result in Hi-Z at the outputs OP2+/-.

7.2.4 OP3_CTRL register

Table 10. OP3_CTRL register (address 0x04) bit description

Default: b'00000000

Bit	Symbol	Access	Value	Description
7:6	RESERVED	R/W	XX	Reserved bit fields. Reads will be zeros and writes do not have any effect.
5	IP6	R/W	0	Switch inputs IP6+/- are not selected
			1	Switch inputs IP6+/- are selected for connection to OP3+/-
4	IP5	R/W	0	Switch inputs IP5+/- are not selected
			1	Switch inputs IP5+/- are selected for connection to OP3+/-
3	IP4	R/W	0	Switch inputs IP4+/- are not selected
			1	Switch inputs IP4+/- are selected for connection to OP3+/-
2:0	RESERVED	R/W	XX	Reserved bit fields. Reads will be zeros and writes do not have any effect.

[1] The only valid bit values are b'XX100XXX, b'XX010XXX and b'XX001XXX. Any other bit combination of 3 bits (5:3) will result in Hi-Z at the outputs OP3+/-.

7.2.5 OP4_CTRL register

Table 11. OP4_CTRL register (address 0x05) bit description

Default: b'00000000

Bit	Symbol	Access	Value	Description
7:6	RESERVED	R/W	XX	Reserved bit fields. Reads will be zeros and writes do not have any effect.
5	IP6	R/W	0	Switch inputs IP6+/- are not selected
			1	Switch inputs IP6+/- are selected for connection to OP4+/-
4	IP5	R/W	0	Switch inputs IP5+/- are not selected
			1	Switch inputs IP5+/- are selected for connection to OP4+/-
3	IP4	R/W	0	Switch inputs IP4+/- are not selected
			1	Switch inputs IP4+/- are selected for connection to OP4+/-
2:0	RESERVED	R/W	XXXX	Reserved bit fields. Reads will be zeros and writes do not have any effect.

[1] The only valid bit values are b'XX100XXX, b'XX010XXX and b'XX001XXX. Any other bit combination of 3 bits (5:3) will result in Hi-Z at the outputs OP4+/-.

7.2.6 OP5_CTRL register

Table 12. OP5_CTRL register (address 0x06) bit description

Default: b'00000000

Bit	Symbol	Access	Value	Description
7	IP8	R/W	0	Switch inputs IP8A/B are not selected
			1	Switch inputs IP8A/B are selected for connection to OP5A/B
6	IP7	R/W	0	Switch inputs IP7A/B are not selected
			1	Switch inputs IP7A/B are selected for connection to OP5A/B
5:0	RESERVED	R/W	XXXXX	Reserved bit fields. Reads will be zeros and writes do not have any effect.

[1] The only valid bit values are b'01XXXXXX and b'10XXXXXX. Any other bit combination of 2 bits (7:6) will result in Hi-Z at the outputs OP5A/B.

7.2.7 CROSS5_CTRL register

Table 13. CROSS5_CTRL register (address 0x07) bit description

Default: b'00000001

Bit	Symbol	Access	Value	Description
7:2	RESERVED	R/W	XXXXXX	Reserved bit fields. Reads will be zeros and writes do not have any effect.
1	CROSS	R/W	0	OP5A/B will be Hi-Z
			1	OP5B is connected to either IP7A or IP8A depending on OP5_CTRL register value OP5A is connected to either IP7B or IP8B depending on OP5_CTRL register value
0	PASS	R/W	0	OP5A/B will be Hi-Z
			1	OP5B is connected to either IP7B or IP8B depending on OP5_CTRL register value OP5A is connected to either IP7A or IP8A depending on OP5_CTRL register value

[1] The only valid bit field values are b'XXXXXX10 and b'XXXXXX01. The bit fields b'XXXXXX00 and b'XXXXXX11 will result in Hi-Z at the outputs OP5A/B.

7.2.8 SW_CTRL register

Table 14. SW_CTRL register (address 0x08) bit description

Default: b'00000000

Bit	Symbol	Access	Value	Description
7:6	RESERVED	R/W	XX	Reserved bit fields. Reads will be zeros and writes do not have any effect.
5	X5_SET	R/W	0	Prior output setting is unchanged
			1	CROSS5_CTRL register value is used to select passing through or crossing the inputs
4	OP5_SET	R/W	0	Prior output setting is unchanged
			1	OP5A/B is connected to one of the inputs based on OP5_CTRL register

Table 14. SW_CTRL register (address 0x08) bit description *…continued*

Default: b'00000000

Bit	Symbol	Access	Value	Description
3	OP4_SET	R/W	0	Prior output setting is unchanged
			1	OP4+/- is connected to one of the inputs based on OP4_CTRL register
2	OP3_SET	R/W	0	Prior output setting is unchanged
			1	OP3+/- is connected to one of the inputs based on OP3_CTRL register
1	OP2_SET	R/W	0	Prior output setting is unchanged
			1	OP2+/- is connected to one of the inputs based on OP2_CTRL register
0	OP1_SET	R/W	0	Prior output setting is unchanged
			1	OP1+/- is connected to one of the inputs based on OP1_CTRL register

7.2.9 REVISION register

Table 15. REVISION register (address 0x09) bit description

Default: b'10100000

Bit	Symbol	Access	Value	Description
7:0	REVISION ID	R	b'10100000	Revision ID A0 = First silicon version

7.3 I²C read and write sequence

An example of an I²C write and read sequence is shown in Figure 5.

Table 16. I²C slave address

Name	Size (bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave address	8	0	1	1	0	SLV_ADDR2	SLV_ADDR1	0	Write = 0 Read = 1

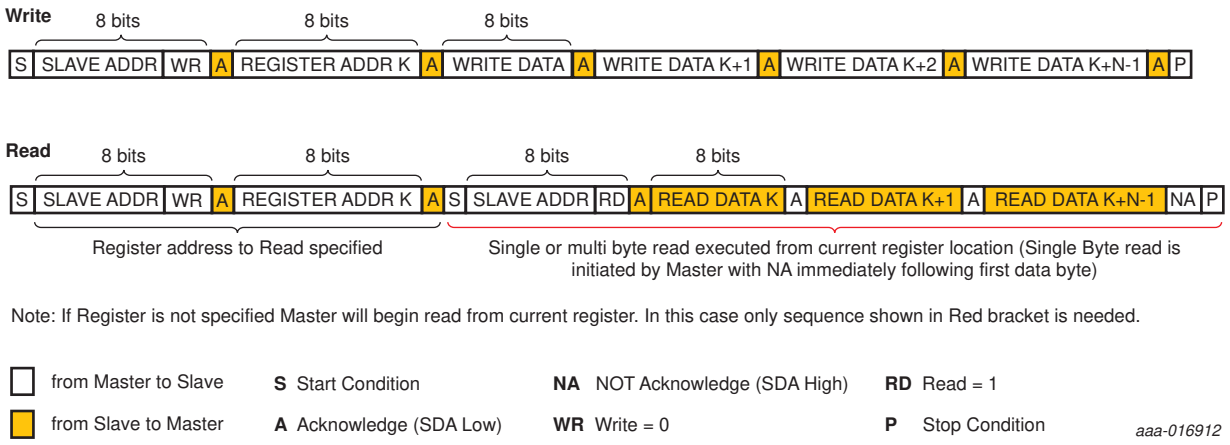


Fig 5. I²C write and read sequence

8. Limiting values

Table 17. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max[2]	Unit
V_{DD}	supply voltage	on pin VDD	−0.5	+4.6	V
$V_{DD(IO)}$	input/output supply voltage	on pin VDDIO	−0.5	+4.6	V
V_I	input voltage	IP1+/-, IP2+/-, IP3+/-, IP4+/-, IP5+/-, IP6+/-	−0.5	+2.6	V
		OP1+/-, OP2+/-, OP3+/-, OP4+/-	−0.5	+2.6	V
		IP7A/7B, IP8A/8B	−0.5	+6.0	V
		OP5A/5B	−0.5	+6.0	V
		SLV_ADDR1, SLV_ADDR2, SW_EN	−0.5	+4.6	V
		I2C_SCL, I2C_SDA (external pull-up needed on the I^2C-bus interface)	−0.5	+4.6	V
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature		−40	+125	°C
V_{ESD}	electrostatic discharge voltage	HBM[3]	2000	-	V
		CDM[4]	500	-	V

[1] All voltage values, except differential voltages, are with respect to network ground terminal.

[2] Stresses above the absolute maximum ratings may damage the device. The device may not function or be operating above the Recommended Operating Conditions and it is strongly recommended not to exceed these levels. Also, the device reliability may get affected if it is subjected to stress levels above the Recommended Operating Conditions.

[3] Human Body Model: ANSI/ESDA/JEDEC JDS-001-2012 (Revision of ANSI/ESDA/JEDEC JS-001-2011), ESDA/JEDEC Joint standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA; JEDEC Solid State Technology Association, Arlington, VA, USA.

[4] Charged Device Model: JESD22-C101E December 2009 (Revision of JESD22-C101D, October 2008), standard for ESD sensitivity testing, Charged Device Model - Component level; JEDEC Solid State Technology Association, Arlington, VA, USA.

9. Recommended operating conditions

Table 18. Operating conditions

Over ambient temperature and power supply ranges (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	on pin VDD	2.9	-	3.6	V
$V_{DD(IO)}$	input/output supply voltage	on pin VDDIO	1.7	-	3.6	V
T_{amb}	ambient temperature		−40	-	+105	°C

10. Characteristics

10.1 Device characteristics

Table 19. Device characteristics

Over ambient temperature and power supply ranges (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{act}	active current	switches are enabled	-	300	-	µA
I_{stdby}	standby current	all switches in Hi-Z	-	-	15	µA
$t_{startup}$	start-up time	SW_EN going LOW → HIGH to switches functioning as per specified operating characteristics; with a non-zero and valid switch selection (refer to Figure 6)	-	60	300	µs
t_{rcfg}	reconfiguration time	Time interval between end of I2C ACK response last bit and switches functioning as per specified operating characteristics	-	-	20	µs

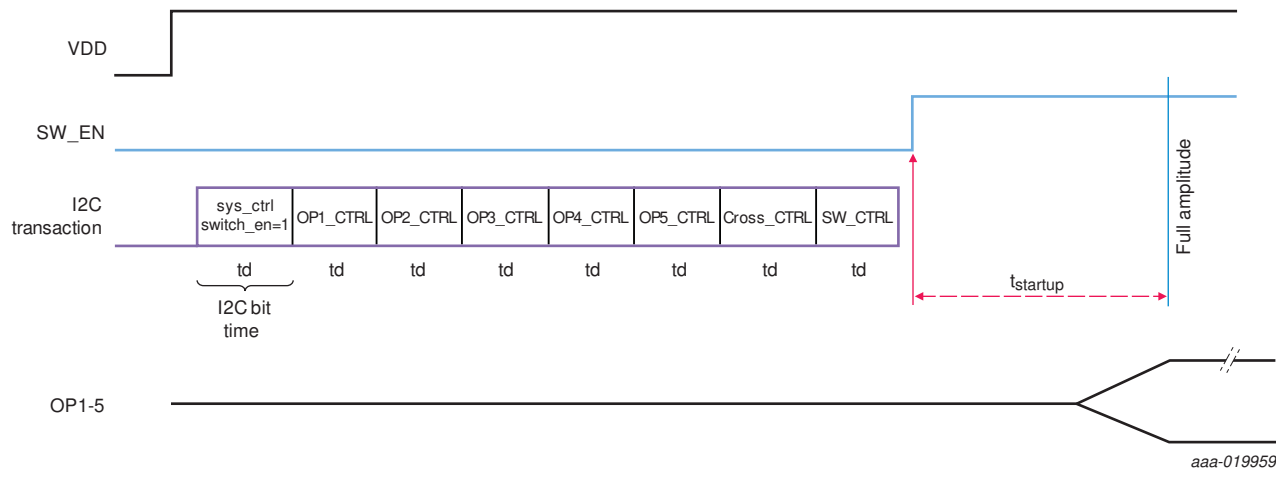


Fig 6. $t_{startup}$ timing

10.2 High speed switch characteristics

Table 20. High speed switch characteristics

Over ambient temperature and power supply ranges (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	input voltage		−0.3	-	+2.55	V
$V_{se,\ LO}$	Single ended voltage LOW level	Applicable for single ended signal switching use cases	-	-	$0.3 \times V_{DD(IO)}$	V
$V_{se,\ HI}$	Single ended voltage HIGH level	Applicable for single ended signal switching use cases	$0.7 \times V_{DD(IO)}$	-	2.55	V
$V_{se,pp\ swing}$	Single ended peak to peak voltage swing	Applicable for differential signal switching use cases	-	-	0.7	V
V_{cm}	Common mode voltage	Applicable for differential signal switching use cases	0	-	2.2	V
R_{on}	ON-state resistance	V_{cm} = 0 V to 2.2 V, I = 15 mA	-	7	10	Ω
I_{max}	Maximum sustained DC current flow		-	-	15	mA
t_{pd}	Propagation delay	At mid-point of differential voltage transition	-	80	120	ps
$t_{SK,diff}$	Intra pair skew	Between mid points of positive and negative terminals of an IO	-	-	6	ps
t_{SK}	Inter pair skew	Skew between different lanes	-	35	-	ps
BW	−3 dB Bandwidth		-	8.5	-	GHz
DDIL	Differential Insertion Loss on both IPx (x = 1 to 6) and OPy+/- (y = 1 to 4)	Switch path is disabled				
		f = 5.4 GHz	-	16.5	-	dB
		f = 2.7 GHz	-	23	-	dB
		Switch path is enabled				
		f = 5.4 GHz	-	1.8	-	dB
		f = 2.7 GHz	-	1.2	-	dB
		f = 1.35 GHz	-	0.9	-	dB
		f = 100 MHz	-	0.8	-	dB
DDRL	Differential return loss on IPx (x = 1 to 6)	f = 5.4 GHz	-	16	-	dB
		f = 2.7 GHz	-	20	-	dB
		f = 1.35 GHz	-	23	-	dB
DDRL	Differential return loss on OPx (x = 1 to 4)	f = 5.4 GHz	-	16	-	dB
		f = 2.7 GHz	-	20	-	dB
		f = 1.35 GHz	-	23	-	dB
DDXTLK	Differential Crosstalk on IPx+/- (x = 1 to 6)	f = 5.4 GHz	-	24	-	dB
		f = 2.7 GHz	-	32	-	dB
		f = 1.35 GHz	-	37	-	dB
DDXTLK	Differential crosstalk on OPx+/- (x = 1 to 4)	f = 5.4 GHz	-	24	-	dB
		f = 2.7 GHz	-	32	-	dB
		f = 1.35 GHz	-	37	-	dB

All S-parameter measurements are with respect to 100 Ω differential impedance reference and 50 Ω single-ended impedance reference.

10.3 Sideband Auxiliary Crossbar switch characteristics

Table 21. Sideband Auxiliary Crossbar switch characteristics

Over ambient temperature and power supply ranges (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	input voltage		−0.3	-	+5.3	V
$V_{se,\ LO}$	Single ended voltage LOW level	Applicable for single ended signal switching use cases	-	-	0.3 × $V_{DD(IO)}$	V
$V_{se,\ HI}$	Single ended voltage HIGH level	Applicable for single ended signal switching use cases	0.7 × $V_{DD(IO)}$	-	5.3	V
$V_{se,pp\ swing}$	Single ended peak to peak voltage swing (diff. signal switching use cases)	Up to 75 MHz	-	-	5.3	V
		75 MHz to 500 MHz	0.075	-	0.575	V
V_{cm}	Common mode voltage (diff. signal switching use cases)	Up to 75 MHz	0.8	-	2.65	V
		75 MHz to 500 MHz	−0.05	-	+0.5	V
R_{on}	ON-state resistance	V_{cm} = −0.05 V to 2.65 V, I = 20 mA	-	7.1	10	Ω
I_{max}	Maximum sustained DC current flow		-	-	20	mA
t_{pd}	Propagation delay	At mid-point of differential voltage transition	-	80	100	ps
t_{SK}	Intra pair skew		-	-	5	ps
BW	−3 dB bandwidth		-	750	-	MHz
DDDIL	Differential Insertion Loss	Switch path is not enabled				
		f = 500 MHz	-	20	-	dB
		f = 250 MHz	-	26	-	dB
		Switch path is enabled				
		f = 750 MHz	-	3.0	-	dB
		f = 500 MHz	-	1.5	-	dB
		f = 375 MHz	-	1.2	-	dB
		f = 250 MHz	-	1.0	-	dB
DDRL	Differential return loss	f = 500 MHz	-	11	-	dB
		f = 375 MHz	-	13	-	dB
		f = 250 MHz	-	16	-	dB

All S-parameter measurements are with respect to 100 Ω differential impedance reference and 50 Ω single-ended impedance reference.

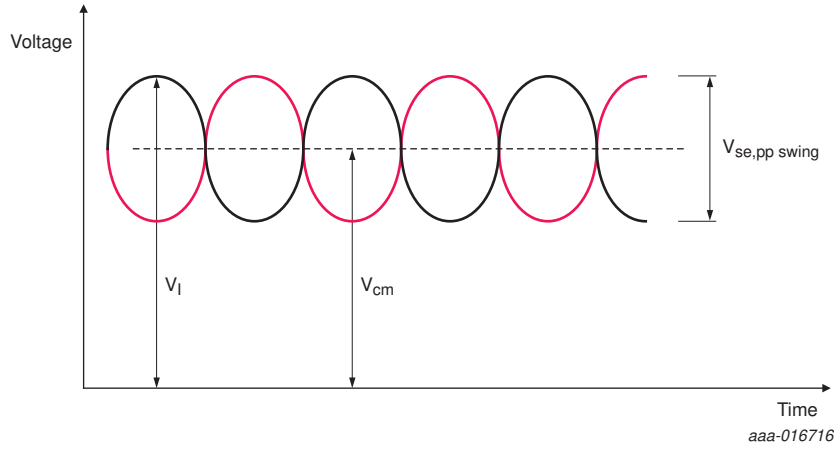


Fig 7. Illustrative diagram of voltage definitions of high speed and sideband auxiliary

10.4 Control I/O characteristics

Table 22. Control I/O characteristics

Over ambient temperature and power supply ranges (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
System side CMOS interface pins (SW_EN, SLV_ADDR1, SLV_ADDR2)						
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DD(IO)}$	-	$V_{DD(IO)}$ + 0.3	V
V_{IL}	LOW-level input voltage		-	-	$0.3 \times V_{DD(IO)}$	V
I_{IL}	Input leakage current	For input levels (LOW, HIGH)	−10	-	+10	µA
C_I	Capacitance of pin		-	-	10	pF
System side open drain interface pins (I2C_SCL, I2C_SDA); pulled up externally to $V_{DD(IO)}$[1] through resistor						
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DD(IO)}$	-	$V_{DD(IO)}$ + 0.3	V
V_{IL}	LOW-level input voltage		-	-	$0.3 \times V_{DD(IO)}$	V
V_{OL}	LOW-level output voltage at 3 mA sink current	$V_{DD(IO)} > 2$ V	0	-	0.4	V
		$V_{DD(IO)} < 2$ V	0	-	$0.2 \times V_{DD(IO)}$	V
I_{IL}	LOW-level input current	Pin voltage: $0.1 \times V_{DD(IO)}$ to $0.9 \times V_{IO}$,max	−10	-	+10	µA
C_I	capacitance of I/O pin		-	-	10	pF

[1] $V_{DD(IO)}$ is pull-up voltage on I^2C-bus interface and the pull-up resistors are sized for 3 mA. It can be different from V_{DD}. Note this is not a chip level power supply.

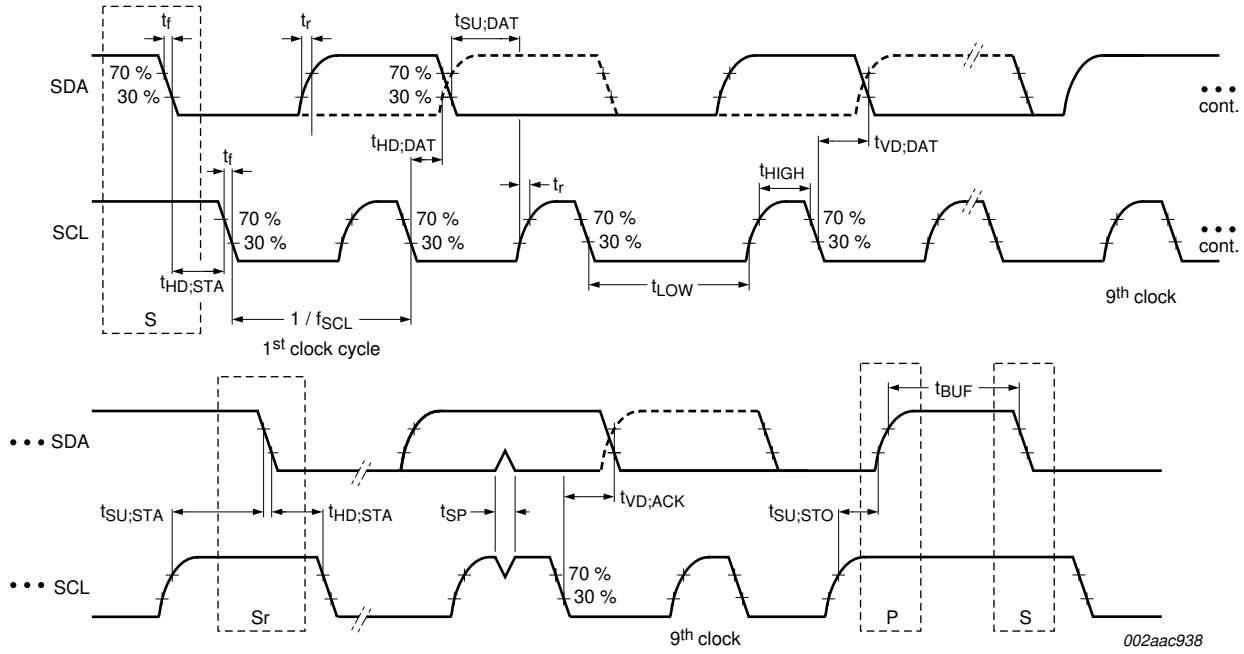
10.5 I²C-bus dynamic characteristics

Table 23. I²C-bus dynamic characteristics

Over ambient temperature and power supply ranges (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency		-	-	400	kHz
$t_{HD;STA}$	hold time (repeated) START condition	Fast mode; after this period, the first clock pulse is generated	0.6	-	-	µs
t_{LOW}	LOW period of the SCL clock	Fast mode	1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock	Fast mode	0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition	Fast mode	0.6	-	-	µs
$t_{HD;DAT}$	data hold time	Fast mode	0	-	-	µs
$t_{SU;DAT}$	data set-up time	Fast mode	100	-	-	ns
t_r	rise time of both SDA and SCL signals		$20 + 0.1 \times C_B$[1]	-	300	ns
t_f	fall time of both SDA and SCL signals		$20 + 0.1 \times C_B$[1]	-	300	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	µs
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	µs
$t_{VD;DAT}$	data valid time		-	-	0.9	µs
$t_{VD;ACK}$	data valid acknowledge time		-	-	0.9	µs
t_{SP}	pulse width of spikes that must be suppressed by input filter		0	-	50	µs

[1] C_B = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times according to Table 6 of [3] are allowed



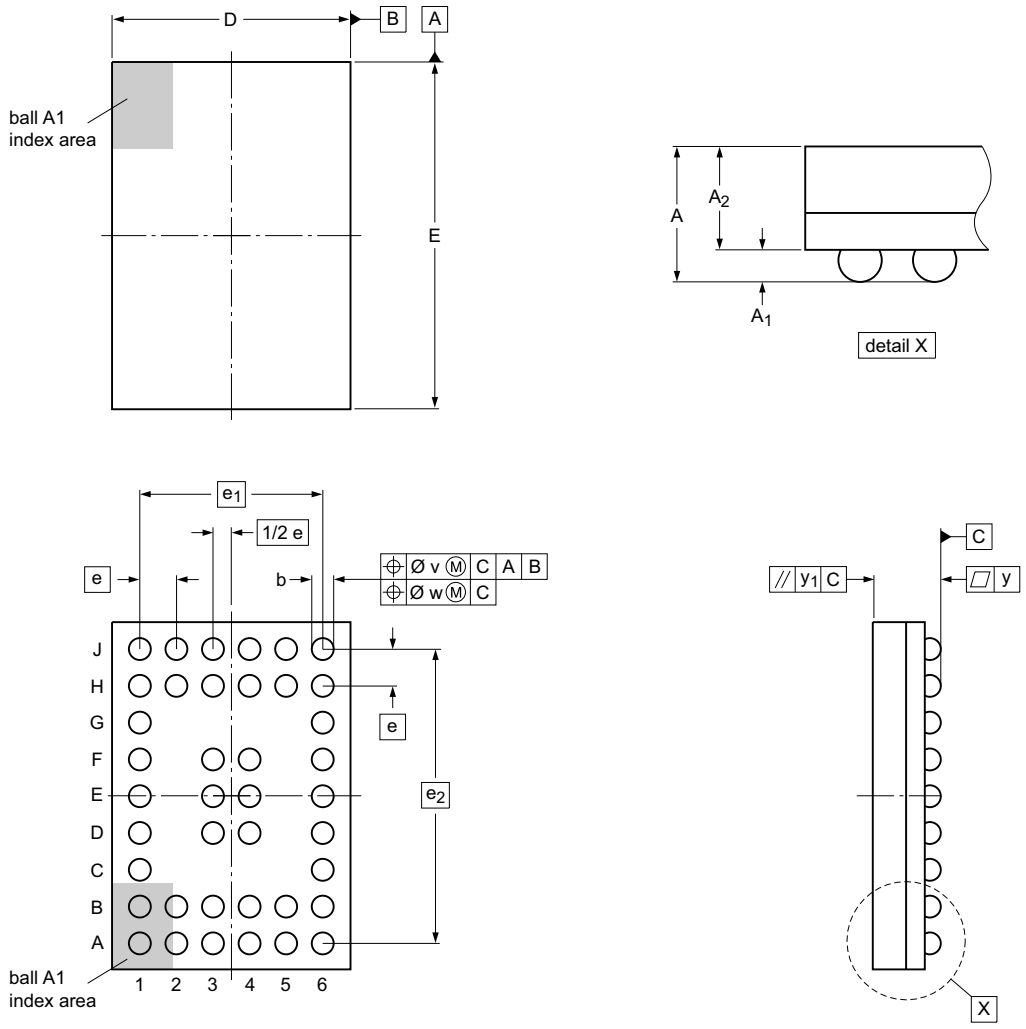
$V_{IL} = 0.3V_{DD(IO)}$

$V_{IH} = 0.7V_{DD(IO)}$

Fig 8. Definition of timing for F/S-mode devices on the I²C-bus

11. Package outline

VFBGA40: plastic very thin fine-pitch ball grid array package; 40 balls **SOT1439-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	0.99	0.26	0.76	0.33	3.35	4.85	0.5	2.5	4.0	0.15	0.05	0.08	0.15
	nom	0.95	0.21	0.71	0.30	3.25	4.75							
	min	0.85	0.16	0.66	0.25	3.15	4.65							

sot1439-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1439-1						~~15-02-09~~ 15-04-02

Fig 9. Package outline SOT1439-1 (VFBGA40)