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CBTV4020

20-bit DDR SDRAM 2 : 1 MUX

Rev. 03 — 4 April 2008 Product data sheet

1. General description

This 20-bit bus switch is designed for 2.3 V to 2.7 V V_{DD} operation and SSTL_2 select input levels.

Each host port pin is multiplexed to one of two DIMM port pins. When the SEL pin is HIGH the A DIMM port is turned on and the B DIMM port is off. The ON-state connects the host port to the DIMM port through a 20 Ω nominal series resistance. When the port is off a high-impedance state exists between the Host and disabled DIMM. The DIMM port is terminated with a 100 Ω resistor to ground. When the SEL pin is LOW the B DIMM port is turned on and the A DIMM port is off.

The part incorporates a very low crosstalk design. It has a very low skew between outputs (< 50 ps) and low skew (< 50 ps) for rising and falling edges. The part has optimal performance in DDR data bus applications.

Each switch has been optimized for connection to 1-bank or 2-bank DIMMs.

The low internal RC time constant of the switch (20 Ω × 7 pF) allows data transfer to be made with minimal propagation delay.

The CBTV4020 is characterized for operation from 0 °C to +85 °C.

2. Features

- SEL signal is SSTL_2 compatible
- Optimized for use in Double Data Rate (DDR) SDRAM applications
- Designed to be used with 400 Mbit/s 200 MHz DDR data bus
- Switch ON resistance is designed to eliminate the need for series resistor to DDR SDRAM
- R_{ON} ~ 20 Ω
- Internal 100 Ω pull-down resistors on DIMM side when path is disabled
- Low differential skew
- Matched rise/fall slew rate
- Low crosstalk
- One DIMM select control line
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 1500 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay	from input DHn or DAn/DBn to output DAn/DBn or DHn	[1]	-	140	-	ps
C_{in}	control pin capacitance	V_I = 2.5 V or 0 V	[2]	-	4	-	pF
C_{on}	switch on capacitance	V_I = 1.5 V	[2]	-	-	10	pF

[1] The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance); 20 Ω × 7 pF. Load capacitance = 7 pF. This parameter is not production tested.

[2] Capacitance values are measured at 10 MHz and a bias voltage 3 V. Capacitance is not production tested.

4. Ordering information

Table 2. Ordering information

T_{amb} = 0 °C to +85 °C

Type number	Package		
	Name	Description	Version
CBTV4020EE/G	TFBGA72	plastic thin fine-pitch ball grid array package; 72 balls; body 6 × 6 × 0.8 mm	SOT761-1

5. Functional diagram

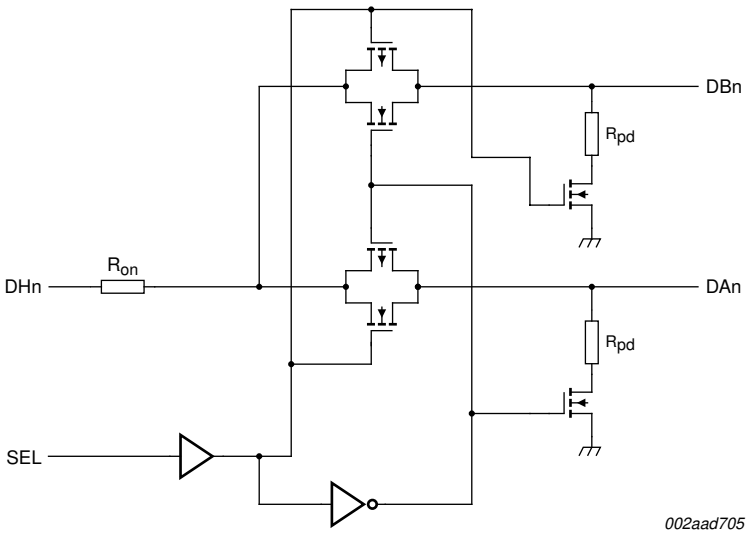
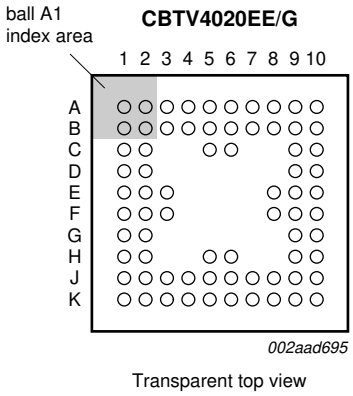


Fig 1. Logic diagram (positive logic)

6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration for TFBGA72

	1	2	3	4	5	6	7	8	9	10
A	DB17	DA17	DB16	DB15	DA15	DB14	DA14	DA13	DB12	DA12
B	DA18	DH17	DH16	DA16	DH15	DH14	DB13	DH13	DH12	DB11
C	DB18	DH18			GND	GND			DH11	DA11
D	DA19	GND							GND	DB10
E	DB19	DH19	SEL					V_{DD}	DH10	DA10
F	DA0	DH0	V_{DD}					V_{DD}	DH9	DB9
G	DB0	GND							GND	DA9
H	DA1	DH1			GND	GND			DH8	DB8
J	DB1	DH2	DH3	DB3	DH4	DH5	DA6	DH6	DH7	DA8
K	DA2	DB2	DA3	DA4	DB4	DA5	DB5	DB6	DA7	DB7

002aad696

Transparent top view.

Empty cell indicates no ball present at that location.

Fig 3. TFBGA72 ball mapping

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
DH0	F2	host ports
DH1	H2	
DH2	J2	
DH3	J3	
DH4	J5	
DH5	J6	
DH6	J8	
DH7	J9	
DH8	H9	
DH9	F9	
DH10	E9	
DH11	C9	
DH12	B9	
DH13	B8	
DH14	B6	
DH15	B5	
DH16	B3	
DH17	B2	
DH18	C2	
DH19	E2	
SEL	E3	select
GND	C5, C6, D2, D9, G2, G9, H5, H6	ground
V_{DD}	E8, F3, F8	positive supply voltage
DA0	F1	A DIMM ports
DA1	H1	
DA2	K1	
DA3	K3	
DA4	K4	
DA5	K6	
DA6	J7	
DA7	K9	
DA8	J10	
DA9	G10	
DA10	E10	
DA11	C10	
DA12	A10	
DA13	A8	
DA14	A7	
DA15	A5	

Table 3. Pin description *...continued*

Symbol	Pin	Description
DA16	B4	A DIMM ports (continued)
DA17	A2	
DA18	B1	
DA19	D1	
DB0	G1	B DIMM ports
DB1	J1	
DB2	K2	
DB3	J4	
DB4	K5	
DB5	K7	
DB6	K8	
DB7	K10	
DB8	H10	
DB9	F10	
DB10	D10	
DB11	B10	
DB12	A9	
DB13	B7	
DB14	A6	
DB15	A4	
DB16	A3	
DB17	A1	
DB18	C1	
DB19	E1	

7. Functional description

Refer to Figure 1 “Logic diagram (positive logic)”.

7.1 Function selection

Table 4. Function selection

H = HIGH voltage level; L = LOW voltage level.

Input SEL	Function
L	host port = B DIMM port A DIMM port = 100 Ω to GND
H	host port = A DIMM port B DIMM port = 100 Ω to GND

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
The package thermal impedance is calculated in accordance with JESD 51.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+3.3	V
I_{IK}	input clamping current	$V_{I/O}$ < 0 V		−50	-	mA
V_I	input voltage	SEL pin only	[1]	−0.3	V_{DD} + 0.3	V
		except SEL pin	[1]	−0.5	+3.3	V
T_{stg}	Storage temperature			−65	+150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamping current ratings are observed.

9. Recommended operating conditions

Table 6. Operating conditions

All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		2.3	2.5	2.7	V
V_{IH}	HIGH-level input voltage	DIMM port and host (SEL)	1.6	-	-	V
V_{IL}	LOW-level input voltage	DIMM port and host (SEL)	-	-	0.9	V
T_{amb}	ambient temperature	operating in free air	0	-	85	°C

10. Static characteristics

Table 7. Static characteristics

T_{amb} = 0 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IK}	input clamping current	V_{DD} = 2.3 V; I_I = −18 mA		-	-	−1.2	V
I_{LI}	input leakage current	V_{DD} = 2.5 V; V_I = V_{DD} or GND; SEL = GND or V_{DD}					
		SEL		-	-	±100	µA
		host port	[2]	-	-	±100	µA
		SEL = GND for I_{IL} (test)					
		DIMM port	[2]	-	-	±100	µA
I_{DD}	supply current	V_{DD} = 2.5 V; I_O = 0 mA; V_I = V_{DD} or GND		-	55	150	µA
I_{OL}	LOW-level output current	on DBn or DAn; V_{OL} = 1 V	[3]	-	9.5	-	mA
C_{in}	control pin capacitance	V_I = 2.5 V or 0 V	[4]	-	4	-	pF
C_{on}	switch on capacitance	V_I = 1.5 V	[4]	-	-	10	pF
R_{ON}	ON resistance	V_{DD} = 2.5 V; V_A = 0.8 V; V_B = 1.0 V	[5]	16	20	30	Ω
		V_{DD} = 2.5 V; V_A = 1.7 V; V_B = 1.5 V	[5]	16	20	30	Ω
R_{pd}	pull-down resistance	output; DAn (SEL = GND) or DBn (SEL = V_{DD}) = 0.5V_{DD}	[3]	-	105	-	Ω

[1] All typical values are at V_{DD} = 2.5 V, T_{amb} = 25 °C.

[2] When SEL is HIGH, DBn must be open and DAn can be HIGH or LOW. When SEL is LOW, DAn must be open and DBn can be HIGH or LOW.

[3] SEL = GND for testing DAn, and SEL = V_{DD} for testing DBn.

[4] Capacitance values are measured at 10 MHz and a bias voltage 3 V. Capacitance is not production tested.

[5] Measured by the current between the host and the DIMM terminals at the indicated voltages on each side of the switch.

11. Dynamic characteristics

Table 8. Dynamic characteristics

V_{DD} = 2.5 V ± 0.2 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay	from input DHn or DAn/DBn to output DAn/DBn or DHn	[1]	-	140	-	ps
t_{en}	enable time	from input SEL to output DAn/DBn or DHn		1	-	2	ns
t_{dis}	disable time	from input SEL to output DAn/DBn or DHn		1	-	3	ns
$t_{sk(o)}$	output skew time	any output to any output; Figure 7	[2]	-	25	50	ps
$t_{sk(edge)}$	edge skew time	difference of rising edge propagation delay and falling edge propagation delay; Figure 8	[2]	-	25	50	ps

[1] The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance); 20 Ω × 7 pF. Load capacitance = 7 pF. This parameter is not production tested.

[2] Skew is not production tested.

11.1 DHn to DAn/DBn AC waveforms

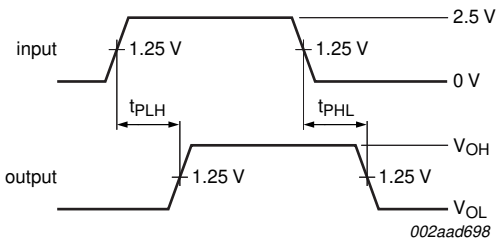
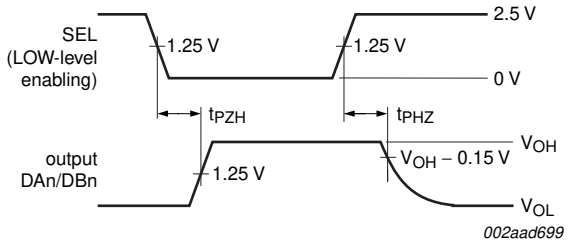


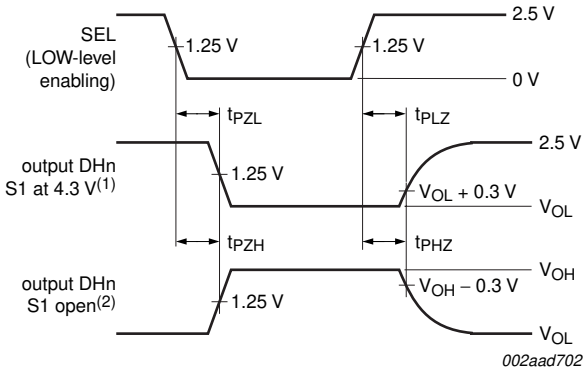
Fig 4. Input to output propagation delays



The output is HIGH except when disabled by the SEL control.

Fig 5. Output enable and disable times

11.2 DAn/DBn to DHn AC waveforms



(1) The output is LOW except when disabled by the SEL control.

(2) The output is HIGH except when disabled by the SEL control.

Fig 6. Output enable and disable times

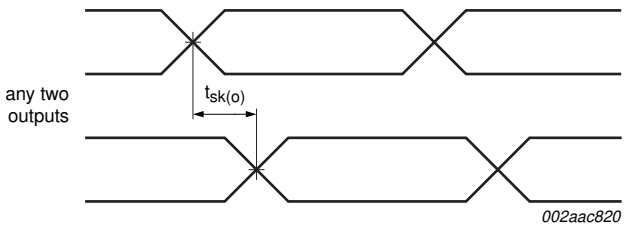


Fig 7. Skew between any two outputs

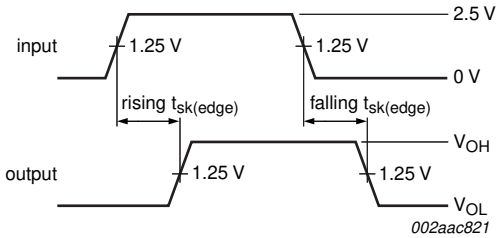


Fig 8. Rising and falling edge skew

12. Test information

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns.

The outputs are measured one at a time with one transition per measurement.

C_L = load capacitance; includes jig and probe capacitance.

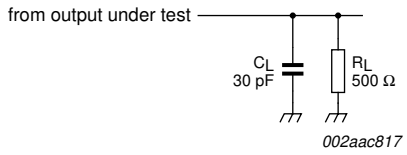
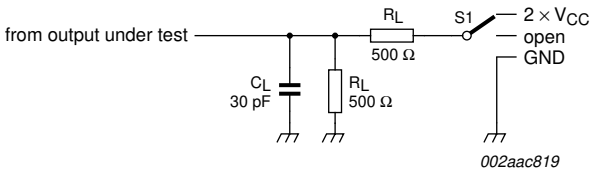


Fig 9. Test circuit, DHn to DAn/DBn



Test data are given in Table 9.

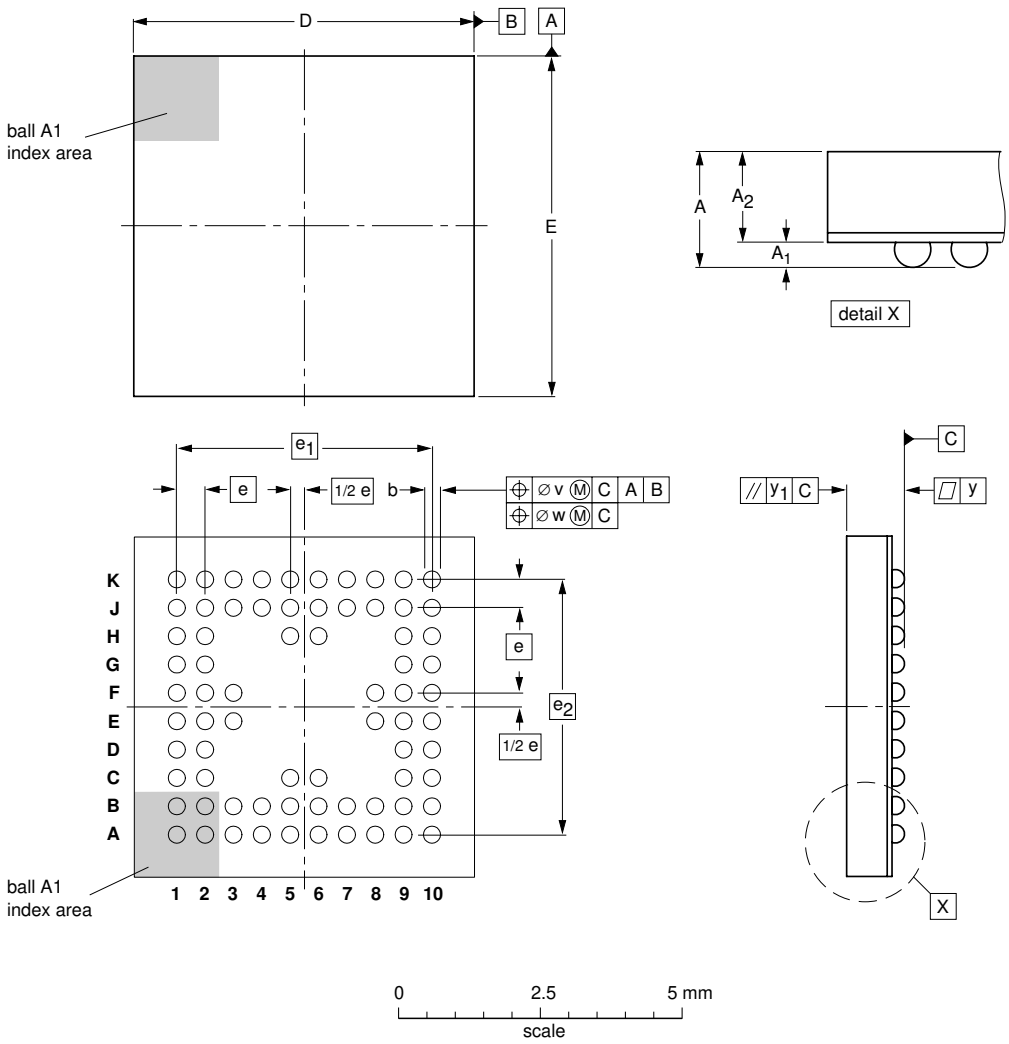
Fig 10. Test circuit, DAn/DBn to DHn

Table 9. Test data

Test	Load		Switch S1
	C_L	R_L	
t_{PD}	30 pF	500 Ω	open
t_{PLZ}, t_{PZL}	30 pF	500 Ω	2 × V_{CC}
t_{PHZ}, t_{PZH}	30 pF	500 Ω	GND

13. Package outline

TFBGA72: plastic thin fine-pitch ball grid array package; 72 balls; body 6 x 6 x 0.8 mm **SOT761-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.1	0.25 0.15	0.85 0.75	0.35 0.25	6.1 5.9	6.1 5.9	0.5	4.5	4.5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT761-1	- - -	MO-195	- - -			02-04-10

Fig 11. Package outline SOT761-1 (TFBGA72)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 12) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

Table 10. SnPb eutectic process (from J-STD-020C)

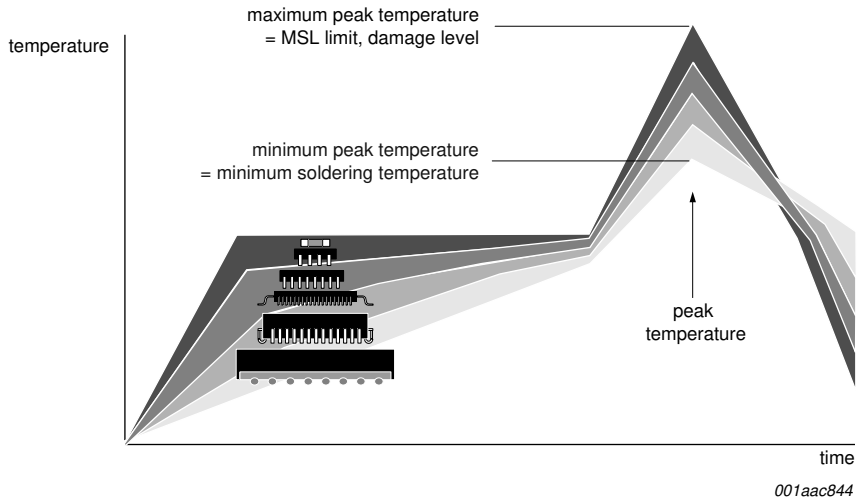
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 12.



MSL: Moisture Sensitivity Level

Fig 12. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DDR	Double Data Rate
DIMM	Dual In-Line Memory Module
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PRR	Pulse Repetition Rate
RC	Resistor-Capacitor network
SDRAM	Synchronous Dynamic Random Access Memory
SSTL_2	Stub Series Terminated Logic for 2.5 V

16. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTV4020_3	20080404	Product data sheet	-	CBTV4020_N_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 2 “Features”: – 5th bullet item: changed “r_{on}” to “R_{ON}” – 9th bullet item: changed from “Low cross-talk data-data/data-DQM” to “Low crosstalk” • Section 3 “Quick reference data” re-written (rows are now direct copies from Table 7 “Static characteristics” and Table 8 “Dynamic characteristics”) • Table 2 “Ordering information”: deleted type number CBTV4020EE • Added Figure 2 “Pin configuration for TFBGA72” • Table 3 “Pin description”: expanded to detail pin assignments • Table 5 “Limiting values”: – deleted (old) Table note [1] (this statement now given in Section 17.3 “Disclaimers”) – under conditions for V_I: changed “$\overline{S}$ pin” to “SEL pin” – separated Min and Max values • Table 7 “Static characteristics”: – changed symbol for “input leakage current” from “I_I” to “I_{LI}” – changed symbol from “r_{on}” to “R_{ON}” – changed symbol from “r_{pd}” to “R_{pd}” – under Conditions for R_{pd}, changed “An” to “DAn” and changed “Bn” to “DBn” • Table 8 “Dynamic characteristics”: – changed symbol from “t_{pd}” to “t_{PD}” – changed symbol from “t_{osk}” to “$t_{sk(o)}$” – changed symbol from “t_{esk}” to “$t_{sk(edge)}$” • added information on soldering SMD packages • added Section 15 “Abbreviations”			
CBTV4020_N_2 (9397 750 13594)	20060515	Product data sheet	-	CBTV4020_N_1
CBTV4020_N_1 (9397 750 10411)	20020927	Product data	ECN 853-2387 28989 of 2002 Sep 26	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contents

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