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ConnectCore™ 9P 9360 Hardware Reference

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Contents

Using this Guide

This guide provides information about the Digi ConnectCore 9P 9360 embedded core module.

Conventions used in this guide

This table describes the typographic conventions used in this guide:

This convention	Is used for
italic type	Emphasis, new terms, variables, and document titles.
monospaced type	Filenames, pathnames, and code examples.

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Documentation updates

Please always chech the product specific section on the Digi support website for the most current revision of this document: www.digiembedded.com/support.

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Change Log

1. Added change log.
2. Revised website address in contact information table.
3. Revised documentation updates section.
4. Removed specific OS reference from the Using This Guide chapter.
5. Corrected document title, footer, and all other mentions of the product name to read ConnectCore 9P 9360, rather than ConnectCore 9P.
6. Improved the module top view image within the Module Specifications section of Appendix A to make the pinout information clear.
7. Corrected typo of pin GPIO32 within the Multiplexed GPIO Pins table and typo of external interrupt EIRQ0 in the External Interrupts section.

About the Module

CHAPTER 1

The ConnectCore 9P 9360 is part of the ConnectCore embedded core processor module family. Built on leading NetSilicon® 32-bit NET+ARM technology, the network-enabled ConnectCore 9P family provides a modular and scalable core processor solution that significantly minimizes hardware and software design risk. This module combines superior performance and a complete set of integrated peripherals and component connectivity options in a compact and versatile form factor.

The ConnectCore 9P 9360 embedded module offers up to 128 MB RAM and 128 MB NAND flash, an integrated 10/100 Mb Ethernet MAC/PHY, up to four configurable UART/SPI ports, an online I^2C bus software interface, 73 shared GPIO ports for application-specific use, and an external 18-bit address/32-bit data bus interface for added component integration flexibility.

The ConnectCore 9P 9360 processor contains the NS9360 microprocessor. For information about the NS9360, see the *NS9360 Hardware Reference* available through your Jump Start kit.

Features and functionality

- 32-bit NET+ARM (ARM926EJ-S) RISC processor NS9750 @ 177MHz or 155MHz
- Up to 128 MB NAND Flash and 128 MB SD RAM
- 8 general purpose timers/counters or 4 PWM functions
- Up to 73 GPIO port options
- ARM9 core with memory management unit (MMU)

- Two 120-pin connectors
- Up to four RS232 serial interfaces with UART and SPI mode
- Integrated USB 2.0 compliant Host/Device interface
- Integrated 10/100Mbps Ethernet MAC/PHY
- I^2C interface, 100KHz and 400KHz
- On-board JTAG interface

Module variations

The ConnectCore 9P 9360 module is currently available in these standard variations:

- CPU speed 177MHz, 16MB SDRAM, 32MB NAND flash, 8KB SPI boot EEPROM, 8KB I^2C EEPROM, RTC, 0° C min / 70° C max
- CPU speed 177MHz, 32MB SDRAM, 32MB NAND flash, 8KB SPI boot EEPROM, 8KB I^2C EEPROM, RTC, 0° C min / 70° C max
- CPU speed 177MHz, 64MB SDRAM, 64MB NAND flash, 8KB SPI boot EEPROM, 8KB I^2C EEPROM, RTC, 0° C min / 70° C max
- CPU speed 177MHz, 128MB SDRAM, 128MB NAND flash, 8KB SPI boot EEPROM, 8KB i^2C EEPROM, RTC, 0° C min / 70° C max
- CPU speed 155MHz, 32MB SDRAM, 32MB NAND flash, 8KB SPI boot EEPROM, 8KB I^2C EEPROM, RTC, -40° C min / 85° C max

Module pinout

The module has two 120 pole connectors, X1 and X2. The next tables describe each pin, its properties, and its use on the development board.

Pinout legend: Type

I	Input
O	Output
I/O	Input or output
P	Power

Pinout legend: RESET state

PUW	Weak pullup to switched 3.3V in CPU on module
PU10	Pull up 10K to switched 3.3V on module

Pinout legend: Other values

- **dup:** Some signals are multiplexed to two (or more) different GPIO pins, to maximize the number of possible applications. Duplicate signals are indicated by *(dup)* after the signal name. Using the primary pin and the duplicate pin for the same function is not recommended.
- **SW:** Indicates GPIO pins that have their external signal path switched off when RESET# is asserted. The format used is *GPIOSWnn*.
- **#:** Indicates that this signal is active low.

X1 Connector

Pin	Signal	Type	BootStrap (BS) / System / Other	UART	SPI	I2C	DMA	LCD	IEEE 1284	PWM / Timer / IRQ	Notes Reset state
1	GND	P									Common GND return
2	RSTIN#	I									PU10
3	PWRGOOD	I/O									
4	RSTOUT#	O									
5	TCK	I	JTAG								PU10
6	TMS	I	JTAG								PU10
7	TDI	I	JTAG								PU10
8	TDO	O	JTAG								PU10
9	TRST#	I	JTAG								PU10
10	CONF0 / DEBUGEN#	I									PU10 Debug enable 0 = Debug enabled, TRST# isolated from SRST#
11	CONF1 / NAND_ FWP#	I									PU10 NAND Flash write protect 0 = NAND Flash write protected
12	CONF2 / OCD_EN#	I									PU10 Enables OCD mode; use with CONF0 Pullup 10K to +3.3V on module
13	CONF3 / not used	I									Not connected
14	CONF4 GPIO38, 2K2 series	I/O	BIT28 GEN_ID								PU10
15	CONF5 GPIO39, 2K2 series	I/O	Bit29 GEN_ID								PU10
16	CONF6 GPIO40, 2K2 series	I/O	Bit30 GEN_ID								PU10

Pin	Signal	Type	BootStrap (BS) / System / Other	UART	SPI	I2C	DMA	LCD	IEEE 1284	PWM / Timer / IRQ	Notes Reset state
17	CONF7 GPIO41, 2K2 series	I/O	Bit31 GEN_ID								PU10
18	GPIOSW8	I/O		TXDA	SPIA_ DO						PU10
19	GPIO09	I/O		RXDA	SPIA_DI						PUW
20	GPIOSW10	I/O		RTSA#						PWM0 (dup)	PU10
21	GPIO11	I/O		CTSA#						EIRQ2 (dup) Timer 0 (dup)	PUW
22	GPIOSW12	I/O		DTRA#						PWM1 (dup)	PU10
23	GPIO13	I/O		DSRA#						EIRQ0 (dup) PWM2 (dup)	PU10
24	GPIOSW00	I/O		TXDB	SPIB_ DO		DMA0_ DONE (dup)			Timer1 (dup)	PU10
25	GPIO01	I/O		RXDB	SPIB_DI		DMA0_ REQ (dup)			EIRQ0	PUW
26	GPIOSW02	I/O		RTSB#			DMA1_ ACK			Timer0	PU10
27	GPIO03	I/O		CTSB#			DMA0_ REQ#		ACK#		PUW
28	GPIOSW04	I/O		DTRB#			DMA0_ DONE		BUSY		PU10
29	GPIO05	I/O		DSRB#			DMA0_ ACK		ERR		PUW
30	GPIO06	I/O		RIB#	SPIB_ CLK				P_JAM	Timer7 (dup)	PUW
31	GPIO07	I/O		DCDB#	SPIB_ EN#		DMA0_ ACK (dup)			EIRQ1	PUW
32	GPIO72	I/O	WAIT#								
33	GPIO68	I/O	A24 MCKE_0							EIRQ0 (dup)	
34	GPIO69	I/O	A25 MCKE_1							EIRQ1 (dup)	
35	No connect										Reserved for A26
36	No connect										Reserved for A27
37	GPIOSW24	I/O		DTRD#				LCDD0			PUW
38	GPIO25	I/O		DSRD#				LCDD1			PUW
39	GND	P									
40	GPIO26	I/O		RID#	SPID_ CLK			LCDD2		Timer3	PUW

Pin	Signal	Type	BootStrap (BS) / System / Other	UART	SPI	I2C	DMA	LCD	IEEE 1284	PWM / Timer / IRQ	Notes Reset state
41	GPIO27	I/O		DCDD#	SPID_ EN#			LCDD3		Timer4	PUW
42	GPIO28	I/O						LCDD4 LCCD8 (dup)		EIRQ1 (dup)	PUW
43	GPIO29	I/O						LCDD5 LCCD9 (dup)		Timer5	PUW
44	GPIO30	I/O						LCDD6 LCDD10 (dup)		Timer6	PUW
45	GPIO31	I/O						LCDD7 LCDD11 (dup)			PUW
46	GPIO32	I/O						LCDD8	D0	EIRQ2	PUW
47	GPIO33	I/O						LCDD9	D1		PUW
48	GPIO34	I/O				SCL		LCDD10	D2		PUW
49	GPIO35	I/O				SDA		LCDD11	D3		PUW
50	GPIOSW36	I/O						LCDD12	D4	PWM0	PU10
51	GPIOSW37	I/O						LCDD13	D5	PWM1	PU10
52	GPIOSW38	I/O						LCDD14	D6	PWM2	PU10
53	GPIOSW39	I/O						LCDD15	D7	PWM3	PU10
54	GPIOSW40	I/O		TXDC	SPIC_ DO			LCDD16		EIRQ3	PU10
55	GPIOSW41	I/O		RXDC	SPIC_DI			LCDD17			PU10
56	GPIO42	I/O	USB_ EXTPHY_ D+	RTSC#							PUW
57	GPIO43	I/O	USB_ EXTPHY_ D-	CTSC#					DIRCON		PUW
58	GPIOSW44	I/O	USB_ EXTPHY_ OE#	TXDD	SPID_ DO				SELECT		PU10
59	GPIO45	I/O	USB_ EXTPHY_ RCV	RXDD	SPID_DI				STB		PUW
60	GPIO46	I/O	USB_ EXTPHY_ RXD+	RTSD#					ALFD		PUW
61	GPIO47	O	USB_ EXTPHY_ RXD-	CTSD#					INIT#		PUW
62	GPIO18	I/O	Ethernet ECAM_REJ					LCD_ PWREN#		EIRQ3 (dup)	PUW
63	GPIO22	I/O		RIC#	SPIC_ CLK			LCD_AE_ BDE			PUW
64	GPIO21	I/O		DSRC#				LCD_ VSYNC			PUW

Pin	Signal	Type	BootStrap (BS) / System / Other	UART	SPI	I2C	DMA	LCD	IEEE 1284	PWM / Timer / IRQ	Notes Reset state
65	GPIOSW19	I/O	Ethernet ECAM_ REQ				DMA1_ ACK#	LCD_ HSYNC			PU10
66	GPIOSW20	I/O		DTRC#				LCD_CLK			PU10
67	GPIO23	I/O		DCDC#	SPIC_ EN#			LCD_LEN D			PUW
68	A0	O									External address
69	A1	O									External address
70	A2	O									External address
71	A3	O									External address
72	A4	O									External address
73	A5	O									External address
74	A6	O									External address
75	A7	O									External address
76	A8	O									External address
77	A9	O									External address
78	A10	O									External address
79	GND	P									
80	A11	O									External address
81	A12	O									External address
82	A13	O									External address
83	A14	O									External address
84	A15	O									External address
85	A16	O									External address
86	A17	O									External address
87	A18	O									External address
88	A19	O									External address
89	A20	O									External address
90	A21	O									External address
91	GPIO66	O	A22								Set to external address
92	EXT_OE#	O									
93	EXT_WE#	O									
94	GPIO67	O	A23								Set to external address
95	CS0#	O	Chip select								
96	CS2#	O	Chip select								
97	CS3#	O	Chip select								
98	No connect	n/a									
99	PWREN	O									

Pin	Signal	Type	BootStrap (BS) / System / Other	UART	SPI	I2C	DMA	LCD	IEEE 1284	PWM / Timer / IRQ	Notes Reset state
100	No connect	n/a									Reserved as BATT_FLT#
101	GPIO48	I/O	USB_ EXTPHY_ SUSP				DMA1_ REQ		P_SEL	Timer14	PUW
102	GPIO16	I	USB_OVC						P_JAM (dup)		PUW
103	EXT_BE0#	O									External byte lane enable
104	EXT_BE1#	O									External byte lane enable
105	EXT_BE2#	O									External byte lane enable
106	EXT_BE3#	O									External byte lane enable
107	GPIO15	I		DCDA#	SPIA_ EN#			LCD_CLKI N		Timer2	PUW
108	No connect	n/a									
109	No connect	n/a									
110	GPIO14	I		RIA#	SPIA_ CLK					PWM3 (dup) Timer1	
111	GPIO70	O	A26 MCKE_2			SCL					
112	GPIO71	I/O	A27 MCKE_3			SDA					
113	GPIOSW17	I/O	USB_PWR								PU10
114	USB_ INTPHY_P	I/O									USB Host / Device
115	USB_ INTPHY_N	I/O									USB Host / Device
116	VRTC	P									3V RTC battery can be connected here
117	GND	P									
118	3.3V_IN	P									Unswitched 3.3V
119	VLIO	P									**Mobile:** Power from Li-Ion battery **Non-mobile:** Connected to unswitched 3.3V
120	3.3V_IN	P									Unswitched 3.3V

X2 Connector

Pin	Type	Signal	PCI	Ethernet	LCD	Notes
1		No connect	PCI_INTA#			
2	P	GND				
3		No connect	PCI_INTC#			
4		No connect	PCI_INTB#			
5		No connect	PCI_RESET#			
6		No connect	PCI_INTD#			
7		No connect	PCI_GNT0#			
8		GND				
9		No connect	PCI_GNT1#			
10		No connect	PCI_CLKOUT			
11		No connect	PCI_CLKIN			
12		No connect	PCI_GNT2#			
13		No connect	PCI_GNT3#			
14	P	GND				
15		No connect	PCI_AD30			
16		No connect	PCI_REQ0#			
17		No connect	PCI_REQ1#			
18		No connect	PCI_REQ2#			
19		No connect	PCI_REQ3#			
20		No connect	PCI_AD31			
21		No connect	PCI_AD28			
22		No connect	PCI_AD29			
23		No connect	PCI_AD26			
24		No connect	PCI_AD27			
25		No connect	PCI_AD24			
26		No connect	PCI_AD25			
27		No connect	PCI_IDSEL			
28		No connect	PCI_CBE3#			
29		No connect	PCI_AD22			
30		No connect	PCI_ADD23			
31		No connect	PCI_AD20			
32		No connect	PCI_AD21			
33		No connect	PCI_AD18			

Pin	Type	Signal	PCI	Ethernet	LCD	Notes
34		No connect	PCI_AD19			
35		No connect	PCI_AD16			
36		No connect	PCI_AD17			
37		No connect	PCI_FRAME#			
38		No connect	PCI_CBE2#			
39		No connect	PCI_TRDY#			
40	P	GND				
41		No connect	PCI_IRDY#			
42		No connect	PCI_STOP#			
43		No connect	PCI_PAR			
44		No connect	PCI_DEVSEL#			
45		No connect	PCI_AD15			
46		No connect	PCI_PERR#			
47		No connect	PCI_AD13			
48		No connect	PCI_SERR#			
49		No connect	PCI_AD11			
50		No connect	PCI_CBE1#			
51		No connect	PCI_AD9			
52		No connect	PCI_AD14			
53		No connect	PCI_CBE0#			
54		No connect	PCI_AD12			
55		No connect	PCI_AD6			
56		No connect	PCI_AD10			
57		No connect	PCI_AD4			
58		No connect	PCI_AD8			
59		No connect	PCI_AD2			
60		No connect	PCI_AD7			
61		No connect	PCI_AD5			
62		No connect	PCI_AD3			
63		No connect	PCI_AD1			
64		No connect	PCI_AD0			
65		No connect			LCD_CLKIN	
66	I			ETH_TPIN		

Pin	Type	Signal	PCI	Ethernet	LCD	Notes
67	O			ETH_LEDLNK		
68	I			ETH_TPIP		
69	O			ETH_LEDH		
70	O			ETH_TPON		
71	I			ETH_ESD0		
72	O			ETH_TPOP		
73		No connect				Reserved for ETH_EREF
74		No connect				
75		No connect				
76		No connect				
77		No connect				
78		No connect				
79		No connect				
80	P	GND				
81	I/O	D0				Data bus
82	I./O	D1				Data bus
83	I/O	D2				Data bus
84	I/O	D3				Data bus
85	I/O	D4				Data bus
86	I/O	D5				Data bus
87	I/O	D6				Data bus
88	I/O	D7				Data bus
89	I/O	D8				Data bus
90	I/O	D9				Data bus
91	I/O	D10				Data bus
92	I/O	D11				Data bus
93	I/O	D12				Data bus
94	I/O	D13				Data bus
95	I/O	D14				Data bus
96	I/O	D15				Data bus
97	I/O	D16				Data bus
98	I/O	D17				Data bus
99	I/O	D18				Data bus

Pin	Type	Signal	PCI	Ethernet	LCD	Notes
100	I/O	D19				Data bus
101	I/O	D20				Data bus
102	I/O	D21				Data bus
103	I/O	D22				Data bus
104	I/O	D23				Data bus
105	I/O	D24				Data bus
106	I/O	D25				Data bus
107	I/O	D26				Data bus
108	I/O	D27				Data bus
109	I/O	D28				Data bus
110	I/O	D29				Data bus
111	I/O	D30				Data bus
112	I/O	D31				Data bus
113		No connect				Reserved for A28
114		No connect				Reserved for A29
115		No connect				Reserved for A30
116		No connect				Reserved for A31
117		No connect				Reserved
118		No connect				Reserved
119	O	CLKOUT				
120	P	GND				

Configuration pins — CPU

Several pins allow configuration of the CPU before booting. CPU pins have weak pullups (value range is 15-300K) for a default configuration. Most pins do not have configuration options and some are connected for internal configuration on the module. Thirty-two of the 73 GPIO pins allow user-specific configurations, which are latched in the GEN_ID register (address 0xA090 0210) five clock cycles after the rising edge of RESET#. Certain pins are protected; that is, they are not accessible externally until strapping information that is configured on the module is latched.

Important

Normally, you will never need to change the hardware module CPU configuration. Configuring the module incorrectly can prevent the module from booting.

Default module CPU configuration

- Little endian mode selected
- PLL active (PLL bypass not allowed)
- PLL_FS divider set to 2
- PLL_ND multiplier set to 24 (177 MHz), 21 (154 MHz), or 14 (103 MHz)
- Boot from SPI EEPROM (spi.bin)

Configuration pins — Module

Module configuration pins change hardware configuration on the module (HCONF0-3) or are user-specific and are read in the GEN_ID register (SCONF0-3).

Module pin configuration

Bold entries indicate default values.

Signal name	Function	PU/PD	External pin name	Comment
DEBUG_EN#	CPU mode select 0 Disconnects TRST# and PWRFOOD for JTAG and boundary scan debug mode **1 TRST# and PWRGOOD connected for normal mode**	PU 10K	HCONF0	
FWP#	Internal NAND flash write protect 0 Write protect active 1 No write protect	PU 10K	HCONF1	
OCD_EN#	JTAG / Boundary scan function select 0 ARM debug mode, BISTEN# set to high **1 Boundary scan mode, BISTEN# set to low**	PU 10K	HCONF2	Select JTAG mode; DEBUG_EN# has to be low, too
	Not used		HCONF3	No function, no connect
GPIO38	User-defined software configuration pin; can be read in GEN_ID register bit 28, default high		SCONF0	Read bit 28, GEN_ID
GPIO39	User-defined software configuration pin; can be read in GEN_ID register bit 29, default high		SCONF1	Read bit 29, GEN_ID

Signal name	Function	PU/PD	External pin name	Comment
GPIO40	User-defined software configuration pin; can be read in GEN_ID register bit 30, default high		SCONF2	Read bit 30, GEN_ID
GPIO41	User-defined software configuration pin; can be read in GEN_ID register bit 31, default high		SCONF3	Read bit 31, GEN_ID

Recommended combinations of DEBUG_EN# and OCD_EN#

HCONF0	HCONF2	Mode
OFF	OFF	Normal mode
ON	OFF	Debug mode
OFF	ON	Not recommended
ON	ON	OCD mode

Clock generation

Clock frequencies

This table summarizes the clock frequencies for the 177 MHz module.

Crystal:	29.4912 MHz
PLL	
PLL_ND(4:0), PLL multiplier:	b10010, d24, CPU PLL active
PLL_FS(1:0), PLL divider:	b11, d2, CPU PLL active
PLL_IS(1:0), value:	b11, ND16-31, CPU PLL active
Resulting PLL clock:	353.8944 MHz
CPU clock:	176.9472 MHz
AHB, SDRAM, and external clock:	88.4736 MHz
BCLK clock:	44.2368 MHz
UART baud rate clock BBus:	44.2368 MHz
LCD clock:	88.4736 MHz, 44.2368 MHz, 22.1184 MHz, or 11.0592 MHz

Changing the CPU speed

To change the CPU speed, write in these fields in the PLL Configuration register:

- PLL ND SW (NDSW)
- PLL frequency select (FSEL)

- PLL SW change (PLLSW)

Important: When PLL parameters are changed, hardware reset duration is 4 ms for the PLL to stabilize. Applications using this feature need to discriminate between cold start and warm start.

Boot process

The ConnectCore 9P 9360 module is preconfigured to boot with SPI channel B from a serial EEPROM. The serial EEPROM contains memory controller setup for SDRAM bank 0, as well as an initial boot program that moves the boot loading program from NAND flash to SDRAM bank 0 and starts it. The size of the serial SPI EEPROM is 8KB.

Chip selects

The module has eight chip selects: four for dynamic memory and for static memory. Each chip select has a 256MB range.

Chip select memory map

Name	Pin	Address range	Size [Mb]	Use	Comments
SDM_CS0#	B4	0x00000000–0x0FFFFFFF	256	SDRAM bank 0	First bank on module
SDM_CS1#	A3	0x10000000–0x1FFFFFFF	256	SDRAM bank 1	Second bank on module
SDM_CS2#	D5	0x20000000–0x2FFFFFFF	256	No connect	
SDM_CS3#	C4	0x30000000–0x3FFFFFFF	256	No connect	
EXT_CS0#	B3	0x40000000–0x4FFFFFFF	256	External, CS0#	
EXT_CS1#	C1	0x50000000–0x5FFFFFFFF	256	NAND-Flash	Program memory
EXT_CS2#	D2	0x60000000–0x6FFFFFFFF	256	External, CS2#	
EXT_CS3#	E3	0x70000000–0x7FFFFFFF	256	External, CS3#	
Reserved		0x80000000–0x8FFFFFFF	256		
BBus		0x90000000–0x9FFFFFFF	256	BBus memory	
Reserved		0xA0000000–0xA03FFFFF	4		
Bridge		0xA0400000–0xA04FFFFF	1	Bridge	
Reserved		0xA0500000–0xA05FFFFF	1	Reserved	
Ethernet		0xA0600000–0xA06FFFFF	1	Ethernet module	
Memory		0xA0700000–0xA07FFFFF	1	Memory controller	

Name	Pin	Address range	Size [Mb]	Use	Comments
LCD		0xA0800000–0xA08FFFFF	1	LCD controller	
System		0xA0900000–0xA09FFFFF	1	System control module	
Reserved		0xA0A00000–0xFFFFFFFF	1	Reserved	

NAND flash

Access the NAND flash with EXT_CS1#. The FWP# signal write-protects the chip externally.

Onboard flash

The module has 32Mx8, 64Mx8, or 128Mx8 NAND flash onboard. Greater sizes can optionally be populated, if available. The interface to the NAND flash requires 32kB due to use of A13 and A14 for address and command control.

SDRAM banks

The module provides two SDRAM banks, connected to CS4# (D_CS0#) and CS5# (D_CS1#). CS6# (D_CS2#) nd CS7# (D_CS3#) are lost. The module does not provide external SDRAM connection.

The module has one of these SDRAM onboard: 1X4MX32, 2X4MX32, or 4X4M32. A12 is the highest address connected, and the chip select range is 256M.

BA0 and BA1 are connected to A13 and A14, respectively. The SDRAM controller connects the appropriate address line to allow a gapless memory space at different SDRAM sizes.

Using the second SDRAM bank

The module's SPI loader initializes only SDRAM bank 0 with SD_CS0. The second bank cannot be initialized when the system is running from SDRAM because it uses the same registers as the running (first) bank but for different parameters. The Dynamic Memory Control register, in particular, must use set mode command rather than normal mode command while starting the second bank. The initialization routine needs to be run from either NOR flash (if you are booting with flash) or from another memory location.

For example, you can run the initialization routine from the Ethernet TX buffer descriptor RAM, starting at address 0xA0601000 with a space of 256 * 32 bit words. Before using this RAM, however, bit 23 in the Ethernet General Control Register 1 must be set to high to enable the RAM.

Multiplexed GPIO pins

The 73 GPIO pins on the module are multiplexed with these other functions:

- UART and SPI
- USB
- Ethernet
- DMA
- Parallel port IEEE1284
- I^2C (IIC) port
- LCD port
- Timers and interrupt inputs
- Memory bus address and control pins

If a pin is used as GPIO, it "gives up" another function.

Pin notes

- GPIO0 – GPIO48 and GPIO66 – GPIO72 are accessible on the connectors.
- GPIO13 is used for RTC interrupt on the module (allows sharing with open drain ORing).
- GPIO 49 – GPIO65 are used on the module and are not accessible externally.
- All GPIOs are set to GPIO input function after RESET. Use in another function requires configuring the GPIO registers at powerup.

GPIO multiplex table

Some signals are multiplexed to two different GPIO pins, to maximize the number of possible applications. These duplicate signals are marked as *(dup)* in the table. Selecting the primary GPIO pin and the duplicate GPIO pin for the same function is not recommended. If both the primary GPIO pin and duplicate GPIO pin are programmed for the same function, however, the primary GPIO pin has precedence and will be used.

Port name, Function 03 (default at powerup)	Alternate function 00, UART	Alternate function 00, miscellaneous	Alternate function 01	Alternate function 02	On module, default used as
GPIO0	TXDB	SPI_Boot_DO SPIB_DO	DMA0 DONE (dup)	Timer 1 (dup)	TXDB, SPI_Boot_DO, or external SPIB_DO
GPIO1	RXDB	SPI_Boot_DI SPIB_DI	DMA0 REQ (dup)	EIRQ0	RXDB, SPI_Boot_DI, or external SPIB_DI
GPIO2	RTSB#		Timer 0	DMA1 ACK	RTSB#, DMA
GPIO3	CTSB#		1284 ACK#	DMA0 REQ	CTSB#, DMA

Port name, Function 03 (default at powerup)	Alternate function 00, UART	Alternate function 00, miscellaneous	Alternate function 01	Alternate function 02	On module, default used as
GPIO4	DTRB#		1284 BUSY	DMA0 DONE	DTRB#
GPIO5	DSRB#		1284 ERR	DMA0 ACK	DSRB#, DMA
GPIO6	RIB#	SPI_Boot_CLK SPIB_CLK External RXCLK_A	1284 P_JAM	Timer 7 (dup)	RIB#, SPI_Boot_CLK, or external SPIB_CLK
GPIO7	DCDB#	SPI Boot CE# SPIB_CE# External TXCLK_A	DMA0 Ack (dup)	EIRQ1	DCDB#, SPI_Boot_CE#, or external SPIB_CE#
GPIO8	TXDA	SPIA_DO	Reserved	Reserved	TXDA, SPI A
GPIO9	RXDA	SPIA_DI	Reserved	Reserved	RXDB, SPI A
GPIO10	RTSA#		Reserved	PWM0 (dup)	GPIO10
GPIO11	CTSA#		EIRQ2 (dup)	Timer 0 (dup)	GPIO11
GPIO12	DTRA#		Reserved	PWM1 (dup)	GPIO12
GPIO13	DSRA#		EIRQ0 (dup)	PWM2 (dup)	EIRQ0 connected to RTC_INT# on module
GPIO14	RIA#	SPIA_CLK External RXCLK_B	Timer 1	PWM3 (dup)	SPI A
GPIO15	DCDA#	SPIA_EN# External TXCLK B	TImer 2	LCD_CLKIN	SPI A
GPIO16		USB overcurrent	1284 P_JAM (dup)	Reserved	USB_OVCUR
GPIO17		USB power relay	Reserved	Reserved	USB_PREL
GPIO18		Ethernet CAM reject	LCD PWREN	EIRQ3 (dup)	LCD
GPIO19		Ethernet CAM request	LCD HSYNC	DMA1 ACK (dup)	LCD
GPIO20	DTRC#		LCD CLK	Reserved	LCD
GPIO21	DSRC#		LCD VFSYNC	Reserved	LCD
GPIO22	RIC#	SPIC_CLK External RXCLK_C	LCD_BIAS_D_EN	Reserved	LCD
GPIO23	DCDC#	SPIC_EN External TXCLK_C	LCD LINE_END	Reserved	LCD
GPIO24	DTRD#		LCDD0	Reserved	LCD
GPIO25	DSRD#		LCDD1	Reserved	LCD
GPIO26	RID#	SPID_CLK External RXCLK_D	LCDD2	Timer 3	LCD