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ConnectCore™ 9M 2443 and Wi-9M 2443

Hardware Reference

90000952_F

Release date: May 2011

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Using this Guide

This guide provides information about the Digi ConnectCore 9M and ConnectCore Wi-9M embedded core modules.

To access current technical documentation available for the S3C2443 processor please visit the Samsung website:
http://www.samsung.com/global/business/semiconductor/productInfo.do?fmly_id=229&partnum=S3C2443

Conventions used in this guide

This table describes the typographic conventions used in this guide:

This convention	Is used for
italic type	Emphasis, new terms, variables, and document titles.
monospaced type	Filenames, pathnames, and code examples.

Digi information

Documentation updates

Please always check the product specific section on the Digi support website for the most current revision of this document: www.digiembedded.com/support.

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Change Log

1. Added WLan information for the ConnectCore Wi-9M 2443.
2. Added WLan information under environmental specifications in Appendix A.
3. Added a new drawing on page 136.
4. Made minor document updates.
5. Revised the module pinout table for pins X1-27, X1-45, X1-46, and X2-4.
6. Updated the Standard Module Variants table in Chapter 1.
7. Added Declaration of Conformity information for the ConnectCore Wi-9M 2443.
8. Removed barcode (last page) from document.
9. Removed the mention of “EEPROM” from the Module Block Diagram in Chapter 1.
10. Added a note to the USB Interface table in Chapter 1.

About the Module

CHAPTER 1

The network-enabled ConnectCore 9M 2443 core module family delivers leading performance, low power operation, and rich peripheral interface support for a wide variety of applications, including medical devices, transportation, security/access control, networked displays, and more.

The modules utilize an innovative and power-efficient Samsung S3C2443 processor with up to 533 MHz and a multilayered memory bus architecture that allows simultaneous data transfer between processor, memory and peripherals. This optimized design eliminates the traditional bus bandwith bottlenecks that are common on other platforms. For example, updating graphical information through the LCD controller and retrieving relevant data from memory at the same time can now be realized without compromising overall performance and user experience.

Designed from the ground up with power budget conscious applications in mind, the ConnectCore 9M 2443 module family is an ideal system platform for mobile and battery-operated product designs with full off-the-shelf hard- and software support for all power management modes. The modules also offer a wide variety of on-board peripherals such as network connectivity options, a TFT/CSTN LCD controller, camera interface, audio codec interfaces, hi-speed USB device, full-speed USB host, high-speed memory card support, external mass storage, and other interfaces.

Features and functionality

32-bit Samsung S3C2443 processor

- ARM920T core at 400/533 MHz
- 16 KB of instruction/data cache
- Up to 133 MHz memory bus speed
- Up to 1 GB of NAND Flash
- Up to 256 MB DDR SDRAM

LCD controller (CSTN/TFT)

- Up 1024x1024 pixels resolution
- Up to 16 grey levels/4096 colors (STN)
- Up to 24 bpp, two overlay windows (TFT)

Camera interface

- ITU-R BT 601/656 8-bit mode support
- 4096x4096 pixels / 2048x2048 scaling
- Mirror, 180° rotation, digital zoom in
- RGB 16/24-bit, YCbCr 4:2:0/4:2:2 output

I2S and AC'97 audio codec controllers

Ethernet Interface

- 10/100 Mbit Ethernet MAC and PHY

WLAN Interface

- 802.11a/b/g WLAN interface with dual-diversity antenna setup

USB support with integrated PHYs

- USB 2.0 device, 1-port, high-/full-speed

- USB 1.1 host, 2-port, low-/full-speed
- Ethernet interface
  - 10/100 Mbit Ethernet MAC and PHY
- WLAN interface
  - 802.11a/b/g WLAN interface with dual-diversity antenna setup

4-channel UART

- Up to 921 kbps, IrDA 1.0 SIR mode

2-port SPI/Single-port HS-SPI

- Master and slave mode
- Up to 33 MHz

I2C-Bus Interface

- 1-ch Multi-Master IIC-Bus
- Serial, 8-bit oriented and bi-directional data transfers up to 100 Kbit/s in Standard mode or up to 400 Kbit/s in fast mode

SD/SDIO/MMC

- 1-/4-bit and block/stream, up to 25 MHzHigh-Speed (HS) MMC
- SD HC 1.0, SD MC 2.1, SDIO 1.0, MMC 4.2
- 1-/4-/8-bit modes, up to 50 MHz
- CE-ATA mode support

CF/ATA

- Compact Flash 3.0 PC card mode
- ATA/ATAPI-6 mode with PIO/UDMA

10-bit ADC & Touch Screen Interface

- 10-channel multiplexed, 500k samples/s

Timers/PWM

- 4-ch 16-bit timer/PWM, 1-ch 16-bit internal

8-/16-bit external memory bus interface

Power management modes

- Normal, idle, stop, and sleep
- Ext IRQ, RTC alarm, tick interrupt wake-up

GPIO options

- Up to 15 external IRQs
- Up to 134 multiplexed GPIOs on the ConnectCore 9M 2443
- Up to 132 multiplexed GPIOs on the ConnectCore Wi-9M 2443

Watchdog Timer (16-bit)

Real-time clock with calendar function

Two 120-pin board-to-board connectors

JTAG signals available on module connectors

Standard module variants

The ConnectCore 9M 2443 module is currently available in the standard variants below.

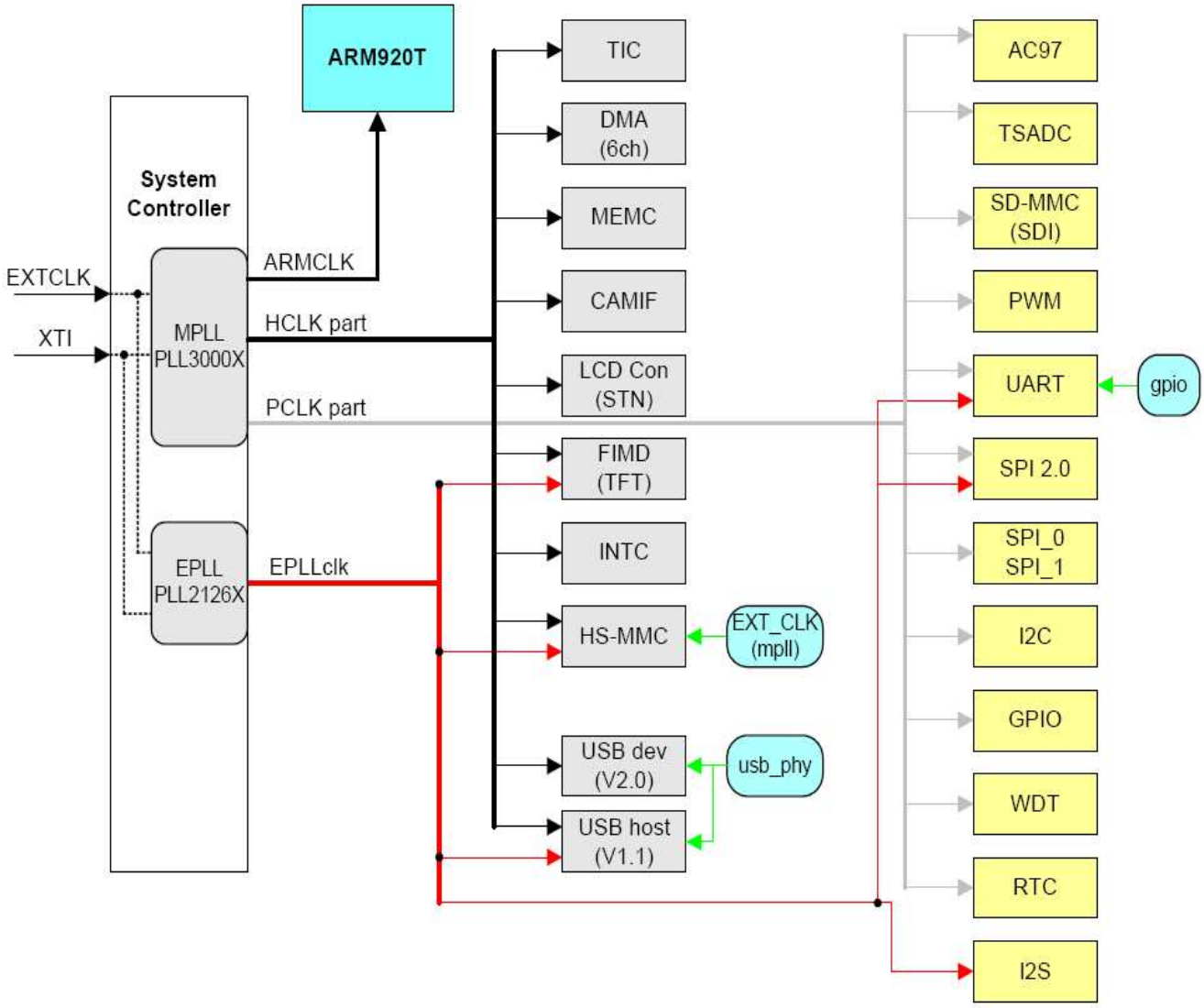
Speed	Flash	SDRAM	Operating temperature	P/N
533 MHz	128 MB	64 MB	-40 to 85C	CC-9M-NA37-Z1
533 MHz	64MB	32 MB	-40 to 85C	CC-9M-NA26-Z1
400 MHz	32 MB	32 MB	0 to 70C	CC-9M-QA25-Z1
533 MHz	128 MB	64 MB	-40 to 65C*	CC-W9M-NA37-XE
533 MHz	64MB	32 MB	-40 to 65C*	CC-W9M-NA26-XE
400 MHz	32 MB	32 MB	0 to 65C*	CC-W9M-QA25-XE

* See section “Thermal specifications” in this document for details.

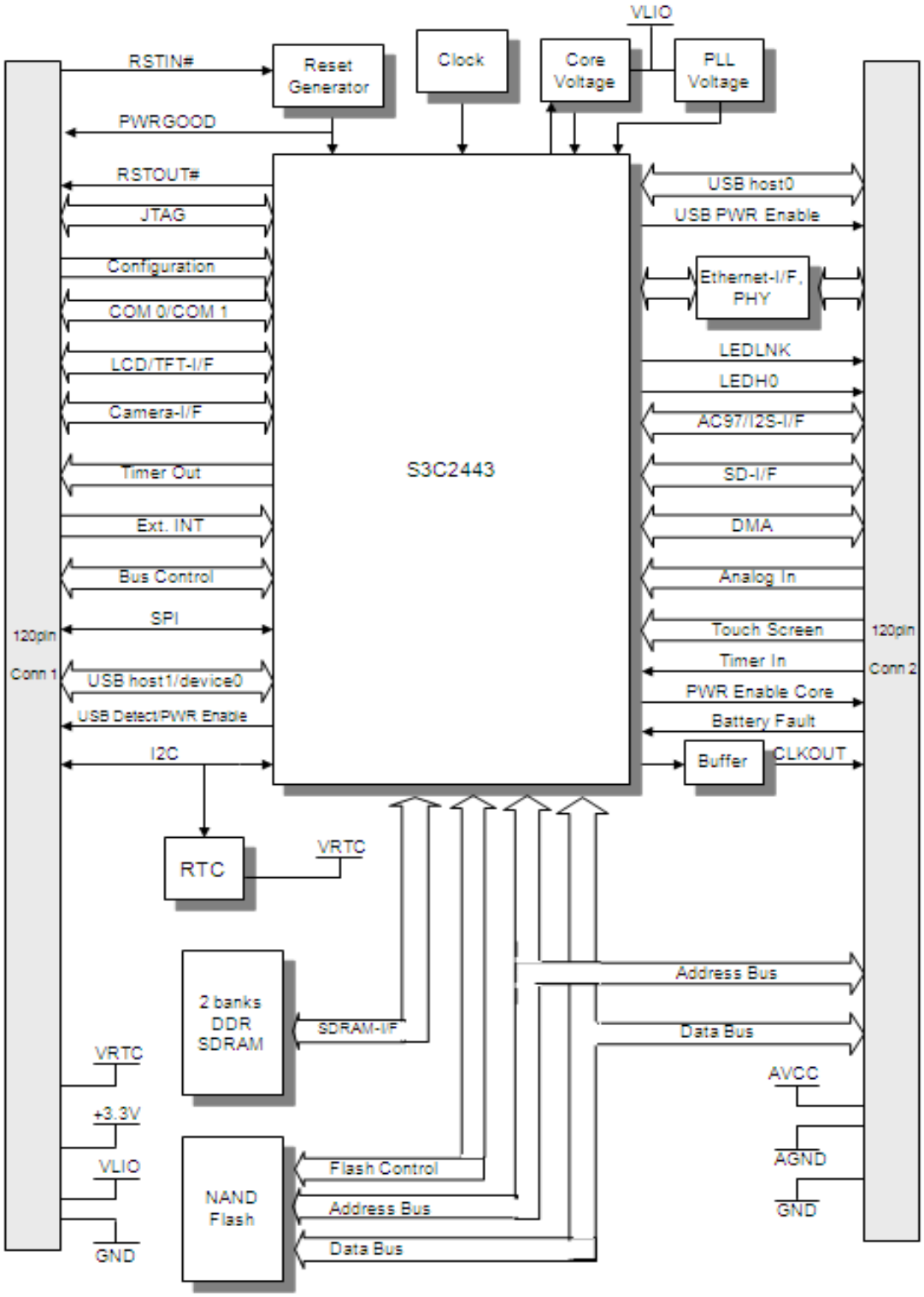
Please visit the Digi web site, www.digiembedded.com/support, or contact Digi for additional population options.

Block diagrams

CPU



Module


VLIO
RSTIN#
Reset Generator
Clock
Core Voltage
PLL Voltage
PWRGOOD
RSTOUT#
JTAG
Configuration
COM 0/COM 1
LCD/TFT-I/F
Camera-I/F
Timer Out
Ext. INT
Bus Control
SPI
USB host1/device0
USB Detect/PWR Enable
I2C
S3C2443
USB host0
USB PWR Enable
Ethernet-I/F, PHY
LEDLNK
LEDH0
AC97/I2S-I/F
SD-I/F
DMA
Analog In
Touch Screen
Timer In
PWR Enable Core
Battery Fault
Buffer
CLKOUT
120pin Conn 1
120pin Conn 2
RTC
VRTC
2 banks DDR SDRAM
SDRAM-I/F
Address Bus
Data Bus
VRTC
+3.3V
VLIO
GND
NAND Flash
Flash Control
Address Bus
Data Bus
AVCC
AGND
GND

Detailed module description

Configuration

The ConnectCore 9M 2443 Module supports 8 configuration pins:

- 4 pins provided for software configuration, which are routed to standard pin locations on the development board (CONF[7:4]).
- 4 pins provided for hardware configuration, routed to the base board at standard pin locations, including debug enable (DEBUG_EN#) and NAND flash write protect (NAND_FWP#).

Power Supply

The common power supply for the module is 3.3VDC. VLIO has to be connected to 3.3V on the base board.

The CPU specific core voltage of 1.2V@300MHz (1.3V@400MHz) and the voltage for VDD alive will be generated on the module from the VLIO input, while the voltage for memory power supply and I/OS is fed directly from the 3.3V.

The following requirements have to be met by the power supply:

Power Supply	@400MHz	@533MHz
Module Power Supply 3.3V	3.3V ±5%	3.3V ± 5%
Module Power Supply VLIO	3.3V ±5%	3.3V ±5%
Core Voltage	1.3V (1.25V - 1.35V)	1.375 (1.325V - 1.425V)
VDD alive	1.15V - 1.35V	1.15V - 1.2V
Voltage for internal RTC	3V (1.8V - 3.6V)	3V (1.8V - 3.6V)
Power Supply for ext. RTC VRTC	3V (e.g. Li-Battery)	3V (e.g. Li-Battery)
Analog Voltage	3.3V (3V - 3.6V)	3.3V (3V - 3.6V)
VIN at common CPU pins	-0.3V - 3.3V ± 0.3V	-0.3V - 3.3V ± 0.3V

The voltage at pin RTCVDD has been connected to 3.3V, even though the RTC is not used. If VDD_RTC is not used, it has to be high (VDD_RTC=3.3V).

The S3C2443 supports DVS (dynamic voltage scaling). This means that the core voltage may be reduced to 1V in idle mode while clock frequency is also reduced.

VRTC is used to connect a battery on the base board for the external RTC on the module. If the external RTC is not used, pin VRTC doesn't need to be connected. VRTC is only used to power the external RTC on the module.

If a battery supplies the power for the module, the pin BATT_FLT# can be connected to a comparator output on the base board. The comparator may supervise the battery voltage on the base board. The CPU does not wake up at power-off mode in case of

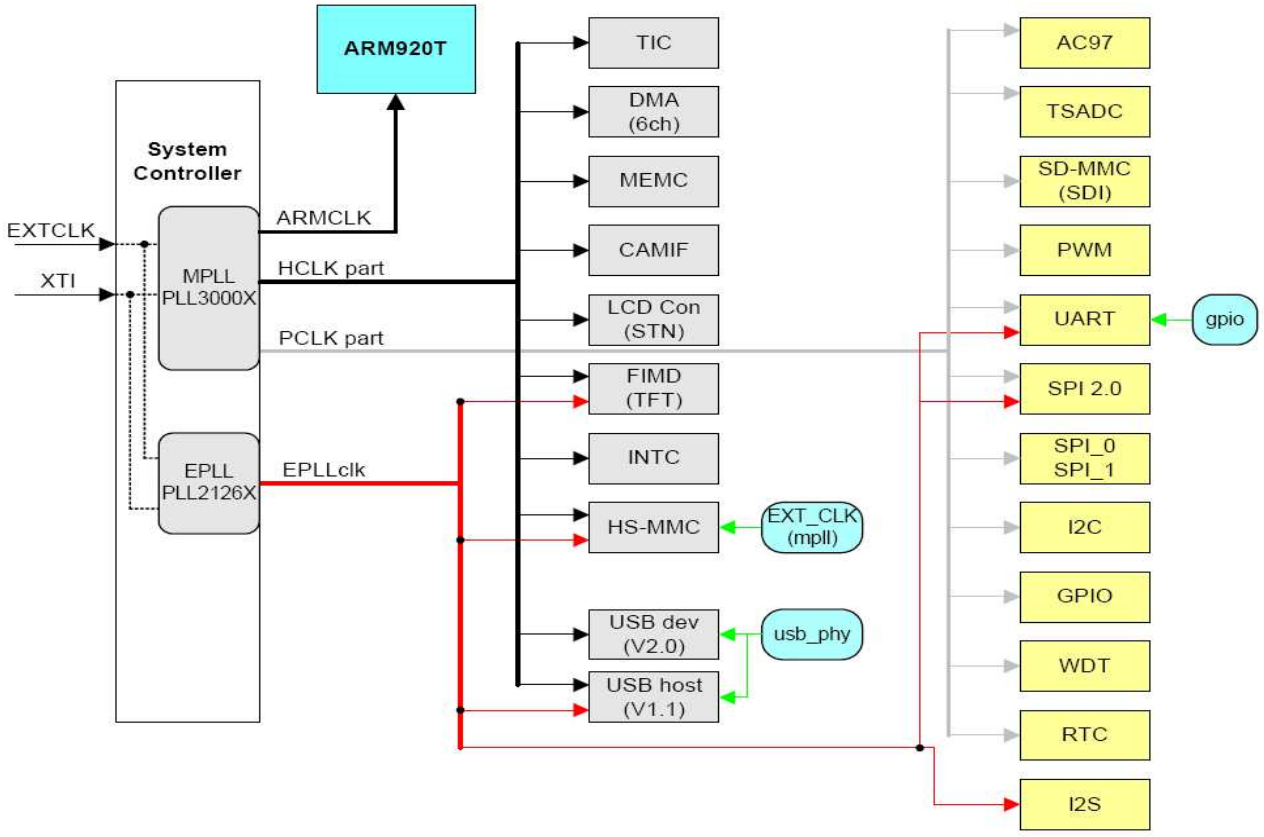
low battery state. If this feature is not used, the pin has to be left open, because a 10k pull up resistor is provided at the module.

Analog voltage AVCC and AGND, e.g. for a touch screen, are also provided on the module system connector.

For the power control logic, the S3C2443 has various power management schemes to keep optimal power consumption for a given task. These schemes are related to PLL, clock control logics (ARMCLK, HCLK, and PCLK) and wake up signals.

- ARMCLK is used for ARM920T core.
- HCLK is the reference clock for internal AHB bus and peripherals such as the memory controller, the interrupt controller, LCD controller, the DMA, USB host block, System Controller, Power down controller and etc.
- PCLK is used for internal APB bus and peripherals such as WDT, IIS, I2C, PWM timer, ADC, UART, GPIO, RTC and SPI etc.

The following figure shows the clock distribution:



Power management

The power management block in the S3C2443 can activate four modes: NORMAL, STOP, IDLE, and SLEEP. These are described below.

NORMAL mode

In General Clock Gating mode, the On/Off clock gating of the individual clock source of each IP block is performed by controlling each corresponding clock source enable bit. The Clock Gating is applied instantly whenever the corresponding bit is changed.

IDLE mode

In IDLE mode, the clock to the CPU core is stopped. The IDLE mode is activated just after the execution of the STORE instruction that enables the IDLE Mode bit. The IDLE Mode bit should be cleared after wake-up from IDLE state.

STOP mode

All clocks are stopped for minimum power consumption. Therefore, the PLL and oscillator circuits are also stopped (oscillator circuit is controlled by PWRCFG register). The STOP mode is activated after the execution of the STORE instruction that enables the STOP mode bit. The STOP Mode bit should be cleared after wake-up from STOP state.

To exit from STOP mode, external interrupt, RTC alarm, RTC Tick, or BATT_FLT has to be activated. During the wake-up sequence, the crystal oscillator and PLL may begin to operate. The crystal oscillator settle-down time and the PLL lock-time is required for a stable ARMCLK and automatically inserted by the hardware of S3C2443X. During these lock and settle-down times, no clock is supplied to the internal logic circuitry.

The following describes the sequence initiating STOP mode:

1. Set the STOP Mode bit (by the main CPU).
2. System controller requests bus controller to finish pending transaction.
3. Bus controller sends acknowledgement to system controller after bus transactions are completed.
4. System controller requests memory controller to enter self-refresh mode, preserving SDRAM contents.
5. System controller waits for self-refresh acknowledgement from memory controller.
6. After receiving the self-refresh acknowledge, system controller disables system clocks, and switches SYSCLK source to MPLL reference clock.
7. Disables PLLs and Crystal (XTI) oscillation. If OSC_EN_STOP bit in PWRCFG register is 'high,' then system controller does not disable crystal oscillation.

Note: *DRAM has to be in self-refresh mode during STOP and SLEEP mode to retain valid memory data. LCD must be stopped before STOP and SLEEP mode, because DRAM can not be accessed when it is in self-refresh mode.*

SLEEP mode

The block disconnects power to CPU, and the internal logic, with the exception of the wake-up logic. Activating the SLEEP mode requires two independent power sources. One of the two power sources supplies the power for the wake-up logic. The other power source supplies the CPU and internal logic, and should be controlled for power on/off. In SLEEP mode, the second power supply source for the CPU and internal logic will be turned off. The wake-up from SLEEP mode can be issued by EINT[15:0].

In SLEEP mode, VDDi, VDDiarm, VDDMPLL and VDDEPLL will be turned off, and are controlled by PWREN. If the PWREN signal is activated (H), VDDi and VDDiarm are supplied by an external voltage regulator. If PWREN pin is inactive (L), VDDi and VDDiarm are turned off.

In Power_OFF mode 1.2V have to be supplied to the VDD alive pin, and it is also necessary to provide the I/O-voltages of 1.8V/3.3V. Therefore the LDO, which supplies VDD alive will not be switched off.

The following describes the sequence of entering SLEEP mode:

1. One of the SLEEP Mode entering events is triggered by the system software or by the hardware.
2. System controller requests bus controller to finish pending transaction.
3. Bus controller sends acknowledgement to system controller after bus transactions are completed.
4. System controller requests memory controller to enter self-refresh mode, preserving SDRAM contents.
5. System controller waits for self-refresh acknowledgement from memory controller.
6. After receiving the self-refresh acknowledge, disables the XTAL and PLL oscillation and also disables the external power source for the internal logic by asserting the PWR_EN pin to low state. The PWR_EN pin is the regulator disable control signal for the internal logic power source.

The SLEEP mode exit sequence is as follows.

1. System controller enables external power source by deasserting PWR_EN to high state and initiates power settle down programmable through a register in the PWRSETCNT field of RSTCON register.
2. System controller releases the System Reset (synchronously, relatively to the system clock) after the power supply is stabilized.

Wake-up event

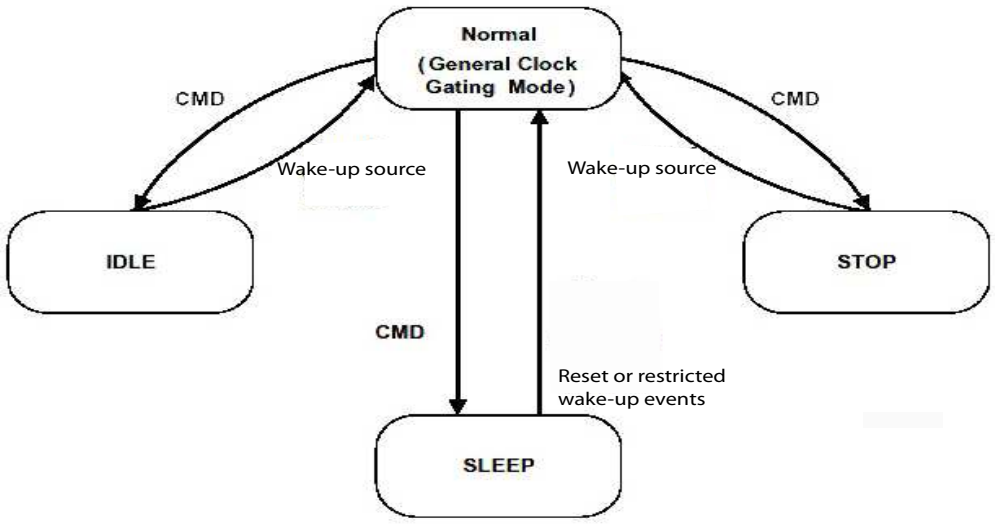
When S3C2443X wakes up from the STOP Mode by an External Interrupt, an RTC alarm interrupt and other interrupts, the PLL is turned on automatically. The initial-state of S3C2443X after wake-up from the SLEEP Mode is almost the same as the Power-On-Reset state except for the contents of the external DRAM is preserved. In contrast, S3C2443X automatically recovers the previous working state after wake-up from the STOP Mode. The following table shows the states of PLLs and internal clocks after wake-ups from the power-saving modes.

Mode before wake-up	PLL on/off after wake-up	SYSCLK after wake-up and before the lock time	SYSCLK after the lock time by internal logic
IDLE	Unchanged	PLL output	PLL output
STOP	PLL state ahead of entering STOP mode (PLL ON or not)	PLL reference clock	SYSCLK ahead of entering STOP mode (PLL output or not)
SLEEP	Off	PLL reference clock	PLL reference (input) clock

- To enter sleep mode by BATT_FLT, BATF_CFG bits of PWRCFG register must be configured.
- Do not exit from sleep mode when BATT_FLT is LOW; SLEEP_CFG bit of PWRCFG register must be configured.

A Battery Fault Signal (BATT_FLT#) is provided at the CPU to recognize the battery state of the battery at the base board, which powers the module. Therefore this pin is routed to the system connector. At the base board a comparator has to supervise the battery state and the output of the comparator delivers the BATT_FLT# signal.

The figure below shows the power management state diagram:



Reset

There are 3 reset signals defined, which are routed to the system connector:

- a reset input to the module (RSTIN#)
- an output of the reset controller from the module (PWRGOOD)
- a reset output from the CPU (RSTOUT#)
- RSTIN# signal from the base board is connected to the reset generator device on the module. At the base board there could be a reset switch connected to the RSTIN# signal. A 10k pull up resistor is connected to the RSTIN# signal on the module.
- PWRGOOD must be held to low level at least 4 FCLKs to recognize the reset signal.

The low active reset of the reset controller is connected to the system via a 470R series resistor.

RSTOUT# can be used for external device reset control. RSTOUT# is a function of Watchdog Reset and Software Reset (RSTOUT# = PWRGOOD & WDTRST# & SW_RESET).

Memory

DDR SDRAM memory

On the module there are two banks provided for DDR SDRAM memory. Both banks can support a 16-bit mobile DDR memory chip. Bank 1 provides one part of a 16bit DDR SDRAM in a FBGA60 package, with 1.8V power supply.

Total size of memory is possible from 16MB (only one bank) up to 256MB (128MB each bank).

Both banks have to be populated with equal devices since they share all control signals with the exception of their chip selects.These are defined in the bank control registers BANKCFG and BANKCON1-3 and Refresh Control Register.

NAND Flash memory

NAND Flash memory is provided, as a single Flash device. In order to support NAND flash boot loader, the S3C2443 is equipped with an internal SRAM buffer called Steppingstone. When booting, the first 4 KBytes of the NAND flash memory will be loaded into Steppingstone and the boot code loaded into Steppingstone will be executed.

Generally, the boot code will copy NAND flash content to DDR-SDRAM. Using hardware ECC, the NAND flash data validity will be checked. Upon the completion of the copy, the main program will be executed on the DDR-SDRAM.

Features:

- NAND Flash memory I/F: Supports 512Bytes and 2KBytes Page.
- Interface: 8-bit NAND flash memory interface bus.
- Hardware ECC generation, detection and indication (Software correction).
- SFR I/F: Supports Little Endian Mode, Byte/half word/word access to Data and ECC Data register, and Word access to other registers.
- Steppingstone I/F: Supports Little/Big Endian, Byte/half word/word access.
- The Steppingstone 4-KB internal SRAM buffer can be used for another purpose after NAND flash booting.

The write protect pin of the Flash device is routed to the hardware configuration pin of the system connector FWP#. The device can be write protected at the base board by connecting this pin to GND. At the module, a pull-up resistor is equipped.

Configuration pins - CPU module

There are eight configuration pins provided on the system connector. Four of them are provided as hardware configuration pins, and the other four can be used as software configuration pins. A 10k pull up resistor is provided on each signal line of the configuration pins.

The following pins on the connector are defined as hardware configuration pins:

Signal	Description
DEBUGEN#	Debug enable
FWP#	Write protect of internal flash
CONF2	Hardware configuration 2 (not yet used)
CONF3	Hardware configuration 3 (not yet used)

The following port pins are defined as software configuration pins:

Signal	Port Pin	Description
CONF4	GPF2	Software configuration 0
CONF5	GPF3	Software configuration 1
CONF6	GPF4	Software configuration 2
CONF7	GPF5	Software configuration 3

The signal DEBUGEN# (CONF0) from the base board to the module is necessary to allow switching a connection on and off between the system reset and the JTAG reset.

Signal	State	Description
DEBUGEN#	High	Switch is on, TRST# and PWRGOOD are connected (default)
DEBUGEN#	Low	Switch is off, TRST# and PWRGOOD are disconnected

At the module a pull up resistor is provided on the DEBUGEN# signal. Therefore only a jumper to GND is necessary on the base board.

Chip selects

Chip select memory map

Name	CPU Signal name	Pin	Address Range	Size [Mb]	Usage	Comments
SCS0#	SCS0#	H15	0x3000_0000-0x37FF_FFFF	128	SDRAM bank 0	First bank on module
SCS1#	SCS1#	D17	0x3800_0000-0x3FFF_FFFF	128	SDRAM bank 1	
RCS0#	RCS0#	A2	0x0000_0000-0x03FF_FFFF	64	not available	
RCS1#	RCS1#	A1	0x0800_0000-0x083F_FFFF	64	external, RCS1#	
RCS2#	RCS2#	B3	0x1000_0000-0x103F_FFFF	64	external, RCS2#	
RCS3#	RCS3#	C1	0x1800_0000-0x183F_FFFF	64	external, RCS3#	
RCS4#	RCS4#	C4	0x2000_0000-0x203F_FFFF	64	external, RCS4#	
RCS5#	RCS5#	E4	0x2800_0000-0x283F_FFFF	64	internal, RCS5#	Used for Ethernet Controller

Multiplexed GPIO pins

S3C2443X Port Configuration

Port A	Selectable Pin Functions			On module, default used as
GPA15	Output only	nWE_CF	-	Output
GPA14	Output only	RSMAVD	-	Output
GPA13	Output only	RSMCLK	-	Output
GPA12	Output only	nRCS5	-	nRCS5
GPA11	Output only	nOE_CF	-	Output
GPA10	RDATA_OEN	RADDR25	-	RADDR25
GPA9	Output only	RADDR24	-	RADDR24
GPA8	Output only	RADDR23	-	RADDR23
GPA7	Output only	RADDR22	-	RADDR22
GPA6	Output only	RADDR21	-	RADDR21
GPA5	Output only	RADDR20	-	RADDR20
GPA4	Output only	RADDR19	-	RADDR19
GPA3	Output only	RADDR18	-	RADDR18
GPA2	Output only	RADDR17	-	RADDR17
GPA1	Output only	RADDR16	-	RADDR16
GPA0	Output only	RADDR0	-	RADDR0