Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ConnectCore®

for i.MX51

Hardware Reference Manual

Revision history—90001128

Revision	Date	Description
L	September, 2013	Changed storage temperature to -40°C to +85°C (-40°F to +185°F) on page 129. Revised Bottom View image on page 149. Revised Side View image on page 150.
M	May, 2014	Correct inaccuracy and sharpen clarity on the high temp start up issue.
N	November, 2014	Miscellaneous editorial updates. Updated the voltages for the table in Coin cell input (VCC_COINCELL). Added a table of related publications.
P	June, 2017	Updated branding and added statements for RED compliance.
R	April, 2018	Added coin cell input topic.

Trademarks and copyright

Disclaimers

Information in this document is subject to change without notice and does not represent a commitment on the part of Digi International. Digi provides this document “as is,” without warranty of any kind, expressed or implied, including, but not limited to, the implied warranties of fitness or merchantability for a particular purpose. Digi may make improvements and/or changes in this manual or in the product(s) and/or the program(s) described in this manual at any time.

Warranty

To view product warranty information, go to the following website:

www.digi.com/howtobuy/terms

Send comments

Documentation feedback: To provide feedback on this document, send your comments to techcomm@digi.com.

Customer support

Digi Technical Support: Digi offers multiple technical support plans and service packages to help our customers get the most out of their Digi product. For information on Technical Support plans and pricing, contact us at +1 952.912.3444 or visit us at www.digi.com/support.

Contents

About the module

About the development board

Module specifications

Module dimensions

Regulatory information

Maximum power and frequency specifications

About the module

The network-enabled ConnectCore for i.MX51 is a highly integrated System-on-Module (SOM) solution based on the new Freescale® i.MX51X application processor with a high-performance ARM® Cortex-A8® core, powerful multimedia options, and a complete set of peripherals.

The module combines the fast integration, reliability and design flexibility of an off-the-shelf SOM with complete out-of-the-box software development support for platforms such as Microsoft® Windows® Embedded CE 6.0, Windows Embedded Compact 7Digi® Embedded Linux® and Timesys® LinuxLink®.

With industry-leading performance and key features like a dual-display interface and a hardware encryption engine, the module is the ideal choice for a broad range of target markets including medical, digital signage, security/access control, retail, industrial/building automation, transportation and more.

Complete and cost-efficient Digi JumpStart Kits™ for Microsoft Windows Embedded CE 6.0 and Linux allow immediate and professional embedded product development with dramatically reduced design risk and time-to-market.

Features and functionality

The ConnectCore for i.MX51 module is based on the i.MX51 processor from Freescale. This processor offers a high number of interfaces. Most of these interfaces are multiplexed and are not available simultaneously. The module has the following features:

- High-end, low-power 32-bit System-on-Module
- 600/800 MHZ ARM Cortex-A8 core
  - 32 kB L1 instruction and 32 kB L1 data cache
  - 256 kB L2 cache
  - NEON co-processor
  - Vector Floating Point (VFP) unit
- SLC and MLC NAND flash support on module
- Up to 512 MB 32-bit/200 MHZ DDR2-400 memory
- Debug interfaces
  - Joint Test Action Group (JTAG)
  - Embedded Trace Macrocell™ (ETM) / Embedded Trace Buffer (ETB)
- Real Time Clock (RTC)
- Security co-processor
  - Encryption: Advanced Encryption Standard (AES), Data Encryption Standard (DES), 3DES and RC4
  - Hashing algorithms: Message Digest (MD)5, Secure Hash Algorithm (SHA)-1, SHA-224 and SHA-256
- Timer
- Watchdog
- Up to three universal asynchronous receiver/transmitter (UART) ports, up to 4 Mb/s each
- Up to three Serial Peripheral Interface (SPI), two of them up to 54 Mb/s each
- Two Inter-Integrated Circuit (I2C) (up to 400 kb/s)
- Three memory card interfaces (two for the wireless version of the module)
  - SD/Secure Digital Input Output (SDIO) - 1 and 4-bits (up to 200 Mb/s)
  - MultiMediaCard (MMC) - 1, 4 and 8-bits (up to 416 Mb/s)
- USB
- Up to 3x USB 2.0 High-Speed USB Host ports
- One USB 2.0 On-The-Go USB port with integrated Physical Layer (PHY) on the module

- 1-wire
- Keypad 6x4
- Two independent pulse-width modulation (PWM) interfaces
- 8, 16-bit External Memory interface
- General-purpose input/output (GPIO) with interrupt capabilities
- Up to 3x 10-bit analog-to-digital converter (ADC) channels
- Multimedia
  - 2x Camera ports
  - 2x Display ports
  - 4-wire touch screen
- Sony/Philips Digital Interface Forma (SPDIF) output
- Three I2S / Audio Codec '97 (AC'97) / Synchronous Serial Interfaces (SSI), up to 1.4Mb/s each
- On-module three axis accelerometer (optional)
- On-module 10/100 Ethernet controller (optional)
- Second on-module 10/100Mb Ethernet interface (optional)
- 2.4 GHz and 5 GHz Institute of Electrical and Electronics Engineers (IEEE) 802.11a/b/g/n wireless local area network (LAN) interface (optional)
- Complete Microsoft Windows Embedded CE 6.0 and Linux platform support with full source code

Module variant

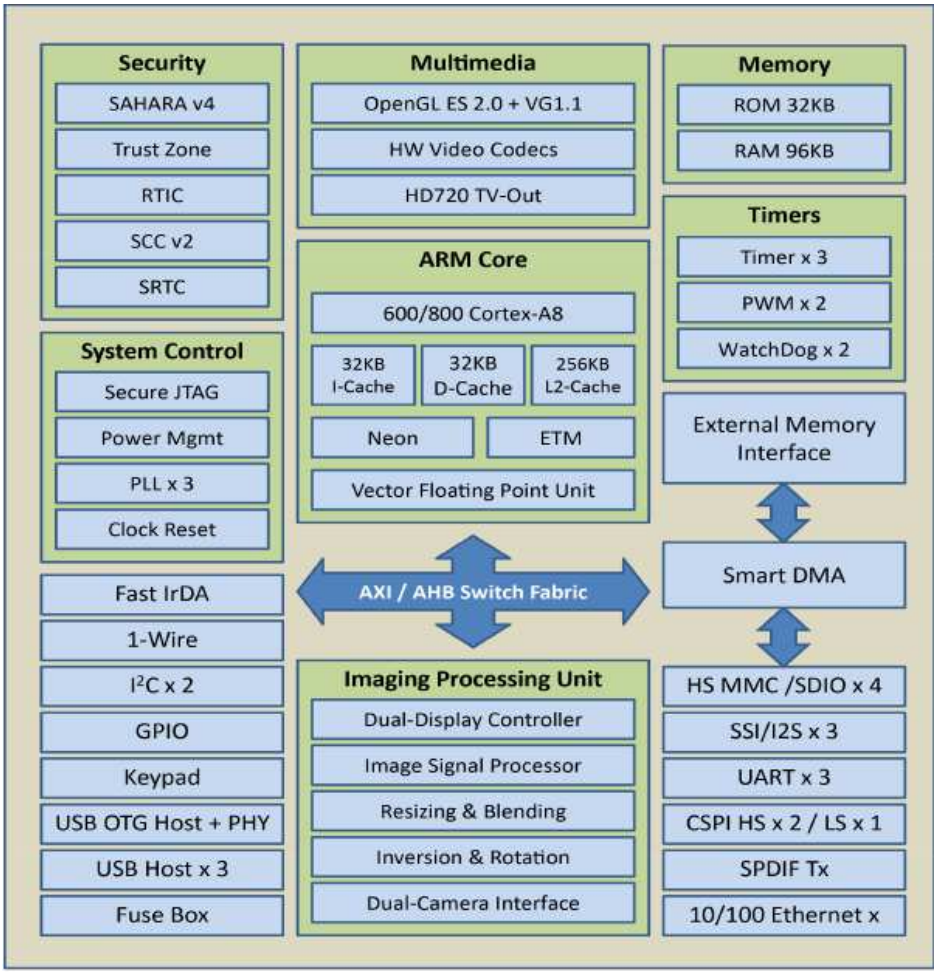
The ConnectCore for i.MX51 module is available with various population options such as network interfaces (Ethernet, wireless local area network [WLAN]), memory (flash, random-access memory [RAM]), processor (speed grade/operating temperature) and others.

Block diagram

The next figures show the block diagram of the Freescale i.MX515 central processing unit (CPU) and the block diagram of the ConnectCore for i.MX51 module.

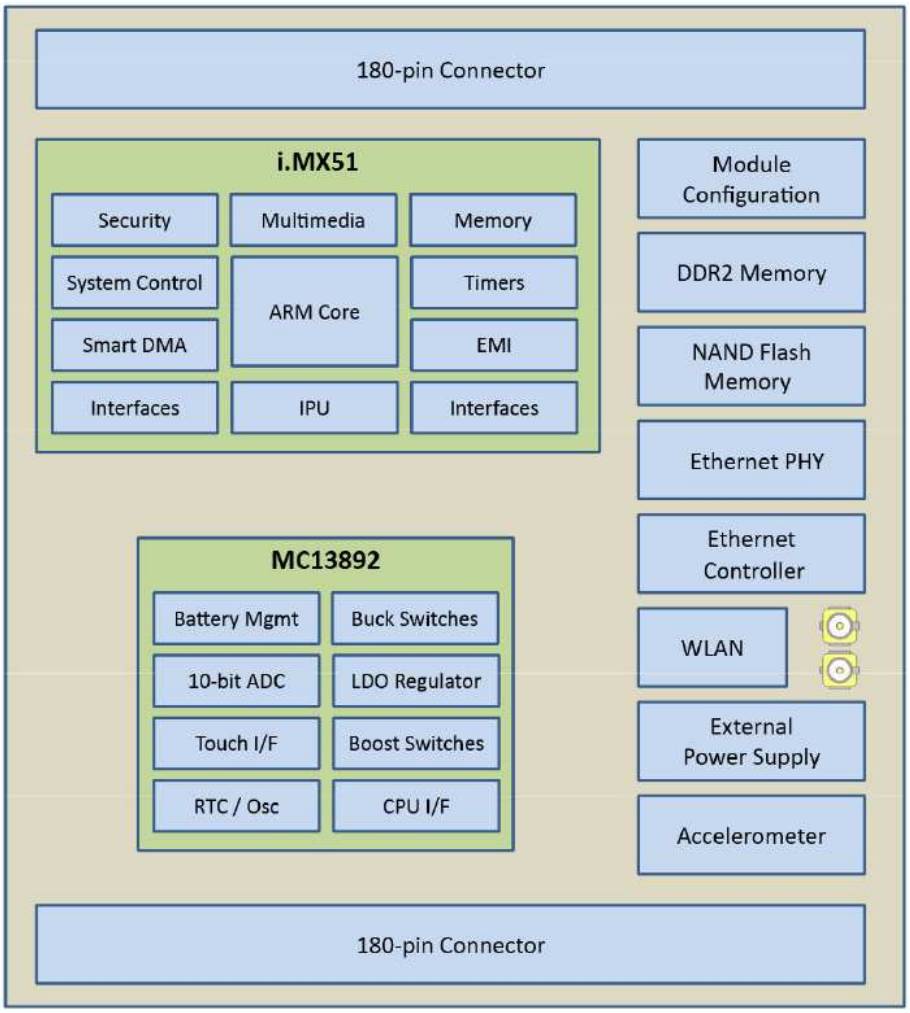
CPU

Freescale i.MX515



Module

ConnectCore I.MX51


180-pin Connector
i.MX51
Security
Multimedia
Memory
System Control
ARM Core
Timers
Smart DMA
EMI
Interfaces
IPU
Interfaces
MC13892
Battery Mgmt
Buck Switches
10-bit ADC
LDO Regulator
Touch I/F
Boost Switches
RTC / Osc
CPU I/F
Module Configuration
DDR2 Memory
NAND Flash Memory
Ethernet PHY
Ethernet Controller
WLAN
External Power Supply
Accelerometer
180-pin Connector

Module pinout

The module has two 180-pin connectors, J1 and J2. The following tables describe each pin, its properties, and its use on the module and development board. The DC parameters for each I/O type are defined in the I/O DC parameters.

The “Use on module” column shows the connection of the signals on the module. The format of this column is “component: pad_name,” where “component” is the chip where the signals are connected, and “pad_name” is the name of the pad where the signals are connected as they are defined in the component’s datasheet.

Pinout legend

I	Input
O	Output
IO	Input or output
P	Power
#	Low level active signal

Pinout definitions

GPIO - General Purpose IO

UHVIO - Ultra High Voltage IO

HSGPIO - High Speed GPIO

LVIO - Low Voltage IO (meaning 1.8V)

The I/O Type descriptions can be read as follows:

- 18 - 1.8V logic level switching (for example, GPIO18)
- 27 - 2.775V logic level switching (for example, GPIO27)
- 31 - 3.15V logic level switching (for example, UHVIO31)
- 33 - 3.3V logic level switching (for example, UHVIO33)

J1 pinout

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:1	GPIO27	CSI1_D8/GPIO3_12	i.MX51: CSI1_D8	Not used	
J1:2	GPIO27	CSI1_D9/GPIO3_13	i.MX51: CSI1_D9	Camera 1 reset	
J1:3	HSGPIO27	CSI1_D10	i.MX51: CSI1_D10	Camera 1 data	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:4	HSGPIO27	CSI1_D11	i.MX51: CSI1_D11	Camera 1 data	
J1:5	HSGPIO27	CSI1_D12	i.MX51: CSI1_D12	Camera 1 data	
J1:6	HSGPIO27	CSI1_D13	i.MX51: CSI1_D13	Camera 1 data	
J1:7	HSGPIO27	CSI1_D14	i.MX51: CSI1_D14	Camera 1 data	
J1:8	HSGPIO27	CSI1_D15	i.MX51: CSI1_D15	Camera 1 data	
J1:9	HSGPIO27	CSI1_D16	i.MX51: CSI1_D16	Camera 1 data	
J1:10	HSGPIO27	CSI1_D17	i.MX51: CSI1_D17	Camera 1 data	
J1:11	HSGPIO27	CSI1_D18	i.MX51: CSI1_D18	Camera 1 data	
J1:12	HSGPIO27	CSI1_D19	i.MX51: CSI1_D19	Camera 1 data	
J1:13	GPIO27	CSI1_VSYNC/GPIO3_14	i.MX51: CSI1_VSYNC	Camera 1 vertical synchronization	
J1:14	GPIO27	CSI1_HSYNC/GPIO3_15	i.MX51: CSI1_HSYNC	Camera 1 horizontal synchronization	
J1:15	GPIO27	CSI1_PIXCLK	i.MX51: CSI1_PIXCLK	Camera 1 pixel clock	
J1:16	GPIO27	CSI1_MCLK	i.MX51: CSI1_MCLK	Camera 1 and 2 Master clock	
J1:17	-	GND	-	-	
J1:18	-	GND	-	-	
J1:19	WLAN	WLAN_TDO	WLAN: TDO	Not used	
J1:20	WLAN	WLAN_TCK	WLAN: TCK	Not used	
J1:21	WLAN	WLAN_TDI	WLAN: TDI	Not used	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:22	WLAN	WLAN_TMS	WLAN: TMS	Not used	
J1:23	WLAN	WLAN_LED	WLAN: LED_ON	WLAN light-emitting diode (LED)	
J1:24	WLAN	RS_BT_PRIORITY	WLAN: BT_ PRIORITY	Not used	
J1:25	WLAN	RS_WLAN_ACTIVE	WLAN: WLAN_ ACTIVE	Not used	
J1:26	WLAN	RS_BT_ACTIVE	WLAN: BT_ACTIVE	Not used	
J1:27	LVIO	BOOT_MODE0	i.MX51: BOOT_ MODE0	Boot Mode selection	Boot configuratio n not available in EA Kit
J1:28	GPIO33	WLAN_DISABLE#	WLAN Power Supply Switch	WLAN Disable Jumper (J17)	This signal switch ON/OFF the supply of WLAN
J1:29	LVIO	BOOT_MODE1	i.MX51: BOOT_ MODE1	Boot Mode selection	Boot configuratio n not available in EA Kit
J1:30	-	VLIO	MC13892: BATT	Battery supply	
J1:31	-	VLIO	MC13892: BATT	Battery supply	
J1:32	-	VCHRG	MC13892: CHRGRAW	Charger supply	
J1:33	-	+2.775V	-	-	
J1:34	-	VCHRG	MC13892: CHRGRAW	Charger supply	
J1:35	-	+2.775V	-	-	
J1:36	-	+2.775V	-	-	
J1:37	PMIC_ GPO	MC13892_GPO1	MC13892: GPO1	Reserved	
J1:38	-	+2.775V	-	-	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:39	PMIC_ PWRON	PMIC_PWRON1	MC13892: PWRON1	Connected to Power Button (S11)	Suspend / Wake-up button
J1:40	PMIC_ STDBY	PMIC_STDBY_REQ	i.MX51: PMIC_ STBY_REQ MC13892: STANDBY	Reserved	Output from i.MX51 to put MC13892 in low power mode
J1:41	PMIC_ INT	PMIC_INT_REQ	i.MX51: PMIC_INT_ REQ	Reserved	This high-priority interrupt input on i.MX51 is not used. The output interrupt from PMIC is connected to standard interrupt GPIO_5 on i.MX51.
J1:42	PMIC_ PWGTDRV	PWRGTDRV1	MC13892: PWRGTDRV1	Not used	
J1:43	PMIC_ LED	CHRGLED	MC13892: CHRGLED	Battery Charging LED	
J1:44	PMIC_ PWGTDRV	PWRGTDRV2	MC13892: PWRGTDRV2 +3.3V_REG: ENABLE	Not used	Used on module to enable / disable the +3.3V supply
J1:45	PMIC_SE	CHRGSE1#	MC13892: CHRGSE1#	Charger detection circuit	This circuit is needed to boot from charger
J1:46	-	VCC_COINCELL	MC13892: LICELL	Coincell voltage	
J1:47	-	VLIO	MC13892: BATT	Battery supply	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:48	-	VCHRG	MC13892: CHRGRAW	Charger supply	
J1:49	-	VLIO	MC13892: BATT	Battery supply	
J1:50	-	VCHRG	MC13892:CHRGRAW	Charger supply	
J1:51	-	VLIO	MC13892: BATT	Battery supply	
J1:52	-	VCHRG	MC13892:CHRGRAW	Charger supply	
J1:53	ETH	ETH1_TX+	ETH_PHY: TXP	Ethernet 1 Tx+	
J1:54	ETH	ETH1_RX+	ETH_PHY: RXP	Ethernet 1 Rx+	
J1:55	ETH	ETH1_TX-	ETH_PHY: TXN	Ethernet 1 Tx-	
J1:56	ETH	ETH1_RX-	ETH_PHY: RXN	Ethernet 1 Rx-	
J1:57	-	GND	-	-	
J1:58	GPIO33	ETH1_LINK	ETH_PHY: LED1	Ethernet 1 Link LED	
J1:59	GPIO27	DISPB2_SER_DIN/GPIO3_5	i.MX51: DISPB_2_SER_DIN	GPIO1 signal to LCD connectors	
J1:60	GPIO33	ETH1_ACTIVITY	ETH_PHY: LED2	Ethernet 1 Activity LED	
J1:61	GPIO27	DISPB2_SER_RS/GPIO3_8	i.MX51: DISPB2_SER_RS	USB Host Reset	In Early Availability Kit USB host and Digital IO interface cannot be used at the same time.
J1:62	GPIO27	DISPB2_SER_DIO/GPIO3_6	i.MX51: DISPB2_SER_DIO	User button 1 & Digital IO 7	
J1:63	GPIO27	DISP2_DATA0/MII_RXD3/USBH3_CLK	i.MX51: DISP2_DATA0 ETH_PHY: RXD3	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:64	GPIO27	DISPB2_SER_CLK_ GPIO3_7	i.MX51: DISPB2_ SER_CLK	Camera 2 Reset	
J1:65	HSGPIO2 7	DISP2_DATA2	i.MX51: DISP2_ DATA2	LCD2 Data	
J1:66	GPIO27	DISP2_DATA1/MII_RX_ ER/USBH3_DIR	i.MX51: DISP2_ DATA1 ETH_PHY: RXD4	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:67	HSGPIO2 7	DISP2_DATA4	i.MX51: DISP2_ DATA4	LCD2 Data	
J1:68	HSGPIO2 7	DISP2_DATA3	i.MX51: DISP2_ DATA3	LCD2 Data	
J1:69	GPIO27	DISP2_DATA6/MII_ TXD1/USBH3_STP	i.MX51: DISP2_ DATA6 ETH_PHY: TXD1	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:70	HSGPIO2 7	DISP2_DATA5	i.MX51: DISP2_ DATA5	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:71	GPIO27	DISP2_DATA8/MII_ TXD3/USBH3_DATA0	i.MX51: DISP2_ DATA8 ETH_PHY: TDX3	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:72	GPIO27	DISP2_DATA7/MII_ TXD2/UBH3_NXT	i.MX51: DISP2_ DATA7 ETH_PHY: TDX2	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:73	GPIO27	DISP2_DATA10/MII_ COL/USBH3_DATA2	i.MX51: DISP2_ DATA10 ETH_PHY: COL	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:74	GPIO27	DISP2_DATA9/MII_TXEN/USBH3_DATA1	i.MX51: DISP2_DATA9 ETH_PHY: TXEN	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:75	GPIO27	DISP2_DAT12/MII_RX_DV/USBH3_DATA4	i.MX51: DISP2_DATA12 ETH_PHY: RXDV	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:76	GPIO27	DISP2_DAT11/MII_RX_CLK/USBH3_DATA3	i.MX51: DISP2_DATA11 ETH_PHY: RXCLK	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:77	GPIO27	DISP2_DATA14/MII_RXD0/USBH3_DATA6	i.MX51: DISP2_DATA14 ETH_PHY: RXD0	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:78	GPIO27	DISP2_DAT13/MII_TX_CLK/USBH3_DATA5	i.MX51: DISP2_DATA13 ETH_PHY: TXCLK	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:79	GPIO27	DI2_PIN2/MII_MDC	i.MX51: DI2_PIN2 ETH_PHY: MDC	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:80	GPIO27	DISP2_DAT15/MII_TXD0/USBH3_DATA7	i.MX51: DISP2_DATA15 ETH_PHY: TXD0	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:81	GPIO27	DI2_PIN4/MII_CRS	i.MX51: DI2_PIN4 ETH_PHY: CRS	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:82	-	GND	-	-	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:83	RGB	IOR	i.MX51: IOR	Not used	
J1:84	GPIO27	DI2_DISP_CLK/MII_RXD1	i.MX51: DI2_DISP_CLK ETH_PHY: RXD1	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:85	RGB	IOR_BACK	i.MX51: IOR_BACK	Not used	
J1:86	GPIO27	DI2_PIN3/MII_MDIO	i.MX51: DI2_PIN3 ETH_PHY: MDIO	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:87	RGB	IOB	i.MX51: IOB	Not useD	
J1:88	IOG	IOG	i.MX51: IOG	Not used	
J1:89	RGB	IOB_BACK	i.MX51: IOB_BACK	Not used	
J1:90	RGB	IOG_BACK	i.MX51: IOG_BACK	Not used	
J1:91	GPIO18	JTAG_TCK	i.MX51: JTAG_TCK	JTAG Connector	
J1:92	GPIO18	JTAG_TRST#	i.MX51: JTAG_TRST#	JTAG Connector	
J1:93	GPIO18	JTAG_TMS	i.MX51: JTAG_TMS	JTAG Connector	
J1:94	GPIO18	JTAG_MOD#	i.MX51: JTAG_MOD#	JTAG Mod Selection	
J1:95	GPIO18	JTAG_TDI	i.MX51: JTAG_TDI	JTAG Connector	
J1:96	GPIO18	JTAG_DE#	i.MX51: JTAG_DE_B	JTAG Connector	
J1:97	GPIO18	JTAG_TDO	i.MX51: JTAG_TDO	JTAG Connector	
J1:98	LVIO	RESET_IN#	i.MX51: RESET_IN_B MC13892: RESETB	Not used	Warm reset input to i.MX51.

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:99	LVIO	POR#	i.MX51: POR_B MC13892: RESETBMCU	LCD 1 & 2 Reset, JTAG Connector and Reset Button (S4)	Cold reset input to i.MX51. Used to reset the module and peripherals on the Dev. Kit.
J1:100	-	+1.8V		-	
J1:101	-	GND		-	
J1:102	-	GND		-	
J1:103	ETH	ETH2_TX+/ETH2_DA+	ETH_CTRL: TPO+	Ethernet 2 Tx+	
J1:104	ETH	ETH2_RX+/ETH2_DB+	ETH_CTRL: TPI+	Ethernet 2 Rx+	
J1:105	ETH	ETH2_TX-/ETH2_DA-	ETH_CTRL: TPO-	Ethernet 2 Tx-	
J1:106	ETH	ETH2_RX-/ETH2_DB-	ETH_CTRL: TPI-	Ethernet 2 Rx-	
J1:107	-	-	-	-	-
J1:108	-	-	-	-	-
J1:109	-	-	-	-	-
J1:110	-	-	-	-	-
J1:111	GPIO33	ETH2_ACTIVITY#	ETH_CTRL: GPIO1/LED2#	Ethernet 2 Activity LED	
J1:112	GPIO33	ETH2_LINK#	ETH_CTRL: GPIO0/LED1#	Ethernet 2 Link LED	
J1:113	GPIO18	EIM_CS0/GPIO2_25	i.MX51: EIM_CS0	Peripheral Application Chip Select	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:114	GPIO18	EIM_CS1/GPIO2_26	i.MX51: EIM_CS1	Not used	
J1:115	GPIO18	EIM_CS2/GPIO2_27/FEC_RDATA2/SISG5/CSI1_D4/AUD5_TXD	i.MX51: EIM_CS2	Not used	
J1:116	GPIO18	EIM_CS3/GPIO2_28/FEC_RDATA3/SSI_EXT2_CLK/CSI1_D5/AUD5_RXD	i.MX51: EIM_CS3	Not used	
J1:117	GPIO18	EIM_CS4/GPIO2_29/FEC_RX_ER/SSI_EXT1_CLK/CSI1_D6/AUD5_TXC	i.MX51: EIM_CS4	Not used	
J1:118	GPIO18	EIM_CS5/GPIO2_30/FEC_CRS/DI1_EXT_CLK/CSI1_D7/AUD5_TXFS	i.MX51: EIM_CS4 EHT_CTRL: CS#	Reserved	
J1:119	GPIO18	EIM_DTACK/GPIO2_31	i.MX51: EIM_DTACK	Not used	
J1:120	GPIO18	EIM_LBA/GPIO3_1	i.MX51: EIM_LBA	Not used	
J1:121	GPIO18	EIM_DA0/TRACE16	i.MX51: EIM_DA0 ETH_CTRL: A1	Peripheral Application Data / Address	
J1:122	GPIO18	EIM_DA1/TRACE17	i.MX51: EIM_DA1 ETH_CTRL: A2	Peripheral Application Data / Address	
J1:123	GPIO18	EIM_DA2/TRACE18	i.MX51: EIM_DA2 ETH_CTRL: A3	Peripheral Application Data / Address	
J1:124	GPIO18	EIM_DA3/TRACE19	i.MX51: EIM_DA3 ETH_CTRL: A4	Peripheral Application Data / Address	
J1:125	-	GND	-	-	
J1:126	GPIO18	EIM_DA5/TRACE21	i.MX51: EIM_DA5 ETH_CTRL: A6	Peripheral Application Data / Address	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:127	GPIO18	EIM_DA4/TRACE20	i.MX51: EIM_DA4 ETH_CTRL: A5	Peripheral Application Data / Address	
J1:128	GPIO18	EIM_DA7/TRACE23	i.MX51: EIM_DA7 ETH_CTRL: FIFO_SEL	Peripheral Application Data / Address	
J1:129	GPIO18	EIM_DA6/TRACE22	i.MX51: EIM_DA6 ETH_CTRL: A7	Peripheral Application Data / Address	
J1:130	-	GND	-	-	
J1:131	GPIO18	EIM_DA8/TRACE24	i.MX51: EIM_DA8	Peripheral Application Data / Address	
J1:132	GPIO18	EIM_DA9/TRACE25	i.MX51: EIM_DA9	Peripheral Application Data / Address	
J1:133	GPIO18	EIM_DA10/TRACE26	i.MX51: EIM_DA10	Not used	
J1:134	GPIO18	EIM_DA11/TRACE27	i.MX51: EIM_DA11	Not used	
J1:135	-	GND	-	-	
J1:136	GPIO18	EIM_DA13/TRACE29	i.MX51: EIM_DA13	Not used	
J1:137	GPIO18	EIM_DA12/TRACE28	i.MX51: EIM_DA12	Not used	
J1:138	GPIO18	EIM_DA15/TRACE31	i.MX51: EIM_DA15	Not used	
J1:139	GPIO18	EIM_DA14/TRACE30	i.MX51: EIM_DA14	Not used	
J1:140	-	GND	-	-	
J1:141	GPIO18	EIM_D16/GPIO2_0/USBH2_DATA0/UART2_CTS#/I2C1_SDA/AUD4_RXFS/TRACE0/AUD5_TXD	i.MX51: EIM_D16 ETH_CTRL: D0	Peripheral Application Data	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:142	GPIO18	EIM_D17/GPIO2_1/USBH2_DATA1/UART2_RXD/UART3_CTS#/SISG4/TRACE1/AUD5_RXD	i.MX51: EIM_D17 ETH_CTRL: D1	Peripheral Application Data	
J1:143	GPIO18	EIM_D18/GPIO2_2/USBH2_DATA2/UART2_TXD/UART3_RTS#/SISG5/TRACE2/AUD5_TXC	i.MX51: EIM_D18 ETH_CTRL: D2	Peripheral Application Data	
J1:144	GPIO18	EIM_D19/GPIO2_3/USBH2_DATA3/UART2_RTS#/I2C1_SCL/AUD4_RXC/TRACE3/AUD5_TXFS	i.MX51: EIM_D19 ETH_CTRL: D3	Peripheral Application Data	
J1:145	-	+3.15V	-	-	
J1:146	GPIO18	EIM_D21/GPIO2_5/USBH2_DATA5/AUD4_RXD/TRACE5	i.MX51: EIM_D21 ETH_CTRL: D5	Peripheral Application Data	
J1:147	GPIO18	EIM_D20/GPIO2_4/USBH2_DATA4/AUD4_TXD/TRACE4	i.MX51: EIM_D20 ETH_CTRL: D4	Peripheral Application Data	
J1:148	GPIO18	EIM_D23/GPIO2_7/USBH2_DATA7/SPDIF_OUT1/AUD4_TXFS/TRACE7	i.MX51: EIM_D23 ETH_CTRL: D7	Peripheral Application Data	
J1:149	GPIO18	EIM_D22/GPIO2_6/USBH2_DATA6/AUD4_TXC/TRACE6	i.MX51: EIM_D22 ETH_CTRL: D8	Peripheral Application Data	
J1:150	-	GND	-	-	
J1:151	GPIO18	EIM_D24/GPIO2_8/UART3_CTS#/I2C2_SDA/AUD6_RXFS/TRACE8	i.MX51: EIM_D24 ETH_CTRL: D8	Peripheral Application Data	
J1:152	GPIO18	EIM_D25/KEY_COL6/UART3_RXD/UART2_CTS#/CMPOUT1/TRACE9	i.MX51: EIM_D25 ETH_CTRL: D9	Peripheral Application Data	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:153	GPIO18	EIM_D26/KEY_COL7/UART3_TXD/UART2_RTS#/CMPOUT2/TRACE10	i.MX51: EIM_D26 ETH_CTRL: D10	Peripheral Application Data	
J1:154	GPIO18	EIM_D27/GPIO2_9/UART3_RTS#/I2C2_SCL/AUD6_RXC/TRACE11	i.MX51: EIM_D27 ETH_CTRL: D11	Peripheral Application Data	
J1:155	-	GND	-	-	
J1:156	GPIO18	EIM_D29/KEY_ROW5/SISG1/AUD6_RXD/TRACE13	i.MX51: EIM_D29 ETH_CTRL: D13	Peripheral Application Data	
J1:157	GPIO18	EIM_D28/KEY_ROW4/SISG0/AUD6_TXD/TRACE12	i.MX51: EIM_D28 ETH_CTRL: D12	Peripheral Application Data	
J1:158	GPIO18	EIM_D31/KEY_ROW7/SISG03/AUD6_TXFS/TRACE15	i.MX51: EIM_D31 ETH_CTRL: D15	Peripheral Application Data	
J1:159	GPIO18	EIM_D30/KEY_ROW6/SISG2/AUD6_TXC/TRACE14	i.MX51: EIM_D30 ETH_CTRL: D14	Peripheral Application Data	
J1:160	GPIO18	EIM_A17/GPIO2_11	i.MX51: EIM_A17	Not used	
J1:161	GPIO18	EIM_A16/GPIO2_10	i.MX51: EIM_A16	Not used	
J1:162	GPIO18	EIM_A19/GPIO2_13	i.MX51: EIM_A19	Not used	
J1:163	GPIO18	EIM_A18/GPIO2_12	i.MX51: EIM_A18	Not used	
J1:164	GPIO18	EIM_A21/GPIO2_15	i.MX51: EIM_A21	Boot Configuration Switch	
J1:165	GPIO18	EIM_A20/GPIO2_14	i.MX51: EIM_A20	Boot Configuration Switch	
J1:166	GPIO18	EIM_A23/GPIO2_17	i.MX51: EIM_A23	Not used	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:167	GPIO18	EIM_A22/GPIO2_16	i.MX51: EIM_A22	Not used	
J1:168	GPIO18	EIM_A25/GPIO2_19/USBH2_DIR/DI1_PIN4	i.MX51: EIM_A25	Not used	
J1:169	GPIO18	EIM_A24/GPIO2_18/USBH2_CLK	i.MX51: EIM_A24	Not used	
J1:170	GPIO18	EIM_A27/GPIO2_21/USBH2_NXT/SISG1/CSI2_DATA_EN/DI1_PIN1	i.MX51: EIM_A27	XBEE_SLEEP_RQ	
J1:171	GPIO18	EIM_A26/GPIO2_20/USBH2_STP/SISG0/CSI1_DATA_EN/DI2_EXT_CLK	i.MX51: EIM_A26	Not used	
J1:172	GPIO18	EIM_OE#/GPIO2_24	i.MX51: EIM_OE ETH_CTRL: RD#	Peripheral Application Output Enable	
J1:173	GPIO18	EIM_EB0	i.MX51: EIM_EB0	Not used	
J1:174	GPIO18	EIM_RW#	i.MX51: EIM_RW ETH_CTRL: WR#	Peripheral Application Read / Write	
J1:175	GPIO18	EIM_EB1	i.MX51: EIM_EB1	Not used	
J1:176	GPIO18	EIM_CRE/GPIO3_2	i.MX51: EIM_CRE	Peripheral Application Interrupt input	
J1:177	GPIO18	EIM_EB2/GPIO2_22/TRCTL/FEC_MDIO/SISG2/CSI1_D2/AUD5_RXFS/CMPOUT1	i.MX51: EIM_EB2	Peripheral Application Byte Enable 2	
J1:178	GPIO18	EIM_WAIT	i.MX51: EIM_WAIT	Not used	
J1:179	GPIO18	EIM_EB3/GPIO2_23/TRCLK/FEC_RDATA1/SISG3/CSI1_D3/AUD5_RXC/CMPOUT2	i.MX51: EIM_EB3	Peripheral Application Byte Enable 3	