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Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

#### **RoHS Compliant**



#### **Applications**

- Wide band power amplifier
- Broadcast systems
- Lasers
- Acoustic noise sensitive systems
- LED signage

### Description

The CC3500AC52FB Rectifier has an extremely wide programmable output voltage capability. Featuring high-density, fully enclosed, conduction-cooled packaging, it is designed for minimal space utilization and is highly expandable for future growth. This standard rectifier incorporates both RS485 and dual-redundant I<sup>2</sup>C communications busses that allow it to be used in a broad range of applications. Feature-set flexibility makes this rectifier an excellent choice for applications requiring operation over a wide output-voltage range.

#### <sup>1</sup> At output voltages exceeding 52V<sub>DC</sub>

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#### **Features**

- Efficiency exceeding 96%<sup>1</sup> (meets 80+ Titanium)
- Compact 1RU form factor with 40 W/in<sup>3</sup> density
- 3500W from nominal 200-240V<sub>AC</sub> up to 50°C case
- 1500W from nominal 100 120V<sub>AC</sub> for  $V_0 > 52V_{DC}$
- Output voltage programmable from  $18V 58V_{DC}$
- ON/OFF control of the main output
- Comprehensive input, output and overtemp. protection
- PMBus compliant dual I<sup>2</sup>C serial bus and RS485
- Precision measurement reporting such as input power consumption, input/output voltage & current
- Remote firmware upgrade capable
- Power factor correction (meets EN/IEC 61000-3-2 and EN 60555-2 requirements)
- Redundant, parallel operation with active load sharing
- Redundant +5V @ 2A Aux power
- Completely enclosed, conduction cooled
- Hot insertion/removal (hot plug)
- Four front panel LED indicators
- UL\* Recognized, CAN/ CSA<sup>†</sup> C22.2 specified compliance with IEC60950-1
- CE mark meets 2006/95/EC directive§

UL is a registered trademark of Underwriters Laboratories, Inc. CSA is a registered trademark of Canadian Standards Association.

VDE is a trademark of Verband Deutscher Elektrotechniker e.V.
This product is intended for integration into end-user equipment. All CE marking procedures of end-user equipment should be followed. (The CE mark is placed on selected products.)
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<sup>\*\*</sup> ISO is a registered trademark of the International Organization of Standards \* The PMBus name and logo are registered trademarks of the System Management Interface Forum (SMIF)

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

#### **Absolute Maximum Ratings**

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

Parameter	Symbol	Min	Max	Unit
Input Voltage: Continuous	VIN	0	264	V <sub>AC</sub>
Operating Case Temperature (sink side) <sup>2</sup>	Tc	-40	75 <sup>24</sup>	°C
Storage Temperature	T <sub>stg</sub>	-40	85	°C

### **Electrical Specifications**

Unless otherwise indicated, specifications apply overall operating input voltage,  $Vo=52V_{DC}$ , resistive load, and temperature conditions.

INPUT					
Parameter	Symbol	Min	Тур	Max	Unit
Startup Voltage Low-line Operation High-line Operation		80	85	90 185	
Operating Voltage Range Low-line Configuration High-line Configuration	Vin	90 185	100 - 120 200 - 240	140 265	V <sub>AC</sub>
Voltage Swell (no damage)		275			
Turn OFF Voltage Hysteresis		75 5	80	85	
Frequency	FIN	47		66	Hz
Source Impedance (NEC allows 2.5% of source voltage drop inside a building)			0.2		Ω
Operating Current; at 110V <sub>AC</sub> at 240V <sub>AC</sub>	l <sub>in</sub>		15.5 16		A <sub>AC</sub>
Inrush Transient (220 $V_{RMS}$ , 25°C, excluding X-Capacitor charging)	I <sub>IN</sub>		25	40	A <sub>PK</sub>
Idle Power (at 240V <sub>AC</sub> , 25°C) 52V OFF 52V ON @ Io=0	P <sub>IN</sub>		9 18		W
Leakage Current (265V <sub>AC</sub> , 60Hz)	l <sub>iN</sub>		2.5	3.5	mA
Power Factor (50 – 100% load)	PF	0.97	0.995		
Efficiency <sup>3</sup> , 240V <sub>AC</sub> , 52V <sub>DC</sub> , @ 25°C 10% of FL 20% of FL 50% of FL FL	η	90 94 96 91			%
Holdup time (output allowed to decay down to 40V <sub>DC</sub> ) For loads below 1500W	Т		10 15		ms
Ride through (at 240V <sub>AC</sub> , 25°C)	Т	1/2	1		cycle
Power Good Warning <sup>4</sup> (main output allowed to decay to $40V_{DC}$ )	PG	3	5		ms
Isolation (per EN60950) (consult factory for testing to this requirement) Input to Chassis & Signals Input to Output	V	1500 3000			V <sub>AC</sub> V <sub>AC</sub>

<sup>&</sup>lt;sup>2</sup> See the derating guidelines under the Environmental Specifications section

<sup>&</sup>lt;sup>3</sup> 5V output at 0A load.

<sup>&</sup>lt;sup>4</sup> Internal protection circuits may override the PG signal and may trigger an immediate shutdown. PG should not indicate normal (HI) until the main output is within regulation. PG should be asserted if the main output is about to shut down for any detectible reason.

<sup>&</sup>lt;sup>24</sup> From 50°C-75°C see derating guidelines

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

## **Electrical Specifications (continued)**

Parameter	Symbol	Min	Тур	Max	Unit
Output Power <sup>5</sup> @ low line input 100 – $120V_{AC}$ , $T_C < 50^{\circ}C$ @ high line input 200 – $240V_{AC}^{6}$ , $V_0 > 42V_{DC}$ , $T_C < 50^{\circ}C$	w	1500 3500			W <sub>DC</sub>
Factory set default set point			52		V <sub>DC</sub>
Overall regulation (load, temperature, aging) 0 - 45°C LOAD > 2.5A > 45°C	Vout	-1 -2		+1 +2	%
Output Voltage Set Range		18		58 <sup>(9)</sup>	V <sub>DC</sub>
Response to a voltage change command	Т		400	500	ms
Output Current - @ 1500W (100 – 120Vac), Vo>=52V @ 3500W (200 – 240V <sub>AC</sub> ), Vo>=52V	lout	1 1		28.3/28.9 66/67.3	A <sub>DC</sub>
Current Share ( $> 50\%$ FL) V <sub>0</sub> > 42V <sub>DC</sub> V <sub>0</sub> < 42V <sub>DC</sub>		-5 -10		5 10	%FL
Output Ripple ( 20MHz bandwidth, load > 1A) RMS (5Hz to 20MHz) Peak-to-Peak (5Hz to 20MHz)	Vout			100 500	mV <sub>rms</sub> mV <sub>p-p</sub>
External Bulk Load Capacitance	Соит	0		5,000	μF
Turn-On (monotonic turn-ON from 30 – 100% of Vnom above 5°C) Delay Rise Time – PMBus mode Rise Time - RS-485 mode <sup>7</sup>	Т		5 100 5		s ms s
Output Overshoot	Vout			2	%
Load Step Response ( $I_{O,START} > 2.5A$ ) $\Delta I^{B}$ $\Delta V$ , Response Time	Ιουτ Vouτ T		2.0 2	50	%FL V <sub>DC</sub> ms
Permissible Power limit , high line (down to $52V_{DC}$ )	Роит	3500			W
Load Low line	Роит	1500			W

 $<sup>^5</sup>$  Output power capability is proportional to output voltage setting, see the permissible load boundary  $^6$  Input line range: 90 – 264  $V_{\text{RMS}}$  (±10%)

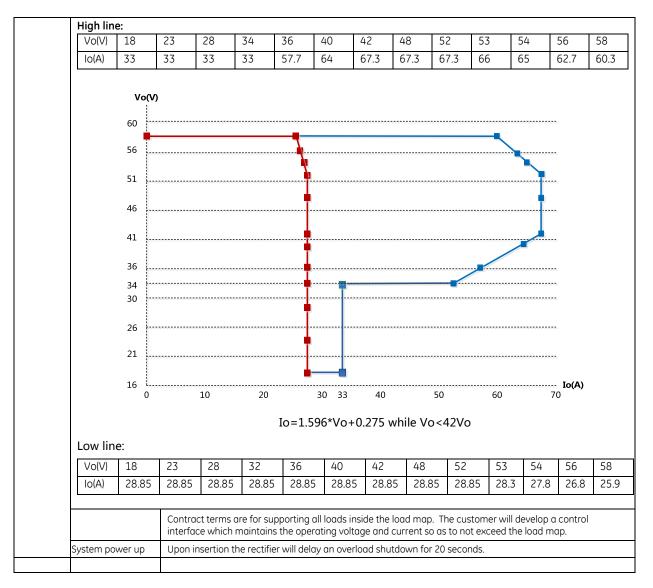
<sup>&</sup>lt;sup>7</sup> Below -5°C, the rise time is approximately 5 minutes to protect the bulk capacitors.

<sup>&</sup>lt;sup>8</sup> di/dt (output current slew rate) 1A/µs.

<sup>&</sup>lt;sup>9</sup> 52 Vdc maximum by trim-pot adjustment. Higher settings require the PMBus Vout\_command to be used.

<sup>&</sup>lt;sup>10</sup> Max output current for -EC & -ES versions is derated for ambient >40°C according to the "Permissible Load Boundary"

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W



## Electrical Specifications (continued)

52VDC MAIN OUTPUT					
Parameter	Symbol	Min	Тур	Max	Unit
Overvoltage - 200ms delayed shutdown Immediate shutdown	Vout	> 60		< 65	V <sub>DC</sub>
Latched shutdown	Three restart attempts are implemented within a 1 minute wi prior to a latched shutdown.				
Over-temperature warning (prior to commencement of shutdown) Shutdown (below the max device rating being protected) Restart attempt Hysteresis (below shutdown level)	т		5 20 10		°C
Isolation Output to Chassis	V	500			V <sub>DC</sub>

5V <sub>DC</sub> Auxiliary output (return is LGND)					
Parameter	Symbol	Min	Тур	Max	Unit
Output Voltage Setpoint	Vout		5		V <sub>DC</sub>

Overall Regulation	-3		+3	%
Output Current	0.005		2	Α
Ripple and Noise (20mHz bandwidth)		50	100	mV <sub>p-p</sub>
Over-voltage Clamp			7	V <sub>DC</sub>
Over-current Limit	110		175	%FL
Isolation LGND to Chassis	100			V <sub>DC</sub>

The  $5V_{DC}$  should be ON before availability of the  $52V_{DC}$  main output and should turn OFF only if insufficient input voltage exists to provide reliable 5V<sub>DC</sub> power. The PG# signal should have indicated a warning that power would get turned OFF and the 52V<sub>DC</sub> main output should be OFF way before interruption of the  $5V_{DC}$  output.

### **General Specifications**

Parameter	Min	Тур	Max	Units	Notes		
Reliability		450,000		Hours	Full load, 25°C ; MTBF per SR232 Reliability protection for electronic equipment, issue 2, method I, case III,		
Service Life		10		Years	At 80% load & 40°C cold plate		
Unpacked Weight		4.5		Kg	CC3500AC52FB-ES/EC		
Packed Weight		5.0		Kg	CC3500AC52FB-ES/EC		
Unpacked Weight		4.1		Kg	CC3500AC52FB		
Packed Weight		4.5		Kg	CC3500AC52FB		
Heat Dissipation190 Watts or 648 BTUs @ 80% load, 250 Watts or 853 BTUs @ 100% load							

## **Signal Specifications**

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions. Signals are referenced to LGND unless noted otherwise. Fault, PG#, OTW, and Alert need to be pulled HI through external pull-up resistors.

Parameter	Symbol	Min	Тур	Max	Unit
ON/OFF Main output OFF	Vout	0.7V <sub>DD</sub>	_	5	V <sub>DC</sub>
52V output ON (should be connected to LGND)	Vout	0	—	0.5	V <sub>DC</sub>
Margining (by adjusting Vprog; see "Voltage programming" section)					
Programmed output voltage range	Vout	<19		58	V <sub>DC</sub>
Linear voltage control range	V <sub>control</sub>	> 0.1		< 3.0	V <sub>DC</sub>
Voltage adjustment resolution (8-bit A/D)	Vcontrol		3.3		mV <sub>DC</sub>
Output set to 52V <sub>DC</sub>	V <sub>control</sub>	3.0		3.3	V <sub>DC</sub>
Output set to 18V <sub>DC</sub>	V <sub>control</sub>	0		0.1	V <sub>DC</sub>
52 – $18V_{DC}$ , settling time to new value	Т		400	600	ms
Interlock	[short pin sł	horted to VOU	T( - ) on system	n side]	
Module Present	[short pin t	o LGND intern	ally]		
Over Temperature Warning (OTW#) Logic HI (temperature normal)	V	0.7V <sub>DD</sub>	—	12	V <sub>DC</sub>
Sink current [note: open collector output FET]	I.		—	5	mA
Logic LO (temperature is too high)	V	0	—	0.4	V <sub>DC</sub>
Power Good (PG) Logic HI (temperature normal)	V	0.7V <sub>DD</sub>	_	12	V <sub>DC</sub>
Sink current [note: open collector output FET]	1			5	mA
Logic LO (temperature is too high)	V	0		0.4	V <sub>DC</sub>
Protocol select Logic HI - Analog/PMBus™ mode	VIH	2.7	_	3.5	V <sub>DC</sub>
Logic – intermediate – RS485 mode	VII	1.0		2.65	V <sub>DC</sub>
Logic LO – DSP reprogram mode	VIL	0	—	0.4	V <sub>DC</sub>
Fault# Logic HI (No fault is present)	V	0.7V <sub>DD</sub>	—	12	V <sub>DC</sub>
Sink current	I	—	—	5	mA
Logic LO (Fault is present)	V	0	—	0.4	V <sub>DC</sub>
Alert# (Alert#_0, Alert#_1) Logic HI (No Alert - normal)	V	0.7V <sub>DD</sub>	—	12	V <sub>DC</sub>
Sink current [note: open collector output FET]	1	—	—	5	mA
Logic LO (Alert# is set)	V	0	—	0.4	V <sub>DC</sub>
SCL, SDA (SCL_0/1, SDA_0/1) Logic HI	V	0.7V <sub>DD</sub>	_	12	V <sub>DC</sub>
Sink current [note: open collector output FET]	1	—	—	5	mA
Logic LO (Alert# is set)	V	0		0.4	V <sub>DC</sub>

### **Digital Interface Specifications**

Min	Тур	Max	Unit
1.5		3.6	V <sub>DC</sub>
0		0.8	VDC
0		10	μΑ
		0.4	V <sub>DC</sub>
3.5			mA
0		10	μΑ
10		400	kHz
•	•		
		25	ms
0		80	A <sub>DC</sub>
-1 5		+1 5	% of FL %
-2		+2	% of FL
0		70	V <sub>DC</sub>
-1		+1	%
0		150	°C
-4		+4	°C
0		320	V <sub>AC</sub>
-1.25 -2		+1.25	%
0		30	I <sub>AC</sub>
-4		+4	% of FL
-2.5 -400		2.5 400	% mA
-400		400	Win
-5		+5	%
-5	35	+3 50	W
-1.5 -2.0 -20	1 1.5 15	+1.5 +2.0 20	% % W
	-2.0	-2.0 1.5	-2.0 1.5 +2.0

 $<sup>^{9}</sup>$  Clock, Data, and Alert# need to be pulled up to  $V_{\mbox{\tiny DD}}$  externally.

<sup>&</sup>lt;sup>10</sup> Below 20% of FL; 10 – 20% of FL: ±0.64A; 5 – 10% of FL: ±0.45A; 2.5 – 5% of FL: ±0.32A.

<sup>&</sup>lt;sup>11</sup> Above 2.5A of load current

<sup>&</sup>lt;sup>12</sup> Within 30° of the default warning and fault levels.

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

### **Environmental Specifications**

Parameter	Min	Тур	Max	Units	Notes
Operating Case Temperature	-4013		50	°C	Measured at the surface that mounted to cold plate and just above the HS_1 and HS2
Storage Temperature	-40		85	°C	
Operating Altitude			5000/16,400	m / ft	
Non-operating Altitude			8200/27,000	m / ft	
Power Derating with Temperature			2	%/°C	50°C - 75°C
Acoustic noise		0		dbA	Full load
Over Temperature Protection		125/110		°C	Shutdown / restart [internally measured points]
Humidity Operating Storage	5 5		95 95	% %	Relative humidity, non-condensing
Shock and Vibration acceleration			2.4	Grms	IPC-9592B, Class II

EMC				
Parameter	Measurement	Standard	Level	Test
	Conducted emissions	EN55022, FCC Docket 20780 part 15, subpart J Meets Telcordia GR1089-CORE by a 3dB margin	A +6dB margin	0.15 – 30MHz
AC input <sup>14</sup>	Radiated emissions	EN55022	A +6dB margin	30 – 10000MHz
	Line harmonics	EN61000-3-2 THD	Table 1 5%	0 – 2 kHz 230 Vac, full load, 25°C
Parameter	Measurement	Standard	Criteria <sup>15</sup>	Test
	Line sags and	EN61000-4-11	В	-30%, 10ms
	interruptions		В	-60%, 100ms
			В	-100%, 5sec
		Output will stay above 40V <sub>DC</sub> @ 75% load		25% line sag for 2 seconds
AC Input Immunity		Sag must be higher than 80Vrms.	A	1 cycle interruption
	Lightning surge	EN61000-4-5, Level 4, 1.2/50µs – error free	А	4kV, common mode
			А	2kV, differential mode
		ANSI C62.41 - level A3	В	6kV, common & differential
	Fast transients	EN61000-4-4, Level 3	В	5/50ns, 2kV (common mode)
	Conducted RF fields	EN61000-4-6, Level 3	А	130dBµV, 0.15-80MHz, 80% AM
Enclosure	Radiated RF fields	EN61000-4-3, Level 3	А	10V/m, 80-1000MHz, 80% AM
immunity		ENV 50140	А	
	ESD	EN61000-4-2, Level 4	В	8kV contact, 15kV air

<sup>&</sup>lt;sup>13</sup> Designed to start and work at an ambient as low as -40°C, but may not meet operational limits until above -5°C

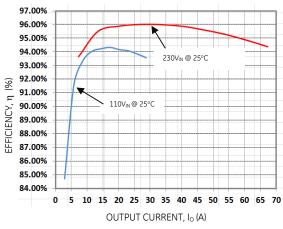
<sup>&</sup>lt;sup>14</sup> Emissions requirements apply to rectifiers with the "-EC" and "-ES" options (which include filters), not the blind-mate-connector version where an external filter must be added to meet these requirements.

<sup>&</sup>lt;sup>15</sup> Criteria A: The product must maintain performance within specification limits. Criteria B: Temporary degradation which is self recoverable. Criteria C: Temporary degradation which requires operator intervention.

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

#### **Characteristic Curves**

The following figures provide typical characteristics for the CC3500AC52TE rectifier and 25°C.



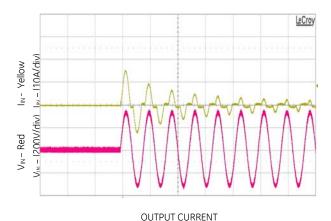


Figure 1. Rectifier Efficiency versus Output Current.

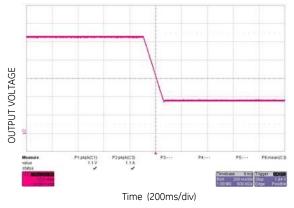
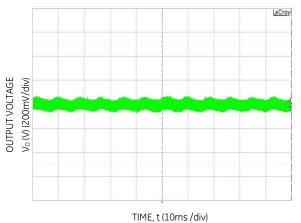


Figure 3. Main output: Output changed from 52V to 18V; commanded via  $\ensuremath{^{2}\text{C}}$  .



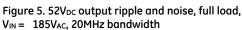


Figure 2. Inrush current  $V_{IN} = 230V_{AC}$ , 0°C phase angle

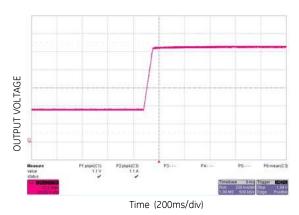
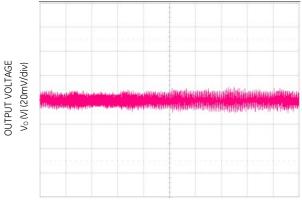
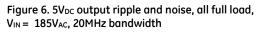


Figure 4. Main output: Output changed from 18V to 52V; commanded via  $\ensuremath{^{2}\text{C}}$  .



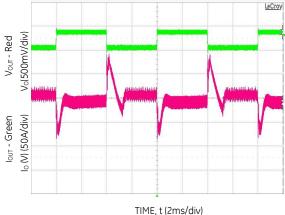
TIME, t (10ms/div)



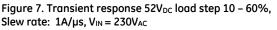
Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

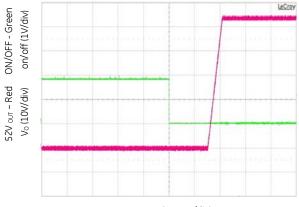
#### **Characteristic Curves (continued)**

The following figures provide typical characteristics for the CC3500AC52TE rectifier and 25°C.









TIME, t (200ms/div)

Figure 9. 52V\_{DC} soft start delay when ON/OFF is asserted,  $V_{\rm IN}{=}230V_{AC}$  -  $1^2C$  mode.

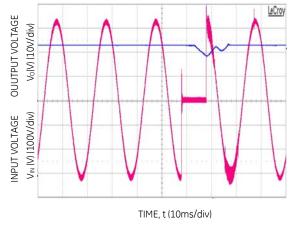
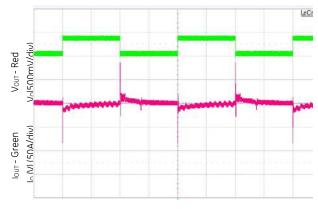
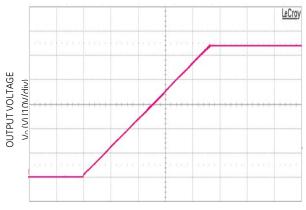


Figure 11. Ride through missing ½ cycle, full load,  $V_{\text{IN}}=~230V_{\text{AC}}.$ 



Time, t (50ms/div)

Figure 8. Transient response  $52V_{DC}$  load step 10 – 60%, Slew rate:  $1A/\mu_S, V_{IN}=230V_{AC}$  .



TIME, t (2s/div)

Figure 10.  $52V_{DC}$  soft start, full load,  $V_{IN} = 230V_{AC} - RS485$  mode with 4700µf external capacitance.

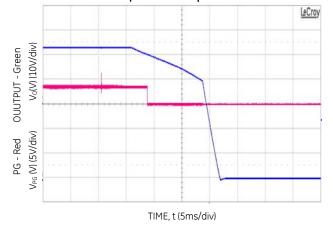
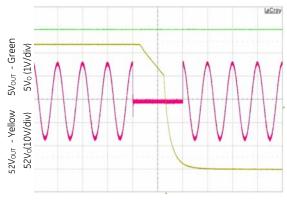


Figure 12. PG# alarmed 10ms prior to Vo < 40V,  $V_{IN} = 230V_{AC}$ , Output at Full load

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

### **Characteristic Curves (continued)**

The following figures provide typical characteristics for the CC3500AC52TE rectifier and 25°C.



TIME, t (20ms/div) Figure 13. 40ms AC dropout @ full load, V<sub>IN</sub> = 230V<sub>AC</sub>.

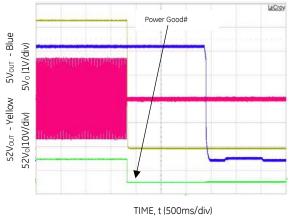
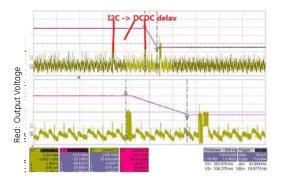


Figure 15. Turn-OFF at full load, VIN=230VAC



Time (100ms/div

Figure 17: Time delay from sending the I<sup>2</sup>C command and executing the output voltage change.

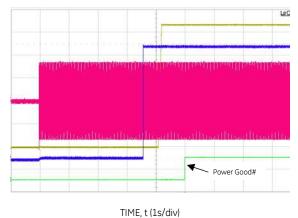
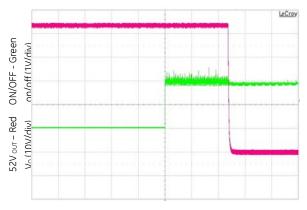


Figure 14. Turn-ON at full load  $V_{IN} = 230V_{AC}$ .



TIME, t (200ms/div)

Figure 16. 52V\_{DC} turn-OFF delay when ON/OFF is diasserted,  $V_{\text{IN}}{=}230V_{\text{AC}}$  -  $\,1^2C$  mode.

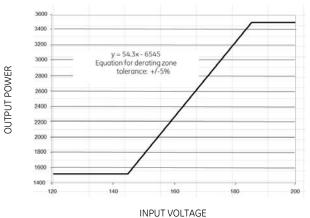
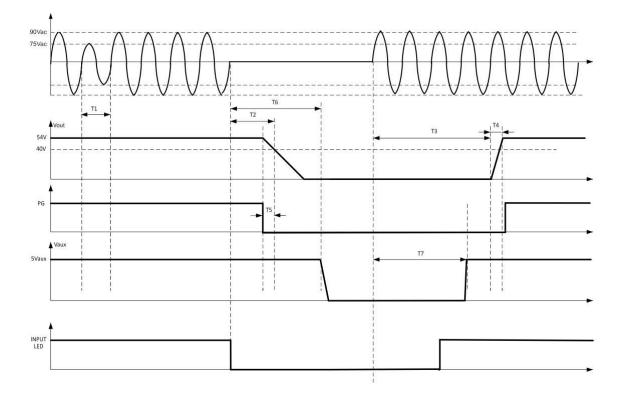


Figure 18. Output power derating below VIN of 185VAC

### Timing diagrams

#### **Response to input fluctuations**



T1 – ride through time – 0.5 to 1 cycles [ 10 - 20ms] V<sub>OUT</sub> remains within regulation – load dependent

T2 – hold up time - 15ms –  $V_{\text{OUT}}$  stays above  $40V_{\text{DC}}$ 

T3 – delay time – 10s – from when the AC returns within regulation to when the output starts rising in I<sup>2</sup>C mode

T4 – rise time - 120ms – the time it takes for  $V_{\text{OUT}}$  to rise from 10% to 90% of regulation in I²C mode

T5 – power good warning – 3ms – the time between assertion of the PG signal and the output decaying below 40V<sub>DC</sub>.

T6 – hold up time of the 5VAUX output @ full load – 1s – from the time AC input failed

T7 – rise time of the 5VAUX output - 3.65ms – 5VAUX is available at least 450ms before the main output is within regulation Blinking of the input/AC LED –  $V_{IN}$  <  $80V_{AC}$  (the low transitioned signal represents blinking of the input LED.

# GE

## CC3500AC52FB Conduction Cooled Wide-Output-Range Rectifier Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

#### **Control and Status**

The Rectifier provides three means for monitor/control: analog, PMBus™, or the GE Galaxy-based RS485 protocol.

Details of analog control and the PMBus™ based protocol are provided in this data sheet. GE will provide separate application notes on the Galaxy RS485 based protocol for users to interface to the rectifier. Contact your local GE representative for details.

**Control hierarchy:** Some features, such as output voltage, can be controlled both through hardware and firmware. For example, the output voltage is controlled both by a signal pin (Vprog) and firmware (Vout\_command, 0x21).

Using output voltage as an example, the Vprog signal pin voltage level sets the output voltage if its value is between 0.1 and 3.0 Vpc (see the "Voltage programming" section). When the programming signal Vprog is either a no-connect (0V) or > 3Vpc, the output voltage is set at the default value of 52Vpc.

The signal pin controls the corresponding feature until the firmware command is executed. Once the firmware command has been executed, the signal pin is ignored until input power is removed and reapplied, which resets control to the signal pin. In the above example, the rectifier will no longer 'listen' to the Vprog pin after Vout\_command has been executed, as long as input power is applied without interruption.

In summary, hardware signals such as Vprog are utilized for setting the initial default value and for varying the value until firmware based control takes over. Once firmware control is executed, hardware based control is relinquished so the processor can clearly decide who has control.

Analog controls: Details of analog controls are provided in this data sheet under Feature Specifications.

Signal Reference: Unless otherwise noted, all signals are referenced to LGND ("Logic Ground"). See the Signal Definitions Table at the end of this document for further description of all the signals.

LGND is isolated from the main output of the rectifier for PMBus communications. Communications and the 5V standby output are not connected to main power return (Vout(-)) and can be tied to the system digital ground point selected by the user. (Note that RS485 communications is referenced to Vout(-), main power return of the rectifier).

LGND is capacitively coupled to Earth Ground inside the rectifier where Earth Ground is also wired to the metal case). The maximum voltage differential between LGND and Earth Ground should be less than 100V<sub>DC</sub>.

Delayed overcurrent shutdown during startup: Rectifiers are programmed to stay in a constant current state for up to 20 seconds during power up. This delay has been introduced to permit the orderly application of input power to a subset of paralleled front-ends during power up. If the overload persists beyond the 20 second delay, the front-end will revert back into its programmed state of overload protection. Unit in Power Limit or in Current Limit: When output voltage is >  $10V_{DC}$  the Output LED will continue blinking. When output voltage is <  $10V_{DC}$ , if the unit is in the RESTART mode, it goes into hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output LED is OFF.

When the unit is in latched shutdown the output LED is OFF.

Auto restart: Auto-restart is the default configuration for over-current and over-temperature shutdowns. These features are configured by the **PMBus™** fault\_response commands

An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again.

Restart after a latchoff: PMBus™ fault\_response commands can be configured to direct the rectifier to remain latched off for over\_temperature and over\_current.

To restart after a latch off either of five restart mechanisms are available.

- 1. The hardware pin **ON/OFF** may be cycled OFF and then ON.
- 2. The unit may be commanded to restart via i2c through the *Operation* command by cycling the output OFF followed by ON.
- 3. Remove and reinsert the unit.
- 4. Turn OFF and then turn ON AC power to the unit.
- 5. Changing firmware from latch off to restart.

Each of these commands must keep the rectifier in the OFF state for at least 2 seconds, with the exception of changing to **restart**.

A successful restart shall clear all alarm registers, set the **restarted successful** bit of the **Status\_2** register.

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all rectifiers,

 Toggling Off and then ON the ON/OFF (ENABLE) signal
Removing and reapplying input commercial power to the entire system.

The rectifiers should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

## **Control Signals**

**Protocol:** This signal pin defines the communications mode setting of the rectifier. Two different states can be configured: State #1 is "Analog/PMBus" mode (I<sup>2</sup>C) for which the protocol pin should be left a no-connect. State #2 is the

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

RS485 mode for which a resistor value between  $1k\Omega$  and  $5k\Omega$  should be present between this pin and Vout ( - ).

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**Device address in I<sup>2</sup>C mode:** Address bits A3, A2, A1, A0 set the specific address of the  $\mu$ P in the rectifier. With these four bits, up to sixteen (16) rectifiers can be independently addressed on a single I<sup>2</sup>C bus. These four bits are configured by two signal pins, Unit\_ID and Rack\_ID. The least significant bit x (LSB) of the address byte is set to either write [0] or read [1]. A write command instructs the rectifier. A read command accesses information from the rectifier.

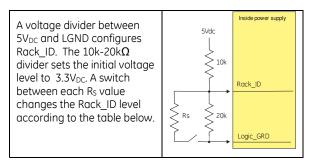
Device	Address	Address Bit Assignments (Most to Least Significant)									
		7	6	5	4	3	2	1	0		
μP	40 – 4F	1	0	0	A3	A2	A1	A0	R/W		
Broadcast	00	0	0	0	0	0	0	0	0		
ARA <sup>16</sup>	С	0	0	0	1	1	0	0	1		
		MS	SΒ						LSB		

Unit\_ID: Up to 10 different units are selectable.

A voltage divider between 3.3V and LGND configures Unit_ID. Internally a 10k $\Omega$ resistor is pulled up to 3.3VDC. A pull down resistor Rs needs to be connected between pin Unit_ID and LGND.	Rs	Inside power supply 3.3Vdc
	$\leq$	Logic_GRD

Unit_ID	Voltage level	Rs (± 0.1%)				
Invalid	3.30					
1	3.00	100k				
2	2.67	45.3k				
3	2.34	24.9k				
4	2.01	15.4k				
5	1.68	10.5k				
6	1.35	7.15k				
7	1.02	4.99k				
8	0.69	2.49k				
9	0.36	1.27k				
10	0	0				

Rack\_ID: Up to 8 different combinations are selectable.



 $<sup>^{\</sup>rm 16}$  Implement if feasible, this is a 'read' only address

# GE

## CC3500AC52FB Conduction Cooled Wide-Output-Range Rectifier

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

Rack_ID	Voltage level	R <sub>s</sub> (± 0.1%)
1	3.3	open
2	2.8	35.2k
3	2.3	15k
4	1.8	8k
5	1.4	4.99k
6	1	2.87k
7	0.5	1.27k
8	0	0

**Configuration of the A3 – A0 bits:** The rectifier will determine the configured address based on the Unit\_ID and Rack\_ID voltage levels as follows (the order is A3 – A0):

				Unit_ID	_	
		1	2	3	4	5
	1	0000	0001	0010	0011	
	2	0100	0101	0110	0111	
	3	1000	1001	1010	1011	
Deck ID	4	1100	1101	1110	1111	
Rack_ID	5					
	6	0000	0001	0010	0011	0100
	7	0101	0110	0111	1000	1001
	8	1010	1011	1100	1101	1110

#### Unit x Rack: 4 x 4 and 5 x 3

				Unit_ID		
		6	7	8	9	10
	1	0000	0001			
	2	0010	0011			
	3	0100	0101			
Back ID	4	0110	0111	0000	0001	0010
Rack_ID	5	1000	1001	0011	0100	0101
	6	1010	1011	0110	0111	1000
	7	1100	1101	1001	1010	1011
	8	1110	1111	1100	1101	1110

#### Unit x Rack: 2 x 8 and 3 x 5

Address detection: The Slot\_ID pin must be connected to Vout(-) in order to deliver output power. This connection provides a second interlock feature. This connection may be a short circuit or any resistance up to 100 kohm, to allow addressing in RS485 mode as described below. Device address in RS485 mode: The address in RS485 mode is divided into three components; Bay\_ID, Slot\_ID and Shelf\_ID

 $\mbox{Bay_ID:}$  The Unit\_ID definition in I²C mode becomes the bay id in RS485 mode.

 $\begin{array}{l} \textbf{Slot\_ID:} \ \mbox{Up to 10 different rectifiers could be positioned} \\ across a 19" shelf if the rectifiers are located vertically within the shelf. The resistor below needs to be placed between \\ \textbf{Slot\_ID and Vout ( - ). Internal pull-up to 3.3V is 10k} \Omega. \end{array}$ 

Slot	Resistor	Voltage	_	Slot	Resistor	Voltage	
invalid	none	3.3V		6	7.15k	1.35V	
1	100k	3V		7	4.99k	1.02V	
2	45.3k	2.67V	45.3k 2.67V		8	2.49k	0.69V
3	24.9k	2.34V		9	1.27k	0.36V	
4	15.4k	2.01V		10	0	0	
5	10.5k	1.68V					

In the -EC & -ES versions, a 100 k $\Omega$  resistor is installed internally to enable the output & indicate slot no. 1. To indicate another slot number, an external resistor should be connected so the parallel combination is the resistance shown in the table above.

**Shelf\_ID:** When placed horizontally up to 10 shelves can be stacked on top of each other in a fully configured rack. The shelf will generate the precision voltage level tabulated below referenced to Vout ( - ).

Shelf	V <sub>MIN</sub>	V <sub>NOM</sub>	V <sub>MAX</sub>		
1	2.3	2.5	2.7		
2	4.7	5.0	5.3		
3	7.4	7.5	7.6		
4	9.5	10.0	10.5		
5	11.8	12.5	13.2		
6	14.2	15.0	15.8		
7	16.6 17.5		18.4		
8	19	20.0	21		
9	21.3	22.5	23.6		
10	23.8	25.0	26.3		

Global Broadcast: This is a powerful command because it instruct all rectifiers to respond simultaneously. A *read* instruction should never be accessed globally. The rectifier should issue an 'invalid command' state if a 'read' is attempted globally.

For example, changing the 'system' output voltage requires the global broadcast so that all paralleled rectifiers change their output simultaneously. This command can also turn OFF the 'main' output or turn ON the 'main' output of all rectifiers simultaneously. Unfortunately, this command does have a side effect. Only a single rectifier needs to pull down the ninth *acknowledge* bit. To be certain that each rectifier responded to the global instruction, a *READ* instruction should be executed to each rectifier to verify that the command properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

Alert Response Address (ARA): This feature enables the 'master' to rapidly determine which 'slave' rectifier triggered

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

the Alert# signal without having to poll each rectifier one at a time. During normal operation the rectifier activates (pulls down LO) the Alert# signal line indicating that it needs attention when a 'state' change occurs. The master can determine who pulled the 'alert' line by sending out the alert-response-address, address 12b, with a 'read' instruction. If the rectifier triggered the 'alert' it should respond back with its address. The instruction takes the form below;

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	1	8		1	8	1	8	1	1	J
	S	ARA address	Rd	А	My address	A	PEC	A	Ρ	

If during the ARA response multiple rectifiers send out their addresses, then the actual address received by the master is the lowest address from the combinations of those rectifiers that responded.

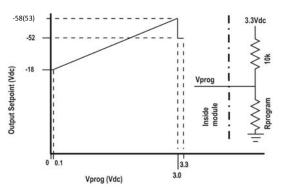
The 'my address' field contains the address of the rectifier in the 7 most significant bits (msb) of the byte. The lsb of the byte is a don't care, it could be a 0 or a 1. For more information refer to the SMBus specification

The  $\mu$ C needs to read the actual **my address** data byte that is sent back to the master. If the **my address** data byte agrees with the address of this unit, then, and only then, the  $\mu$ C needs to clear (de-assert) its Alert# signal. Thus, the rectifier whose address has been sent out gets de-asserted from the joint Alert# line.

If the Alert# line is still asserted, the host should send out an ARA request again and find out who else asserted Alert#. This process needs to continue until the Alert# is released which is a clear indication that all rectifiers that asserted Alert# have had their status states read back.

**Voltage programming (V**<sub>prog</sub>): Hardware voltage programming controls the output voltage until a software command to change the output voltage is executed. Then software voltage programming overrides the hardware margin setting and the rectifier no longer listens to any hardware margin settings until power to the controller is interrupted, for example if input power or bias power is cycled off, then on.

Under hardware voltage programming, an analog voltage on Vprog can vary the output voltage linearly from 18Vdc to 53Vdc (FB version) or 18Vdc to 58Vdc (FB2 version) for  $0.1V \le$ Vprog  $\le 3.0V$  referenced to LGND. If Vprog is raised  $\ge 3.2V$ , Vout is reset to its default value of 52V. If  $0 \le$  Vprog <0.1V, the output remains at its minimum value of 18V.



Factory default setting driven by Vprog

For the blind-mate rectifier option, the Vprog pin level can be set by an external resistor divider between an external voltage source and LGND as shown in the figure above, or by a precision voltage source connected between Vprog and LGND.

For the non-blind-mate options, the resistor divider shown above for Vprog is internal, connected to the 5V bias supply with 46.4 kohm 1% pull-up resistor. The "Vout Adjust" potentiometer (100k) is connected between Vprog and LGND when the "Initial Vout" control switch is set to "Trimmed."

When bias power to the controller is recycled, the controller restarts into its default configuration, programmed to set the output voltage as instructed by the V<sub>prog</sub> pin. Again, subsequent software commanded settings permanently override the "Vout Adjust" setting.

Before enabling a hot-plugged rectifier, the output voltage should be set to a safe level—no higher than the bus voltage—to avoid a transient or possible shutdown. Assuming the shelf enables the rectifier by shorting ON/OFF to LGND, the shelf should also pull Vprog down to a safe level. This could be 0V (Vprog shorted to LGND), setting Vout to 18V, or some higher voltage that corresponds to an output voltage no greater than the bus voltage. The hotplugged rectifier will remain at this output voltage, possibly supplying no power, until commanded to a higher voltage.

Load share (Ishare): This is a single wire analog signal that is generated and acted upon automatically by rectifiers connected in parallel. Ishare pins should be connected to each other for rectifiers, if active current share among the rectifiers is desired. No resistors or capacitors should get connected to this pin.

**ON/OFF:** Controls the main  $52V_{DC}$  output when either analog control or PMBus protocols are selected, as configured by the Protocol pin. This pin must be pulled low to turn **ON** the rectifier. The rectifier will turn **OFF** if either the **ON/OFF** or the **Interlock** pin is released. This signal is referenced to LGND. Note that in RS485 mode the ON/OFF pin is ignored.

**Interlock**: This is a shorter pin utilized for hot-plug applications to ensure that the rectifier turns **OFF** before the power pins are disengaged. It also ensures that the rectifier

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

turns **ON** only after the power pins have been engaged. Must be connected to V\_OUT ( - ) for the rectifier to be ON, done internally for the -EC and -ES versions.

**Module Present:** This signal is tied to LGND inside the rectifier. It's intent is to provide a signal to the system that a rectifier is physically present in the slot.

**8V\_INT:** Single wire connection between rectifiers, Provides bias to the DSP of an unpowered rectifier.

#### **Status Signals**

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Power Good Warning (PG#): This signal is HI when the main output is being delivered and goes LO if the main output is about to decay below regulation. Note that should a catastrophic failure occur, the signal may not be fast enough to provide a meaningful warning. PG# also pulses at a 1ms duty cycle if the unit is in overload.

Fault#: A TTL compatible status signal representing whether a Fault occurred. This signal needs to be pulled HI externally through a resistor. This signal goes LO for any failure that requires rectifier replacement. These faults may be due to:

- Over-temperature shutdown
- Over-voltage shutdown
- Internal Rectifier Fault

Over temp warning (OTW#): A TTL compatible status signal representing whether an over temperature exists. This signal needs to be pulled HI externally through a resistor.

If an over temperature should occur, this signal would pull LO for approximately 10 seconds prior to shutting down the rectifier. In its default configuration, the unit would restart if internal temperatures recover within normal operational levels. At that time the signal reverts back to its open collector (HI) state.

**Power\_CAP:** This signal is HI when the main output is 3000w and goes LO when the main output is 1400w.

#### **Serial Bus Communications**

The I<sup>2</sup>C interface facilitates the monitoring and control of various operating parameters within the unit and transmits these on demand over an industry standard I<sup>2</sup>C Serial bus.

All signals are referenced to 'LGND'.

**Pull-up resistors:** The clock, data, and Alert# lines do not have any internal pull-up resistors inside the rectifier. The customer is responsible for ensuring that the transmission impedance of the communications lines complies with I<sup>2</sup>C and SMBus standards.

Serial Clock (SCL): The clock pulses on this line are generated by the host that initiates communications across

the I<sup>2</sup>C Serial bus. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I<sup>2</sup>C /SMBus specifications.

Serial Data (SDA): This line is a bi-directional data line. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I<sup>2</sup>C /SMBus specifications.

#### **Digital Feature Descriptions**

**PMBus™ compliance:** The rectifier is fully compliant to the Power Management Bus (PMBus™) rev1.2 requirements. This Specification can be obtained from <u>www.pmbus.org</u>.

'Manufacturer Specific' commands are used to support additional instructions that are not in the PMBus™ specification.

All communication over the PMBus interface must support the Packet Error Checking (PEC) scheme. The PMBus master must generate the correct PEC byte for all transactions, and check the PEC byte returned by the rectifier.

The Alert# response protocol (ARA) whereby the PMBus Master can inquire who activated the Alert# signal is also supported. This feature is described in more detail later on.

Non-volatile memory is used to store configuration settings. Not all settings programmed into the device are automatically saved into this non-volatile memory. Only those specifically identified as capable of being stored can be saved. (see the Table of Commands for which command parameters can be saved to non-volatile storage).

Non-supported commands: Non supported commands are flagged by setting the appropriate STATUS bit and issuing an Alert# to the 'host' controller.

If a non-supported read is requested the rectifier will return 0x00h for data.

**Data out-of-range:** The rectifier validates data settings and sets the data out-of-range bit and Alert# if the data is not within acceptable range.

Master/Slave: The 'host controller' is always the MASTER. Rectifiers are always SLAVES. SLAVES cannot initiate communications or toggle the Clock. SLAVES also must respond expeditiously at the command of the MASTER as required by the clock pulses generated by the MASTER.

**Clock stretching:** The 'slave'  $\mu$ Controller inside the rectifier may initiate clock stretching if it is busy and it desires to delay the initiation of any further communications. During the clock stretch the 'slave' may keep the clock LO until it is ready to receive further instructions from the host controller. The maximum clock stretch interval is 25ms.

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

The host controller needs to recognize this clock stretching, and refrain from issuing the next clock signal, until the clock line is released, or it needs to delay the next clock pulse beyond the clock stretch interval of the rectifier. Note that clock stretching can only be performed after completion of transmission of the 9<sup>th</sup> ACK bit, the exception being the START command.

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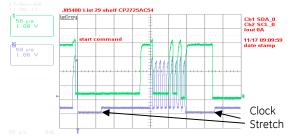


Figure 15. Example waveforms showing clock stretching.

I<sup>2</sup>C Bus Lock-Up detection: The device will abort any transaction and drop off the bus if it detects the bus being held low for more than 35ms.

**Communications speed:** Both 100kHz and 400kHz clock rates are supported. The rectifiers default to the 100kHz clock rate.

Packet Error Checking (PEC): The rectifier will not respond to commands without the trailing PEC. The integrity of communications is compromised if packet error correction is not employed. There are many functional features, including turning OFF the main output, that require validation to ensure that the desired command is executed.

PEC is a CRC-8 error-checking byte, based on the polynomial  $C(x) = x^8 + x^2 + x + 1$ , in compliance with PMBus<sup>TM</sup> requirements. The calculation is based in all message bytes, including the originating write address and command bytes preceding read instructions. The PEC is appended to the message by the device that supplied the last byte.

Alert#: The rectifier can issue Alert# driven from either its internal micro controller ( $\mu$ C) or from the I<sup>2</sup>C bus master selector stage. That is, the Alert# signal of the internal  $\mu$ C funnels through the master selector stage that buffers the Alert# signal and splits the signal to the two Alert# signal pins exiting the rectifier. In addition, the master selector stage signals its own Alert# request to either of the two Alert# signals when required.

The  $\mu$ C driven Alert# signal informs the 'master/host' controller that either a STATE or ALARM change has occurred. Normally this signal is HI. The signal will change to its LO level if the rectifier has changed states and the signal will be latched LO until the rectifier receives a 'clear\_faults' instruction.

The signal will be triggered for any state change, including the following conditions;

- VIN under or over voltage
- Vout under or over voltage
- IOUT over current
- Over Temperature warning or fault
- Communication error

- PEC error
- Invalid command
- Internal faults
- Both Alert#\_0 and -1 are asserted during power up to notify the master that a new rectifier has been added to the bus.

The rectifier will clear the Alert# signal (release the signal to its HI state) upon the following events:

- Receiving a CLEAR\_FAULTS command
- Bias power to the processor is recycled

The rectifier will re-assert the Alert line if the internal state of the rectifier has changed, even if that information cannot be reported by the status registers until a clear\_faults is issued by the host. If the Alert asserts, the host should respond by issuing a clear\_faults to retire the alert line (this action also provides the ability to change the status registers). This action triggers another Alert assertion because the status registers changed states to report the latest state of the rectifier. The host is now able to read the latest reported status register information and issue a clear\_faults to retire the Alert signal.

**Re-initialization:** The I<sup>2</sup>C code is programmed to re-initialize if no activity is detected on the bus for 5 seconds. Reinitialization is designed to guarantee that the I<sup>2</sup>C  $\mu$ Controller does not hang up the bus. Although this rate is longer than the timing requirements specified in the SMBus specification, it had to be extended in order to ensure that a re-initialization would not occur under normal transmission rates. During the few µseconds required to accomplish reinitialization the I<sup>2</sup>C  $\mu$ Controller may not recognize a command sent to it. (i.e. a start condition).

**Read back delay:** The rectifier issues the Alert# notification as soon as the first state change occurred. During an event a number of different states can be transitioned to before the final event occurs. If a read back is implemented rapidly by the host a successive Alert# could be triggered by the transitioning state of the rectifier. In order to avoid successive Alert# s and read back and also to avoid reading a transitioning state, it is prudent to wait more than 2 seconds after the receipt of an Alert# before executing a read back. This delay will ensure that only the final state of the rectifier is captured.

Successive read backs: Successive read backs to the rectifier should not be attempted at intervals faster than every one second. This time interval is sufficient for the internal processors to update their data base so that successive reads provide fresh data.

**Dual, redundant buses:** Two independent I<sup>2</sup>C lines provide true communications bus redundancy and allow two independent controllers to sequentially control the rectifier. For example, a short or an open connection in one of the I<sup>2</sup>C lines does not affect communications capability on the other I<sup>2</sup>C line. Failure of a 'master' controller does not affect the rectifiers and the second 'master' can take over control at any time.

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc. 5 Vdc @ 10W

Conceptually a Digital Signal Processor (DSP) referenced to Vout(-) of the rectifier provides secondary control. A Bidirectional Isolator provides the required isolation between power ground, Vout(-) and signal/logic ground (LGND). A secondary micro controller provides instructions to and receives operational data from the DSP. The secondary micro controller also controls the communications over two independent I2C lines to two independent system controllers.

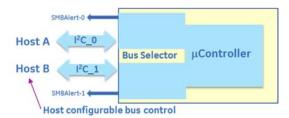
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The secondary micro controller is designed to default to 12C 0 when powered up. If only a single system controller is utilized, it should be connected to I2C\_0. In this case the I2C\_1 line is totally transparent as if it does not exist.

If two independent system controllers are utilized, then one of them should be connected to I2C\_0 and the other to I2C 1.

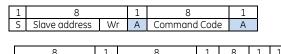
At power up the master connected to I2C 0 has control of the bus. See the section on Dual Master Control for further description of this feature.



Conceptual representation of the dual I<sup>2</sup>C bus system.

### PMBus<sup>™</sup> Commands

Standard instruction: Up to two bytes of data may follow an instruction depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.



, , ,	4	•	4	•	4
Low data byte	Α	High data byte	Α	PEC	Α
Master to Slave	<b>_</b> Slo	ive to Master			

SMBUS annotations; S – Start , Wr – Write, Sr – re-Start, Rd – Read.

A – Acknowledge, NA – not-acknowledged, P – Stop

Standard READ: Up to two bytes of data may follow a READ request depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

1	7	1		8	1
S	Slave address	Wr	Α	Command Code	Α

	1	7		1	1	8	3	1	
ç	Sr	Slave Addres	s I	Rd	Α	LS	SB	Α	
		8	1		8		1		1
		MSB	Α	PEC		C NA			Ρ

Block communications: When writing or reading more than two bytes of data at a time BLOCK instructions for WRITE and READ commands are used instead of the Standard Instructions above to write or read any number of bytes greater than two.

Block write format:

1	7			1	1				8			1	
S	Slave address		Wr	A			Comm	nand	l Co	de	Α		
Γ	8	1		8		1		8		1			
E	Byte count = N A		Data 2	L	А	[	Data 2		Α				
	8	1		8		1		8	3		1	1	1
		Α		Data N		J A		PEC			Α	Ρ	
k read format:													
1	7			1	1				8			1	

Bloc

1		7			1	1		8			1
S	S	Slave address				Slave address Wr A Command Code			Code	Α	
	1	7			1		1				
	Sr	Slave Ad	dres	SS	Ro	b	А				
		8		1	5	3	1	8		1	
	By	∕te count = N	1	Α	Dat	ta 1	A	Data 2		А	
		8	1		8		1	8		1	1
			Α	C	)ata	Ν	Α	PEC		NA	Р

Linear Data Format: The definition is identical to Part II of the PMBus Specification. All standard PMBus values, with the exception of output voltage related functions, are represented by the linear format described below. Output voltage functions are represented by a 16 bit mantissa. Output voltage has a E=9 constant exponent.

The Linear Data Format is a two byte value with an 11-bit, two's complement mantissa and a 5-bit, two's complement exponent or scaling factor, its format is shown below.

	Data Byte High								Dat	a By	∕te L	.ow				
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
		Ехро	oner	nt (E)	)					Man	tisso	a (M	)			

The relationship between the Mantissa, Exponent, and Actual Value (V) is given by the following equation:

 $V = M * 2^E$ 

Where: V is the value, M is the 11-bit, two's complement mantissa, E is the 5-bit, two's complement exponent

#### **Standard features**

**Supported features that are not readable:** The commands below are supported at the described setting but they cannot be read back through the command set.

Command	Comments
ON_OFF_CONFIG (0x02)	Both the CNTL pin, and the OPERATION command, enabling or disabling the output, are supported. Other options are not supported.
Capability (0x19)	400KHz, ALERT#
PMBus revision (0x98)	1.2

**Status and Alarm registers:** The registers are updated with the latest operational state of the rectifier. For example, whether the output is ON or OFF is continuously updated with the latest state of the rectifier. However, alarm information is maintained until a clear\_faults command is received from the host. For example, the shutdown or OC\_fault bits stay in their alarmed state until the host clears the registers.

A clear\_faults clears all registers. If a fault still persists after the clear\_faults is commanded, the register bit annunciating the fault is reset again.

#### **Adjustment Ranges**

Some of the PMBus commands on the next page enable adjustment of operating parameters within the ranges specified below. If a command is received with a value outside this range, the module does not change the present setting. Instead it uses CML to indicate a communication failure.

	Hex	Default	Adjust ran	
Command	Code	HL (LL)	Low	High
Vout_command	0x21	52	17	54
Vout_OV_fault_limit	0x40	55	16	55
Vout_OV_warn_limit	0x42	54	16	55
Vout_UV_warn_limit	0x43	17	16	55
Vout_UV_fault_limit	0x44	16	16	55
lout_OC_fault_limit	0x46	68 (30)	0	68
lout_OC_LV_fault_limit	0x48	16	16	55
lout_OC_warn_limit	0x4A	67.3(29.8)	0	67.3
OT_fault_limit	0x4F	110	0	150
OT_warn_limit	0x51	105	0	150
Vin_OV_fault_limit	0x55	270	90	270
Vin_OV_warn_limit	0x57	265	90	265
Vin_UV_warn_limit	0x58	87.5	87.5	265
Vin_UV_fault_limit	0x59	80	80	270

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

#### **Command Descriptions**

GF

Commands are listed in numerical order, with a summary table at the end of this section.

**Operation (0x01) :** Turns the 52V output ON or OFF. The default state is **ON** at power up. Only the following data bytes are supported:

FUNCTION	DATA BYTE
Unit ON	0x80
Unit OFF	0x00

To **RESET** the rectifier using this command, command the rectifier OFF, wait at least 2 seconds, and then command the rectifier back ON. All alarms and shutdowns are cleared during a restart.

**Clear\_faults (0x03):** Clears all STATUS and FAULT registers and resets the Alert# line of the I<sup>2</sup>C side in control. The I<sup>2</sup>C side not in control cannot clear registers in the rectifier. This command is always executable.

If a fault still persists after the issuance of the clear\_faults command, the specific registers indicating the fault first clears but then get set again to indicate that the unit is still in the fault state.

WRITE\_PROTECT register (0x10): Used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. All supported commands may have their parameters read, regardless of the write\_protect settings. The contents of this register cannot be stored into non-volatile memory using the Store\_user\_code command. The default setting of this register is enable\_all\_writes, write\_protect 0x00h. The write\_protect command must always be accepted.

FUNCTION	DATA BYTE
Enable all writes	00
Disable all writes except write_protect	80
Disable all writes except write_protect and OPERATION	40

**Restore\_Default\_All (0x12):** Restores all operating register values and responses to the factory default parameters set in the rectifier. The factory default cannot be changed.

**Restore\_default\_code (0x14):** Restore only a specific register parameter into the operating register section of the rectifier.

Store\_user\_code (0x17): Changes the user default setting of a single register. In this fashion some protection is offered to ensure that only those registers that are desired to be changed are in fact changed.

**Restore\_user\_code (0x18):** Restores the user default setting of a single register.

Vout\_mode (0x20): This is a 'read only' register. The upper three bits specify the supported data format, in this case Linear mode. The lower five bits specify the exponent of the data in two's complement binary format for output voltage related commands, such as Vout\_command. These commands have a 16 bit mantissa. The exponent is fixed by the rectifier and is returned by this command

Mode	Bits [7:5]	Bits [4:0] (Parameter)
Linear	000b	xxxxxb

Vout\_Command (0x21): Used to dynamically change the output voltage of the rectifier. This command can also be used to change the factory programmed default set point of the rectifier by executing a store-user instruction that changes the user default firmware set point.

The default set point can be overridden by the Vprog signal pin which is designed to override the firmware based default setting during turn ON.

In parallel operation, changing the output voltage should be performed simultaneously to all rectifiers using the Global Address (Broadcast) feature. If only a single rectifier is instructed to change its output, it may attempt to source all the required power which can cause either a power limit or shutdown condition.

Digital programming of output voltage overrides the set point voltage configured by the **Vprog** signal pin as long as ac input power is applied continuously. The program no longer looks at the '**Vprog** pin' and will not respond to any hardware voltage settings. If ac input power is removed, the  $\mu$ Controller is reset to its default configuration, looking at the **Vprog** signal for output voltage control. In many applications, the **Vprog** pin is used for setting initial conditions, if different that the factory setting. Software programming then takes over once a Vout\_Command is sent.

To properly hot-plug a rectifier into a live backplane, the system generated voltage should match either the factory adjusted firmware level or the voltage level reconfigured by the Vprog pin. Otherwise, the voltage state of the plugged in rectifier could be significantly different than the powered system.

Programmed voltage range:  $18V_{\text{DC}}$  –  $53V_{\text{DC}}$  for FB version;  $18V_{\text{DC}}$  –  $58V_{\text{DC}}$  for FB2 version.

A voltage programming example: The task: set the output voltage to  $50.45 V_{\text{DC}}$ 

This rectifier supports the linear mode of conversion specified in the PMBus™ specification. The supported output voltage exponent is documented in the Vout\_mode (0x20) command. The exponent for output voltage setting is 2-<sup>9</sup> (see the PMBus™ specification for reading this command). Calculate the required voltage setting to be sent; 50.45 x 2<sup>9</sup> = 25830. Convert this decimal number into its hex equivalent: 64E6 and send it across the bus LSB first and then MSB; E664 with the trailing PEC.

Vin\_ON (0x35): This is a 'read only' register that informs the controller at what input voltage level the rectifier turns ON. The default value is tabulated in the data section. The value is contingent on whether the rectifier operates in the low\_line or high\_line mode.

Vin\_OFF (0x36): This is a 'read only' register that informs the controller at what input voltage level the rectifier turns OFF. The default value is tabulated in the data section. The value

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

is contingent on whether the rectifier operates in the low\_line or high\_line mode.

GF

Vout\_OV\_fault\_limit (0x40): Sets the value at which the main output voltage will shut down. The default OV\_fault value is set at 60Vdc. This level can be permanently changed and stored in non-volatile memory.

Vout\_OV\_fault\_response (0x41): This is a 'read only' register. The only allowable state is a latched state after three retry attempts.

An overvoltage shutdown is followed by three attempted restarts, each successive restart delayed 1 second. If within a 1 minute window three attempted restarts failed, the unit will latch OFF. If less than 3 shutdowns occur within the 1 minute window then the count for latch OFF resets and the 1 minute window starts all over again. This performance cannot be changed.

**Restart after a latched state:** Either of four restart mechanisms is available;

- The hardware pin ON/OFF may be cycled OFF and then ON.
- The unit may be commanded to restart via i2c through the Operation command by first turning OFF then turning ON.
- The third way to restart is to remove and reinsert the unit.
- The fourth way is to turn OFF and then turn ON ac power to the unit.

A successful restart clears all STATUS and ALARM registers.

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

- Issuing a GLOBAL OFF and then a GLOBAL ON command to all rectifiers
- Toggling Off and then ON the **ON/OFF** signal, if this signal is paralleled among the rectifiers.
- Removing and reapplying input commercial power to the entire system.

The rectifiers should be OFF for at least 20 - 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

Vout\_OV\_warn\_limit (0x42): Sets the value at which a warning will be issued that the output voltage is too high. The default OV\_warn limit is set at 56Vdc. Exceeding the warning value will set the Alert# signal. This level can be permanently changed and stored in non-volatile memory.

Vout\_UV\_warn\_limit (0x43): Sets the value at which a warning will be issued that the output voltage is too low. The default UV\_warning limit is set at 41Vdc. Reduction below the warning value will set the Alert# signal. This level can be permanently changed and stored in non-volatile memory.

Vout\_UV\_fault\_limit (0x44): Sets the value at which the rectifier will shut down if the output gets below this level when not in overload (see 0x48 for overload). The default UV\_fault limit is set at 36Vdc. This register is masked if the UV is caused by interruption of the input voltage to the rectifier. This level can be permanently changed and stored in non-volatile memory.

Vout\_UV\_fault\_response (0x45): Sets the response if the output voltage falls below the UV\_fault\_limit. The default UV\_fault\_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

**lout\_OC\_fault\_limit (0x46):** Sets the value at which the rectifier will shut down at High Line. This level can be permanently changed and stored in non-volatile memory. The Low Line level is not adjustable, it is set at 30A.

**lout\_OC\_fault\_response (0x47):** Sets the response if the output overload exceeds the OC\_Fault\_limit value. The default OC\_fault\_response is hiccup (0xF8). The only two allowable states are latched (0xC0) or hiccup. The default response state can be permanently changed and stored in non-volatile memory. The response is the same for both low\_line and high\_line operations.

**lout\_OC\_LV\_fault\_limit (0x48):** Sets the value at which the rectifier will shut down when the rectifier is in overload and the output gets below this level. The default fault limit is set at 36Vdc. This register is masked if the UV is caused by interruption of the input voltage to the rectifier. This level can be permanently changed and stored in non-volatile memory.

**lout\_OC\_warn\_limit (0x4A):** Sets the value at which the rectifier issues a warning that the output current is getting too close to the shutdown level at high line. This level can be permanently changed and stored in non-volatile memory. The Low Line level is not adjustable, it is set at 29A.

**OT\_fault\_limit (0x4F):** Sets the value at which the rectifier responds to an OT event, sensed by the dc-sec sensor. The response is defined by the OT\_fault\_response register.

**OT\_fault\_response (0x50):** Sets the response if the output overtemperature exceeds the OT\_Fault\_limit value. The default OT\_fault\_response is hiccup (0xC0). The only two allowable states are latched (0x80) or hiccup. The default response state can be permanently changed and stored in non-volatile memory.

**OT\_warn\_limit (0x51):** Sets the value at which the rectifier issues a warning when the dc-sec temperature sensor exceeds the warn limit.

Vin\_OV\_fault\_limit (0x55): Sets the value at which the rectifier shuts down because the input voltage exceeds the

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

allowable operational limit. The default Vin\_OV\_fault\_limit is set at 300Vac. This level can be permanently lowered and stored in non-volatile memory.

GF

Vin\_OV\_fault\_response (0x56): Sets the response if the input voltage level exceeds the Vin\_OV\_fault\_limit value. The default Vin\_OV\_fault\_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

Vin\_UV\_warn\_limit (0x58): This is another warning flag indicating that the input voltage is decreasing dangerously close to the low input voltage shutdown level. The default UV\_fault\_limit is 90Vac. This level can be permanently raised, but not lowered, and stored in non-volatile memory.

Vin\_UV\_fault\_limit (0x59): Sets the value at which the rectifier shuts down because the input voltage falls below the allowable operational limit. The default Vin\_UV\_fault\_limit is set at 85Vac. This level can be permanently raised and stored in non-volatile memory

Vin\_UV\_fault\_response (0x5A): Sets the response if the input voltage level falls below the Vin\_UV\_fault\_limit value. The default Vin\_UV\_fault\_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

**STATUS\_BYTE (0x78)**: Returns one byte of information with a summary of the most critical device faults.

Bit Position	Flag	Default Value
7	Unit is busy	0
6	OUTPUT OFF	0
5	VOUT Overvoltage Fault	0
4	IOUT Overcurrent Fault	0
3	VIN Undervoltage Fault	0
2	Temperature Fault or Warning	0
1	CML (Comm. Memory Fault)	0
0	None of the above	0

**STATUS\_WORD (0x79):** Returns status\_byte as the low byte and the following high\_byte.

Bit Position	Flag	Default Value
7	VOUT Fault or Warning	0
6	IOUT Fault or Warning	0
5	INPUT Fault or Warning	0
4	MFR SPECIFIC	0
3	POWER_GOOD# (is negated)	0
2	N/A	0
1	OTHER	0
0	UNKNOWN Fault or Warning	0

STATUS\_VOUT (0X7A): Returns one byte of information of output voltage related faults.

Bit Position	Flag	Default Value
7	VOUT OV Fault	0
6	VOUT_OV_WARNING	0

5	VOUT_UV_WARNING	0
4	VOUT UV Fault	0
3 - 0	×	0

**STATUS\_IOUT (0X7B):** Returns one byte of information of output current related faults.

Bit Position	Flag	Default Value
7	IOUT OC Fault	0
6	IOUT OC LV Fault	0
5	IOUT OC Warning	0
4	X	0
3	CURRENT SHARE Fault	0
2	IN POWER LIMITING MODE	0
1-0	×	0

The OC Fault limit sets where current limit is set. The rectifier actually shuts down below the LV fault limit setting.

**STATUS\_INPUT (0X7C):** Returns one byte of information of input voltage related faults.

Bit Position	Flag	Default Value
7	VIN_OV_Fault	0
6	VIN_OV_Warning	0
5	VIN_UV_ Warning	0
4	VIN_UV_Fault	0
3	Unit OFF for low input voltage	0
2	IIN_OC_Fault	0
1-0	X	0

STATUS	TEMPERATURE (0x7D): Returns one byte of
informat	ion of temperature related faults.

Bit Position	Flag	Default Value
7	OT Fault	0
6	OT Warning	0
5 - 0	X	0

**STATUS\_CML (0X7E):** Returns one byte of information of communication related faults.

Bit Position	Flag	Default Value
7	Invalid/Unsupported Command	0
6	Invalid/Unsupported Data	0
5	Packet Error Check Failed	0
4 - 2	Х	0
1	Other Communication Fault	0
0	Х	0

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

#### **Read back Descriptions**

GF

Single parameter read back: Functions can be read back one at a time using the read\_word\_protocol with PEC. A command is first sent out notifying the slave what function is to be read back followed by the data transfer.

Analog data is always transmitted LSB followed by MSB. A NA following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

1	8				1		8	3	1
S	Slave a	ddres	SS	Wr	Α	(	Comma	nd Code	А
1		8			1				
Sr	Slave o	Slave address Rd			A				
	8	1		8		1	8	1	1
	LSB	A MSB				Ą	PEC	No-Ack	Ρ

Read back error: If the  $\mu$ C does not have sufficient time to retrieve the requested data, it has the option to return all FF's instead of incorrect data.

Read\_FRU\_ID (0x99,0x9A,0x9B,0x9E): Returns FRU information. Must be executed one register at a time.

1			8	1	8			1	1		
S	Slav	/e ac	ldress	Wr	А	Command 0x9x			Α		
											-
1			8		1	8			1		
Sr	Slav	/e ad	dress	Rd	А	Byte count = $x$			:	А	
8	3	1	8	1	8	8		8		1	1
Byt	e_1	А	Byte	А	Byte_x		А	PEC	No	o-Ack	Ρ

Mfr\_ID (0x99): Manufacturer in ASCII – 6 characters maximum,

General Electric – Critical Power represented as, GE-CP

Mfr\_model (0x9A): Manufacturer model-number in ASCII – 16 characters, for this unit: CC3500AC52TEFBxx

Mfr\_revision (0x9B): Total 8 bytes, this is the product series taking the form X:YZ. Each byte is in ASCII format. The series number is read from left to right, scanned from the series number bar code on the power supply. Unused characters are filled at the end with null

Mfr\_serial (0x9E): Product serial number includes the manufacturing date, manufacturing location in up to 16 characters. For example:

13KZ51018193xxx, is decoded as;

- 13 year of manufacture, 2013
- KZ manufacturing location, in this case Matamoros

51 – week of manufacture

018193xxx - serial #, mfr choice

### Manufacturer-Specific PMBus™ Commands

Many of the manufacturer-specific commands read back more than two bytes. If more than two bytes of data are returned, the standard SMBus<sup>™</sup> Block read is utilized. In this process, the Master issues a Write command followed by the data transfer from the rectifier. The first byte of the Block Read data field sends back in hex format the number of data bytes, exclusive of the PEC number, that follows. Analog data is always transmitted LSB followed by MSB. A No-ack following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

Mfr\_Specific Status and alarm registers: The content and partitioning of these registers is significantly different than the standard register set in the PMBus™ specification. More information is provided by these registers and they are either accessed rapidly, at once, using the 'multi parameter' read back scheme of this document, or in batches of two STATUS and two ALARM registers.

Status\_summary (0xD0) : This 'manufacturer specific' command is the basic read back returning STATUS and ALARM register data, output voltage, output current, and internal temperature data in a single read. Internal temperature should return the temperature that is closest to a shutdown level.

iuu		leve	1.										
L			8					8				1	
5	Slave	e add	ress	Wr		Α		Command	d Co	de		A	
												_	
1			8			1		8			1		
ŝr	Slave	e ada	dress	Rc	1	А	f	Byte count	: = 1	1	Α		
8	3	1		8		1	8 1 8		8 1		3	1	
Stat	us-2	Α	Sto	atus-1		Α		Alarm-3 A			Alarm-2		Α
												_	
8	3	1	-	8			1	8			1		
۱ar	m-1	Α	Vo	tage L	SB	A	4	Voltage	MS	З	Α		
	8			1				8		1			
С	urrent	-LSB		А		Cur	Current-MSB			A			
	8			1		8			1				
Ten	nperat	ure-l	SB	Α	Т	em	pe	rature-MS	В	A	1		
	L S L S I S S I S S S S S S S S S S S S S	L Slave Slave ir Slave ktatus-2 8 Narm-1 8 Current	Slave add Slave add Slave add Slave add Slave add Slave add Alarm-1 A S Current-LSB	L 8   Slave address   I 8   Slave address   8 1   Status-2 A   Alarm-1 A   Vol   8   Current-LSB	L 8   L 8   Slave address Wr   L 8   I 8   Slave address Rc   8 1 8   Alarm-1 A Voltage L   8 1 8   1 A Voltage L   8 1 8   1 A Voltage L	L 8   L 8   Solave address Wr   L 8   I 8   I 8   I 8   I 8   I 8   I 8   I 8   I 8   I 8   I 8   I 8   I 8   I 8   I 8   I 8   I 8   I 1   I 1   I 1   I 1	L 8 1   L 8 1   Slave address Wr A   L 8 1   I 8 1   ir Slave address Rd   Slave address Rd A   8 1 8 1   Alarm-1 A Voltage LSB /   8 1 Current-LSB A Cur   8 1 1 1	L 8 1   L 8 1   S Slave address Wr A   I 8 1 I   ir Slave address Rd A   8 1 8 1   itatus-2 A Status-1 A   8 1 8 1   Alarm-1 A Voltage LSB A   8 1 Current-LSB A Curre   8 1 1 1	L 8 1 8   L 8 1 8   Slave address Wr A Command   L 8 1 8   Slave address Rd A Byte count   B 1 8 1 8   Status-2 A Status-1 A Alarm-3   8 1 8 1 8   A Voltage LSB A Voltage   8 1 8 1   Current-LSB A Current-MSB   8 1 8	L 8 1 8   L 8 1 8   So Slave address Wr A Command Co   L 8 1 8   I 8 1 8   Ir Slave address Rd A   B 1 8 1   Itatus-2 A Status-1 A   Alarm-1 A Voltage LSB A   Voltage LSB A Voltage MSI   B 1 8   Current-LSB A Current-MSB   8 1 8   1 8	L 8 1 8   L 8 1 8   Solave address Wr A Command Code   L 8 1 8   I 8 1 8   ir Slave address Rd A   B 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1	L 8 1 8   L 8 1 8   Solave address Wr A Command Code   L 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1   I 8 1 8 1	Solution   Solutity is a solity is a solity is a solution   Solution<

8	1	1
PEC	No-Ack	Ρ

Default

# CC3500AC52FB Conduction Cooled Wide-Output-Range Rectifier

Input: 100-120/200-240 Vac; 3500W capable; Output: 18-58 Vdc, 5 Vdc @ 10W

**Status\_unit(0xD1):** This command returns the STATUS-2 and STATUS-1 register values using the standard 'read' format.

#### Status-2

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Bit Position	Flag	Default Value
7	PEC Error	0
6	OC [hiccup=1,latch=0]	1
5	Invalid_Instruction	0
4	Power_Capacity [HL = 1]	х
3	OR'ing Test Failed	0
2	n/a	0
1	Data_out_of_range	0
0	Remote ON/OFF [HI = 1]	х

**Oring fault:** Triggered either by the host driven or'ing test or by the repetitive testing of this feature within the rectifier. A destructive fault would cause an internal shutdown. Success of the host driven test depends on power capacity capability which needs to be determined by the external processor. Thus a non-destructive or'ing fault does not trigger a shutdown.

#### Status-1

Bit Position	Flag	Default Value
7	OT [Hiccup=1, latch=0]	1
6	OR'ing_Test_OK	0
5	Internal_Fault	0
4	Shutdown	0
3	Service LED ON	0
2	External_Fault	0
1	LEDs_Test_ON	0
0	Output ON (ON = 1)	×

Status\_alarm (0xD2): This command returns the ALARM-3 - ALARM-1 register values.

#### Alarm-3

Bit Position	Flag	Default Value
7	Interlock open	0
6	Fuse fail	0
5	PFC-DC communications fault	0
4	DC-i2c communications fault	0
3	AC monitor communications fault	0
2	×	0
1	×	0
0	Or'ing fault	0

#### Alarm-2

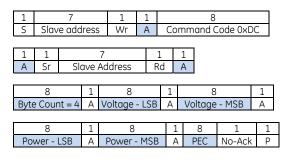
Bit Position	Flag	Default Value
7	N/A	0
6	No_Primary	0
5	Primary_OT	0
4	DC/DC_OT	0
3	Vo lower than BUS	0
2	Thermal sensor filed	0
1	Stby_out_of_limits	0
0	Power_Delivery	0

**Power Delivery:** If the internal sourced current to the current share current is > 10A, a fault is issued.

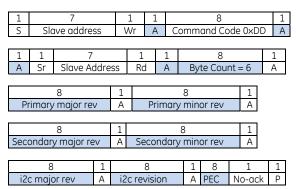
Α	Alarm-1			
	Bit Position	Fla		
	7	POWER		

Position	5	Value
7	POWER LIMIT	0
6	PRIMARY Fault	0
5	OT_Shutdown	0
4	OT_Warning	0
3	IN OVERCURRENT	0
2	OV_Shutdown	0
1	VOUT_out_of_limits	0
0	VIN_out_of_limits	0

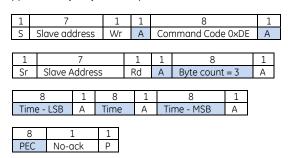
**Read input string (0xD4):** Reads back the input voltage and input power consumed by the rectifier.



**Read\_firmware\_rev [0 x D5]:** Reads back the firmware revision of all three  $\mu$ C in the rectifier.



**Read\_run\_timer [0 x D6]:** This command reads back the recorded operational ON state of the rectifier in hours. The operational ON state is accumulated from the time the rectifier is initially programmed at the factory. The rectifier is in the operational ON state both when in standby and when it delivers main output power. Recorded capacity is approximately 10 years of operational state.



**EEPROM record (0xD9):** The  $\mu$ C contains 128 bytes of reserved EEPROM space for customer use. After the