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Evaluation Board For CS42518/16

Features

- Single-Ended Analog Inputs and Outputs
- Integrated S/PDIF compatible Receiver
- CS5361 converters supply ADCIN1 and ADCIN2 for CS42518 One Line Modes
- CS8406 S/PDIF Digital Audio Transmitter
- Header for optional external configuration of CS42518 and board
- Header for external DSP serial audio I/O
- 3.3 or 5.0 Volt Logic Interface supply
- Demonstrates recommended layout and grounding arrangements
- Windows compatible software interface to configure CS42518 and inter-board connections

Description

The CDB42518 demonstration board is an excellent means for evaluating the CS42518/16 family of highly integrated multi-channel CODEC-S/PDIF receivers. Evaluation requires an analog/digital signal source and analyzer, Windows compatible computer, and power supplies.

System timing can be provided by an on-board oscillator or phase-locked to an S/PDIF input. RCA phono jacks are provided for the CS5361 analog inputs and CS42518 analog inputs and outputs. Digital data I/O is available via RCA phono jacks or optical connectors to/from the CS42518 and CS8406.

The Windows software provides a GUI to make configuration of the board easy. The software communicates through the computer's parallel port, and will configure the hardware to allow all features of the CS42518 to be evaluated. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB42518

Evaluation Board

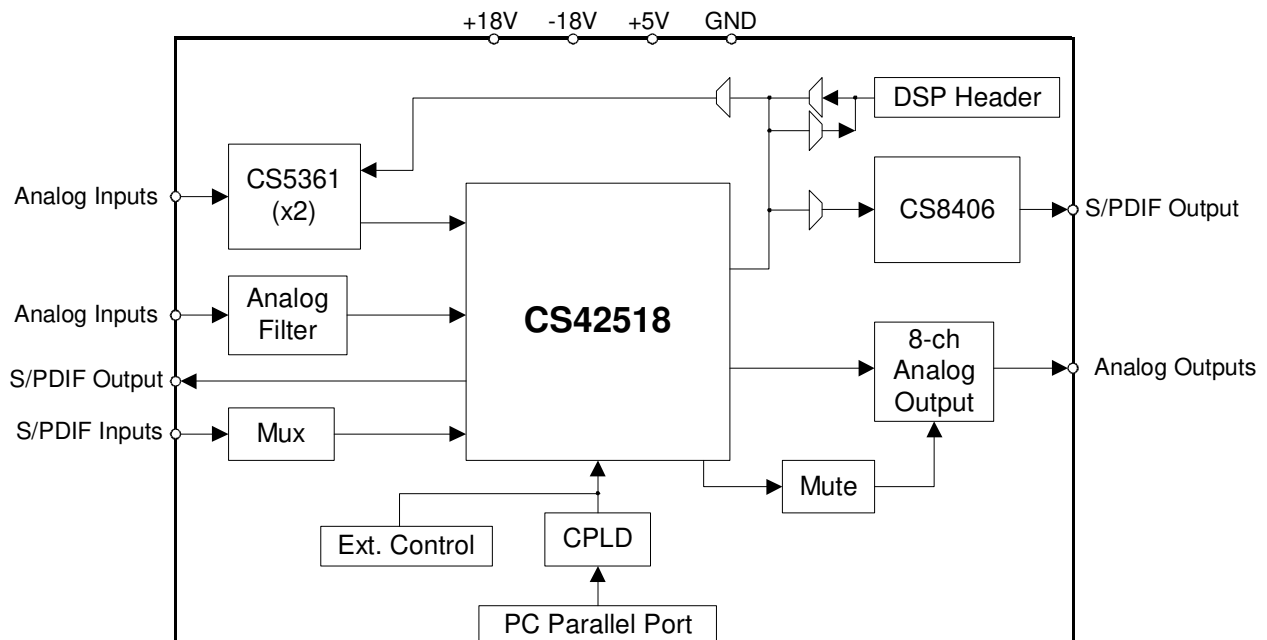


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1. SYSTEM OVERVIEW

The CDB42518 demonstration board is an excellent means for evaluating the CS42518/16 family of highly integrated CODEC-S/PDIF receivers. Analog and digital audio signal interfaces are provided, as well as a DB-25 computer parallel port interface for use with the supplied Windows configuration software.

The CDB42518 schematic set has been partitioned into 13 pages as shown in Figures 6 through 18.

1.1 CS42518

A complete description of each member of the CS42518/16 family is included in each respective product data sheet.

1.2 CS8406

The CS8406 S/PDIF transmitter on the demonstration board (see Figure 8) allows the performance of the CS42518 to be measured digitally. Either the CS42518 CODEC (CX) port or the Serial Audio Interface (SAI) port can be multiplexed to the CS8406. The CS8406 transmitter is configured to operate in slave mode only, and will receive the required clocks from the CS42518. The data format for the CS8406 is selectable and must match that of its source. The CS8406 must be configured using the supplied software.

1.3 CS5361

There are two CS5361 A/D converters on the CS42518 demonstration board (see Figures 9 and 10). These converters supply the CS42518 ADCIN signals, and must operate in left-justified, 24-bit mode only. Their serial data outputs are used when supporting the CS42518 One Line Mode of operation.

RCA analog connectors supply the inputs to each CS5361 channel through a unity gain, AC-coupled, single-to-differential circuit. Each CS5361 input circuit is biased to $1/2 V_A$, and a $1V_{RMS}$ signal will drive the converter to full scale. The CS5361 converters are set to operate in slave mode and will receive their clocks from the CS42518. The SCLK and LRCK signals can be provided from either the CS42518 CX or SAI port, and must be selected using the configuration software.

1.4 Crystal Oscillator

Oscillator Y1 (see Figure 7) provides the System Clock (OMCK) for the CS42518. The crystal oscillator on the board is mounted in pin sockets that allow it to be removed or replaced. The board is shipped with a 24.000 MHz crystal oscillator stuffed at Y1. Please refer to the CS42518/16 data sheet for details on OMCK operation.

The buffer on the output of the oscillator provides for signal level shifting to the proper VLS supply. This buffer can be removed if the oscillator is powered from the same VLS voltage source as the codec.

1.5 Analog Input

RCA phono connectors supply the CS42518 analog inputs through unity gain, AC-coupled single-to-differential circuits (see Figure 11). Each input circuit is biased to match the $2.7V_{DC}$ VQ, and a $1V_{RMS}$ differential signal will drive the CS42518 converter to full scale.

1.6 Analog Outputs

Each CS42518 analog output is routed through a differential to single-ended, unity-gain low pass filter, which is AC-coupled to an RCA phono jack (see Figures 12 through 15). The analog output filter on the CDB42518 has been designed to add flexibility when evaluating the CS42518 DAC outputs. The output filter was designed in a two stage format, with the first stage being an optional instrumentation amplifier, and the second stage a 2-pole butterworth low pass filter.

The 2-pole low pass filter provides an example of an inexpensive circuit with good distortion and dynamic range performance. It is designed to have the in-band impedance matched between the positive and negative legs. It also provides a balanced to single-ended conversion for standard un-balanced outputs. Evaluate this circuit by placing the FILT jumpers (three per output channel) to position 1 (selectable by J9, J10 & J11 for OUTA1, etc.).

The instrumentation amplifier is optionally inserted before the LPF by changing the FILT jumpers to position 2. The instrumentation amplifier incorporates a 5x gain (+14dB) which effectively lowers the noise contribution of the following 2-pole LPF. This improves the overall dynamic range of the system. The gain of this stage is determined from the following equation:

$$\text{Gain} = 1 + \frac{2(R)}{R_2}$$

The resistor designated by R_2 (see Figure 1) can be adjusted to change the gain of the instrumentation amp. The feedback resistors on the two sides of the instrumentation amp 'R' must be equal.

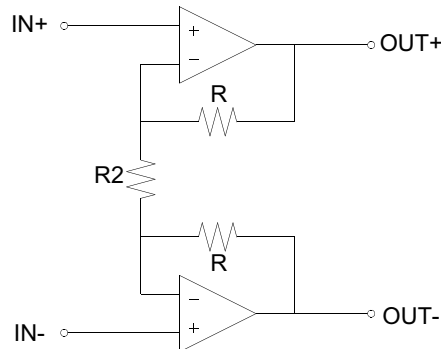


Figure 1. Instrumentation Amplifier Configuration

A resistor divider pad (R66 and R84 for OUTA1) has been placed after the low pass filter to bring the circuit back to unity gain (selectable with jumper J11 for OUTA1).

The attenuation provided by the output mute transistor (Q2 for OUTA1) is determined by the resistor-divider formed between the collector-emitter on-resistance and the output resistor of the LPF (R66 for OUTA1). The greater the output resistor, the greater the attenuation will be for a given transistor. The trade off is that a high output impedance is not usually desirable, and may affect the voltage transfer to the next stage based upon its input impedance.

The same resistor that affects the transistor mute level also affects the HPF formed with the output DC-block capacitor (C63 for OUTA1). For LPF configuration 2, the values for the DC-block capacitor and output resistor pad (R66 and R84 for OUTA1) were chosen to give uniform distortion performance across the audio bandwidth, particularly at low frequency. The HPF formed by this R-C pair must be such that the voltage across the aluminum electrolytic DC-block capacitor must be a minimum at 20Hz. This keeps the distortion due to the electrolytic's dielectric absorption properties to a minimum. For a design utilizing only LPF configuration 1, there is no post-LPF resistor-divider pad, and a much smaller value capacitor can be used.

1.7 CPLD

The CPLD controls the on-board signal routing and configuration (see Figure 17). The CPLD interfaces with the computer software through the DB-25 parallel port header, or can communicate with an external processor via the External Control header.

1.8 DB-25 Computer Parallel Port

On-board clock and data routing and configuration logic, as well as the CS42518 part are configured using a computer with the supplied Windows-based software. The software communicates via the DB-25 parallel port interface (see Figure 16) to a local CPLD that can configure all parts on the board.

1.9 External Control Header

A 26-pin dual-row header allows access to the control signals needed to configure the CS42518. The external controller has access to the CS42518 I²C/SPI signals, master mute and reset, and the CS42518 interrupt signal is available (see Figure 16). All control header signals are buffered, and are referenced to VLC levels. See Table 3 for a complete description of External Control Header signals.

1.10 DSP Header

A 32-pin dual-row header provides access to the serial audio signals required to interface with a DSP (see Figure 7). Either the CS42518 or the DSP header can be the master of the MCLK signal. The CS42518 can supply the DSP header with its recovered master clock (RMCK), or pass the local oscillator-sourced OMCK. An optional configuration supported is for the DSP header to source DSP_MCLK to the OMCK input, and the RMCK of the CS42518 is not used.

The CS42518 SAI and CX ports are individually selectable to be master or slave, and should source/receive their clocks to/from the DSP as required. All serial port timings must be synchronous to the to RMCK or the clock source supplying OMCK. See the data sheet for a complete description of serial port modes of operation. All DSP header signals are buffered, and are referenced to VLS levels. DSP interface power VLS and ground are supplied to the header. See Table 4 for a complete description of DSP Header signals.

1.11 LED Function Indicator

D1 (see Figure 16) indicates that a master reset condition has occurred on the board. D4 (see Figure 17) is sourced from the CPLD and is currently unsupported.

1.12 Power

Power can easily be supplied to the evaluation board through three binding posts, all referenced to the single black binding post ground connector (see Figure 18).

Supply +18.0 VDC to the green binding post to provide the positive analog rail. Supply -18.0 VDC to the yellow binding post to provide the negative analog rail. +18V and -18V supply power to the op-amps and can be +/-12 to +/-18 volts (must be +/-18 V when filter 2 is selected).

Supply +5.0VDC to the red binding post. This directly supplies the digital +5V, is regulated down to provide the digital +3.3V, and is filtered to supply VLC, VA and VARX.

VLS and VD must be individually set with jumpers to either +3.3V or +5V.

1.13 Grounding and Power Supply Decoupling

The CS42518 requires careful attention to power supply and grounding arrangements to optimize performance. Figures 15 and 16 detail the routing and component placement for both top and bottom layers of the demonstration board. Power supply decoupling capacitors are located as close to the CS42518 as possible. Extensive use of ground plane fill in the demonstration board yields large reductions in radiated noise.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5V	Input	+ 5VDC power
-18V	Input	-18 to -12VDC negative supply for the op-amps
+18V	Input	+12 to +18VDC positive supply for the op-amps
GND	Input	Ground connection from power supply
SPDIF RX - J1	Input	Digital audio interface input via coax
SPDIF RX - OPT1	Input	Digital audio interface input via optical
SPDIF TX - J2	Output	CS8406 digital audio interface output via coax
SPDIF TX - OPT2	Output	CS8406 digital audio interface output via optical
CS42518 TXP - OPT3	Output	CS42518 digital audio interface output via optical
PC Port - J22	Input/Output	Parallel connection to computer for SPI / I ² C control port signals
EXTERNAL CONTROL HEADER - J17	Input/Output	I/O for SPI / I ² C control port signals - see signal descriptions below
DSP HEADER - J36	Input/Output	I/O for DSP serial port signals - see signal descriptions below
ANALOG IN LFT/RT	Input	RCA phono jacks for analog input signal to CS42518 internal ADCs
EXT A/D #1 LEFT/RIGHT	Input	RCA phono jacks for analog input signal to CS5361 ADC #1
EXT A/D #2 LEFT/RIGHT	Input	RCA phono jacks for analog input signal to CS5361 ADC #2
OUT_A1 to OUT_B4	Output	RCA phono jacks for channels A1 to B4 analog outputs

Table 1. System Connections

JUMPER / SWITCH	PURPOSE	POSITION	FUNCTION SELECTED
J37	Selects source of voltage for the VLS supplies	+3.3V *+5V	Voltage source is +3.3V regulator Voltage source is +5V binding post
J38	Selects source of voltage for the VD supply	+3.3V *+5V	Voltage source is +3.3V regulator Voltage source is +5V binding post
S2	Stand-Alone Mode Select	SAM0 SAM1	Stand-Alone Modes are for debug use and are presently unsupported
J9,J10,J11 J13,J15,J16 J18,J19,J20 J23,J25,J26 J28,J29,J30 J32,J34,J35 J39,J40,J41 J43,J45,J46	DAC Output Filter select - FILT	*1 2	Selects standard 2-pole LPF Selects instrumentation-amp/LPF/pad *Default Factory Settings

Table 2. Jumper Settings
1.14 External Control Header Signals

Header Pin #	Signal Description	Source	Schematic Signal Name	Buffer	Buffer Voltage
1	External Control Present Signal	CTRL	EXT_CONTROL_PRESENT-	-	-
2	Ground	CDB	GND	-	-
3	Address Bit 0 (I ² C) / CS- (SPI)	CTRL	AD0/CS	74VHC125	VLC
4	Ground	CDB	GND	-	-
5	Address Bit 1 (I ² C) / CDIN (SPI)	CTRL	AD1/CDIN	74VHC125	VLC
6	Ground	CDB	GND	-	-
7	SDA (I ² C) / CDOOUT (SPI)	CTRL or CS42518	SDA/CDOOUT	MOSFET	VLC
8	Ground	CDB	GND	-	-
9	Serial Control Port Clock	CTRL	SCL/CCLK	74VHC125	VLC
10	Ground	CDB	GND	-	-
11	Master MUTE to all Outputs	CTRL	EXT_MUTE	74VHC125	VLC
12	Ground	CDB	GND	-	-
13	Master RESET	CTRL	EXT_RESET	Diode	-
14	Ground	CDB	GND	-	-
15	CS42518 Interrupt (Programmable)	CS42518	EXT_HDR_INT	74VHC125	VLC
16	Ground	CDB	GND	-	-
17	Enable external I2C interface	CTRL	EXT_EN_SCL	74VHC125	VLS
18	Ground	CDB	GND	-	-
19	Enable external I2C interface	CTRL	EXT_EN_SDA	74VHC125	VLS
20	Ground	CDB	GND	-	-

Table 3. CS42518 External Control Header Signals

1.15 DSP Header Signals

Header Pin #	Signal Description	Source	Schematic Signal Name	Buffer	Buffer Voltage
1	Master Clock	CS42518 or DSP	DSP_MCLK	74VHC125	VLS
2	Ground	CDB	GND	-	-
3	CODEC port LRCK	CS42518 or DSP	DSP_CX_LRCK	74VHC125	VLS
4	Ground	CDB	GND	-	-
5	CODEC port SCLK	CS42518 or DSP	DSP_CX_SCLK	74VHC125	VLS
6	Ground	CDB	GND	-	-
7	CODEC port SDATA Input 1	DSP	DSP_SDAT1	74VHC125	VLS
8	Ground	CDB	GND	-	-
9	CODEC port SDATA Input 2	DSP	DSP_SDAT2	74VHC125	VLS
10	Ground	CDB	GND	-	-
11	CODEC port SDATA Input 3	DSP	DSP_SDAT3	74VHC125	VLS
12	Ground	CDB	GND	-	-
13	CODEC port SDATA Input 4	DSP	DSP_SDAT4	74VHC125	VLS
14	Ground	CDB	GND	-	-
15	no connect	-	-	-	-
16	Ground	CDB	GND	-	-
17	SAI port LRCK	CS42518 or DSP	DSP_SAI_LRCK	74VHC125	VLS
18	Ground	CDB	GND	-	-
19	SAI port SCLK	CS42518 or DSP	DSP_SAI_SCLK	74VHC125	VLS
20	Ground	CDB	GND	-	-
21	no connect	-	-	-	-
22	Ground	CDB	GND	-	-
23	CODEC port SDATA Output	CS42518	DSP_CX_SDOUT	74VHC125	VLS
24	Ground	CDB	GND	-	-
25	SAI Port SDATA Output	CS42518	DSP_SAI_SDOUT	74VHC125	VLS
26	Ground	CDB	GND	-	-
27	MCLK Direction Control	DSP	MCLK_TO_DSP-	-	-
28	Ground	CDB	GND	-	-
29	Serial Port Interface Power	CDB	VLS	-	-
30	Ground	CDB	GND	-	-
31	Serial Port Interface Power	CDB	VLS	-	-
32	Ground	CDB	GND	-	-

Table 4. CS42518 DSP Header Signals

2. INITIAL BOARD SETUP

2.1 Power Supplies

- 1) Verify that all power supplies are off before making connections.
- 2) Connect a +5.0 VDC power supply to the +5V (J47) red binding post. Select VLS and VD operating voltage by placing a jumper on J37 and J38 to select either +5V or +3.3V.
- 3) Connect a +12.0 to +18.0 VDC power supply to the +18V (J49) green binding post. If using the FILT position number 2 for the output filter stage, then supply +18.0V only.
- 4) Connect a -12.0 to -18.0 VDC power supply to the -18V (J50) yellow binding post. If using the FILT position number 2 for the output filter stage, then supply -18.0V only.
- 5) Connect the common ground of the power supplies to the GND (J48) binding post.
- 6) Attach parallel port cable between board and computer.
- 7) Attach all required analog and digital cables to the board jacks and connectors.
- 8) If using the DSP Header connection, attach the required user supplied flat ribbon cable to the header with the power supplies turned off.
- 9) If using the External Control Header connection, attach the required user supplied flat ribbon cable to the header with the power supplies turned off. Note that external controller must ground the EXT_CONTROL_PRESENT-signal to gain control of the I2C/SPI signals. This can be done easily by connecting External Control Header pins 1 and 2 together.
- 10) With all cables and connections in place, turn on the power supplies to the board. Turn on supplies in this order: +5 V, +18 V, -18 V.
- 11) Press and release the RESET switch S1. The LED, D1, will illuminate as long as S1 is depressed indicating a reset condition. Once S1 is released, the LED should turn off. If it remains on, an error has occurred. At this point, power off the power supplies and re-check all connections. Apply power to the board and press and release S1. Once the LED has turned off, the board should now be ready for setup and use.

2.2 Installing the Software

- 1) Create a directory called CDB42518 anywhere on your system.
- 2) Copy CDB425XX.EXE from the included CD into this directory.
- 3) Copy the .LVS preset script files from the CD into this directory.
- 4) Run port95nt.exe from the CD. This will install a utility that will allow the CDB software to access the parallel port. After running the program the system will need to be restarted.
- 5) If desired, create a shortcut to CDB425XX.EXE on your desktop. You should now be able to run CDB425XX.EXE. Double-click on CDB425XX.EXE or its shortcut.
- 6) Select the LPT port you are using to connect to the CDB42518.
- 7) Shut down the application, reset the board, and then restart the application.

3. CDB425XX.EXE USER'S GUIDE

3.1 Main Window

The main window of the CDB42518 control application allows the user to configure the CDB42518 inter-board routing of clocks and data, as well as setup the CS5361 and CS8406 parts. To make changes to the CS5361, CS8406, or inter-board routing, the “Configure Board” radio button must be selected.

The RESET CS425xx button will reset only the part. The MASTER RESET button will reset the CS42518, as well as reset the board into its default state.

3.2 CS425XX Window

To configure the CS42518, the “Configure CS425xx” radio button must be selected, then press the “CS425XX” button. This will bring up the complete CS42518 configuration window.

3.3 Preset Scripts

To make configuring the board and part easier, preset scripts can be saved and recalled. A preset script is a “snapshot” of all GUI board and component settings. This can be done using the File pulldown menu and choosing Load or Save. Scripts are saved with the default .LVS extension, and when loaded, will create a .LOG file. There are several preset scripts included with the software. The following sections represent three common setup modes with scripts for quick evaluation of the board.

3.4 Quick Start Preset - Analog In to Analog Out

To measure analog in to analog out performance, you will need the following:

- CS42518 Demonstration Board
- +18 VDC, -18 VDC, and +5 VDC power supplies
- Analog signal source and analyzer
- Windows compatible computer with parallel port cable and CDB425xx software

Step 1 - Follow Initial Board Setup procedure as described above

Step 2 - Select Output Filter Jumpers

Set all CDB42518 analog output filter jumpers to the FILT2 settings.

Step 3 - Connect to Windows Software

Connect the computer to the board and launch the CDB425xx software.

Step 4 - Connect Signal Source

Connect the analog output from the analyzer to the Left Analog Input J7. Connect J12 analog OUTA1 RCA to the input of the analyzer. Set the analyzer output to 1.0 VRMS, 1 kHz. Set the analyzer input to measure signal level and apply a 22-22 kHz filter.

Step 5 - Configure the Board

Using the Windows software, load the preset script “Single Speed Analog In To Analog Out.LVS”. This preset will configure the CS42518 to use OMCK as the master clock, CX and SAI ports will be masters, and the CX_SDOOUT (ADC) data will source all CX_SDIN (DAC) inputs. The left/right analog inputs will appear at all odd/even analog outputs. The single speed sample rate will be 46.875kHz based upon the 24.000MHz OMCK. You may load the similar double speed or quad speed presets to investigate higher sample rates.

Step 6 - Measure Audio

You should now have audio appearing at the Analog A1 output.

3.5 Quick Start Preset - Analog In to Digital Out

To measure the analog to digital converter performance, you will need the following:

- CS42518 Demonstration Board
- +18 VDC, -18 VDC, and +5 VDC power supplies

- Analog signal source and analyzer
- Digital signal source and analyzer
- Windows compatible computer with parallel port cable and CDB425xx software

Step 1 - Follow Initial Board Setup procedure as described above**Step 2 - Connect to Windows Software**

Connect the computer to the board and launch the CDB425xx software.

Step 3 - Connect Signal Source

Connect the analog output from the analyzer to the Left Analog Input J7. Connect the CS8406 digital output (coax J2 or optical OPT2) to the input of the analyzer. Set the analyzer output to 1.0 VRMS, 1 kHz. Set the analyzer input to measure digital signal level and apply a 22-22 kHz filter.

Step 4 - Configure the Board

Using the Windows software, load the preset script "Single Speed Analog In To Digital Out.LVS". This preset will configure the CS42518 to use OMCK as the master clock, CX and SAI ports will be masters, and the CX (ADC) clocks data will source the CS8406 inputs. The CS8406 will output the ADC digital data to both the optical and RCA jacks. The single speed sample rate will be 46.875kHz based upon the 24.000MHz OMCK. You may load the similar double speed or quad speed presets to investigate higher sample rates.

Step 5 - Measure Audio

You should now have digital audio appearing at the CX_SDOUT port and the CS8406 digital output.

3.6 Quick Start Guide - Digital In to Analog Out

To measure digital to analog performance, you will need the following:

- CS42518 Demonstration Board
- +18 VDC, -18 VDC, and +5 VDC power supplies
- Analog signal source and analyzer
- Digital signal source and analyzer
- Windows compatible computer with parallel port cable and CDB425xx software

Step 1 - Follow Initial Board Setup procedure as described above**Step 2 - Select Output Filter Jumpers**

Set all CDB42518 analog output filter jumpers to the FILT2 settings.

Step 3 - Connect to Windows Software

Connect the computer to the board and launch the CDB425xx software.

Step 4 - Connect Signal Source

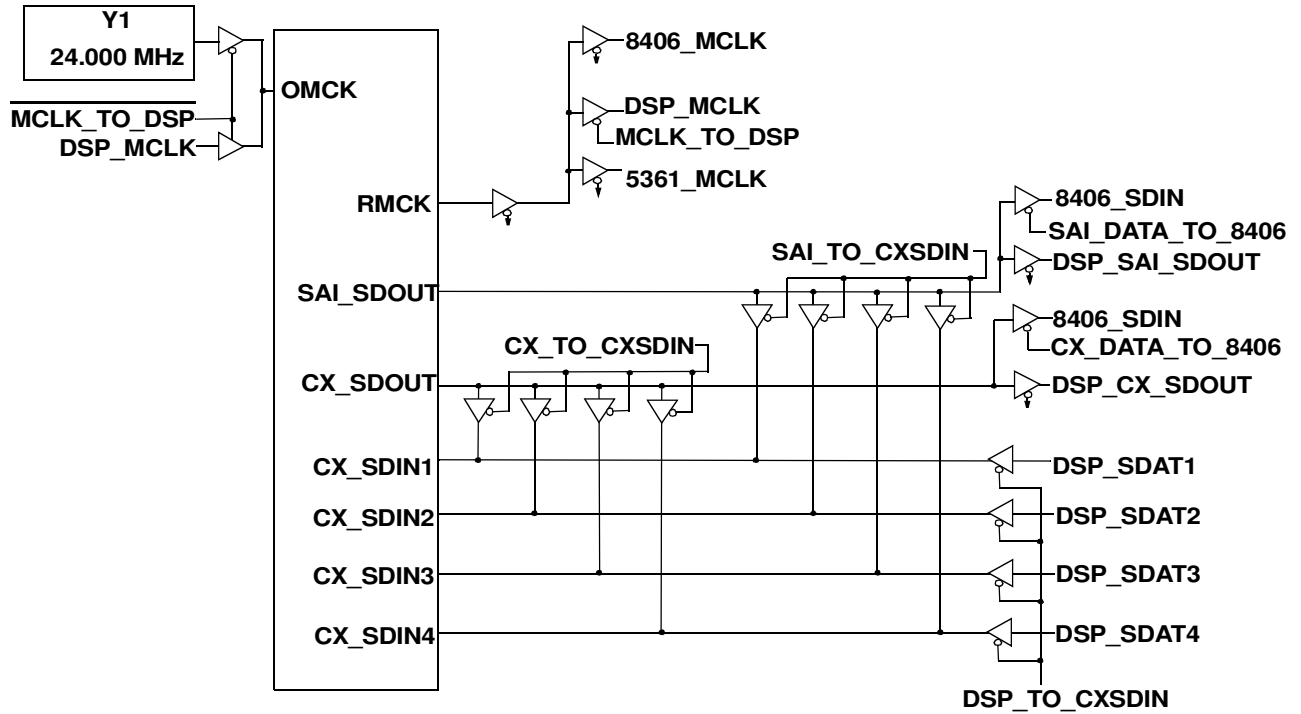
Connect the S/PDIF digital output from the analyzer to the optical input connector OPT1. Connect the analog OUTA1 RCA phono jack J12 to the input of the analyzer. Set the analyzer output to 0 dBFS, 1 kHz, sample rate at 48 kHz. Set the analyzer input to measure signal level and apply a 22-22 kHz filter.

Step 5 - Configure the Board

Using the Windows software, load the preset script "Single Speed Optical In to Analog Out.LVS". This preset will configure the CS42518 to use the recovered PLL clock as the master clock, the SAI port will be master, the CX port will be slaved to the SAI port, the SAI_SDOUT will source all CX_SDIN inputs. The test source left/right data will appear at all odd/even analog outputs. You may load the similar double speed or quad speed presets to investigate higher sample rates, but you must be sure to supply an appropriate speed SPDIF signal.

Step 6 - Measure Audio

You should now have audio appearing at the Analog A1 output.

4. BLOCK DIAGRAMS

Figure 2. MCLK and SDATA

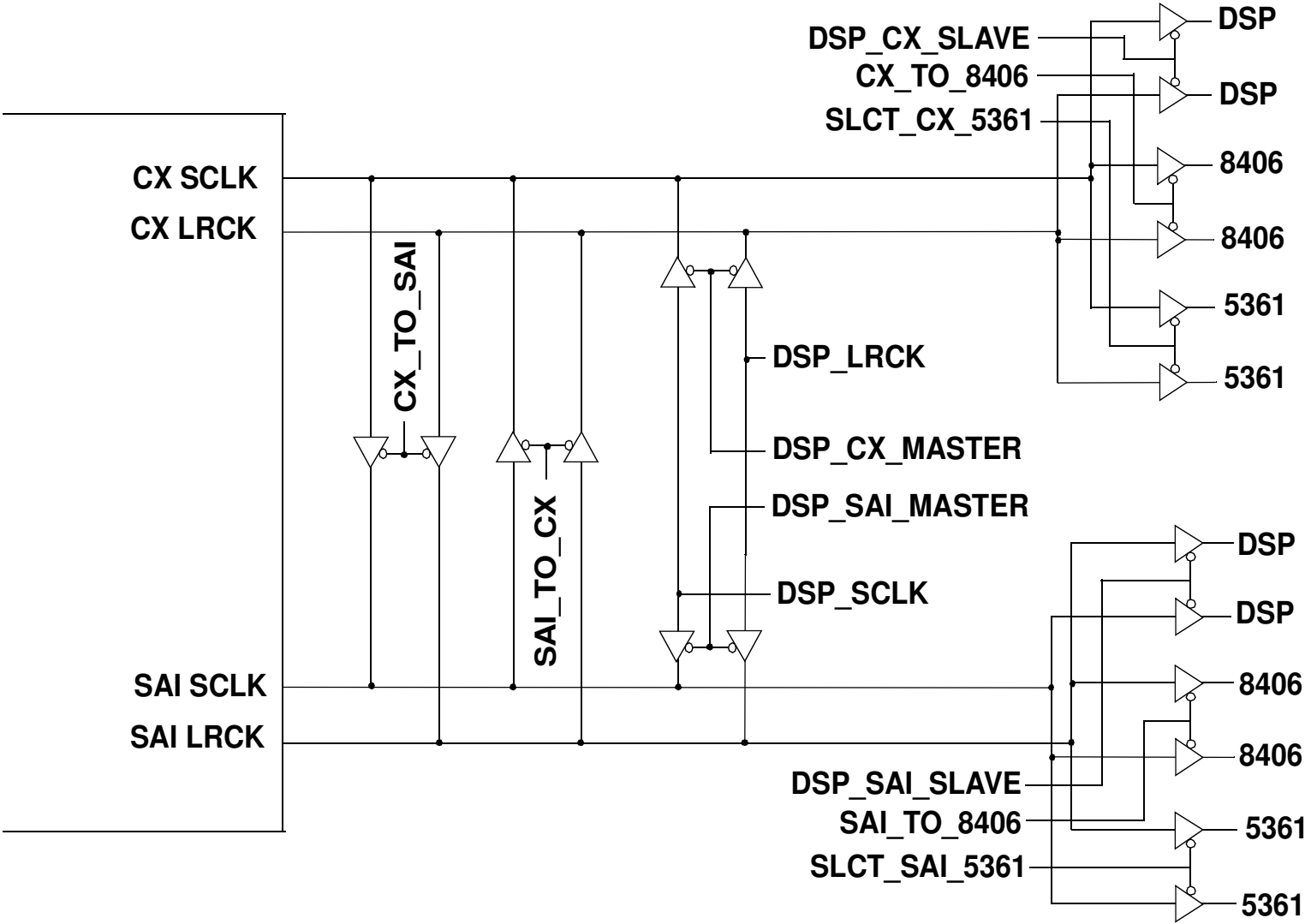
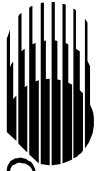
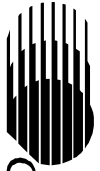


Figure 3. CX and SAI LRCK/SCLK



MUTE CONTROL	CHANNEL
$\overline{\text{EXT_MUTE}}$ and $\overline{\text{MUTE6}}$	1
$\overline{\text{EXT_MUTE}}$ and $\overline{\text{MUTE6}}$ or $\overline{\text{EXT_MUTE}}$ and GPO7	2
$\overline{\text{EXT_MUTE}}$ and $\overline{\text{MUTE6}}$ or $\overline{\text{EXT_MUTE}}$ and GPO6	3 - 8

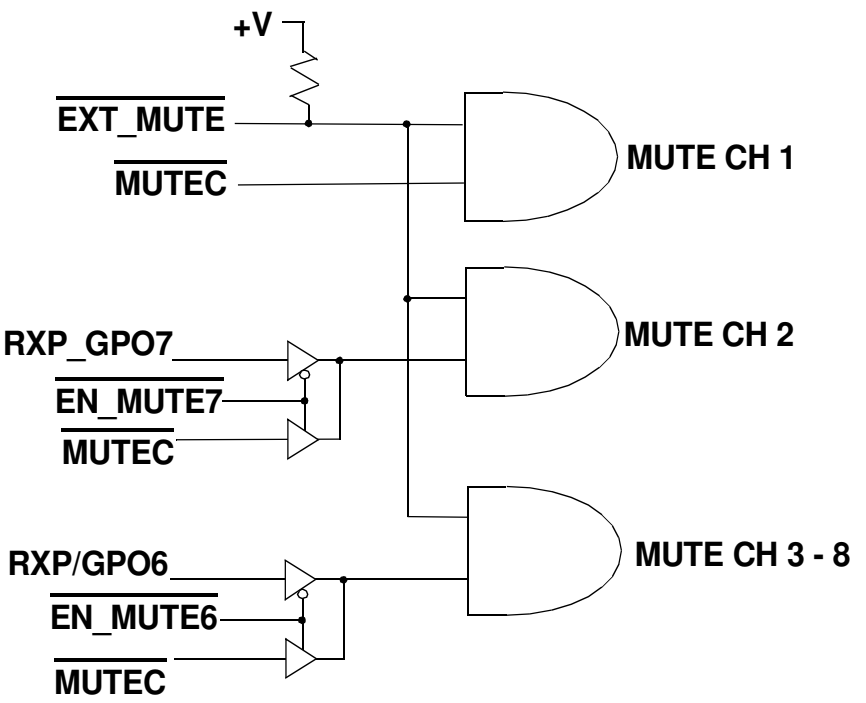


Figure 4. Output Channel Mute Select

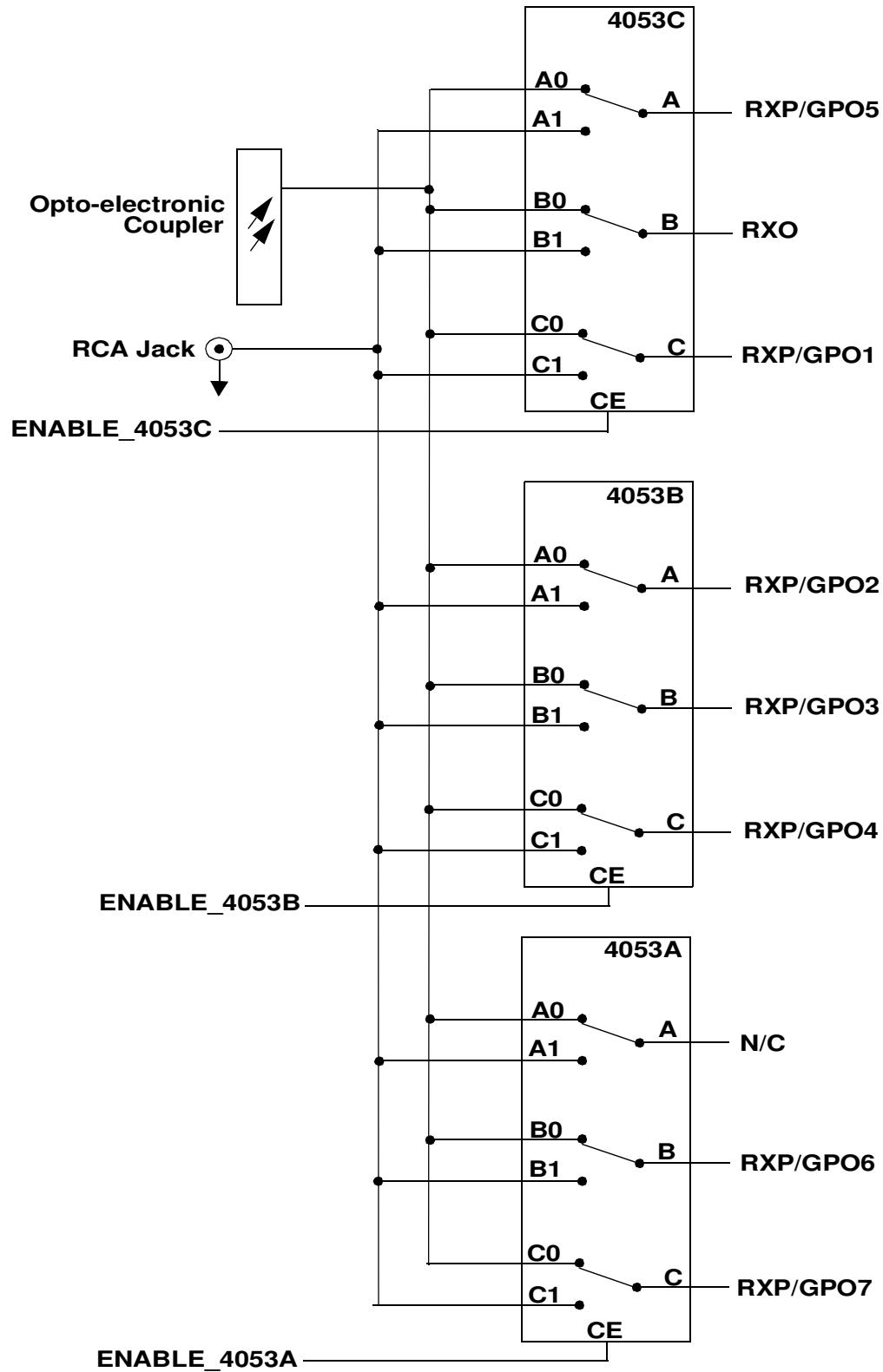
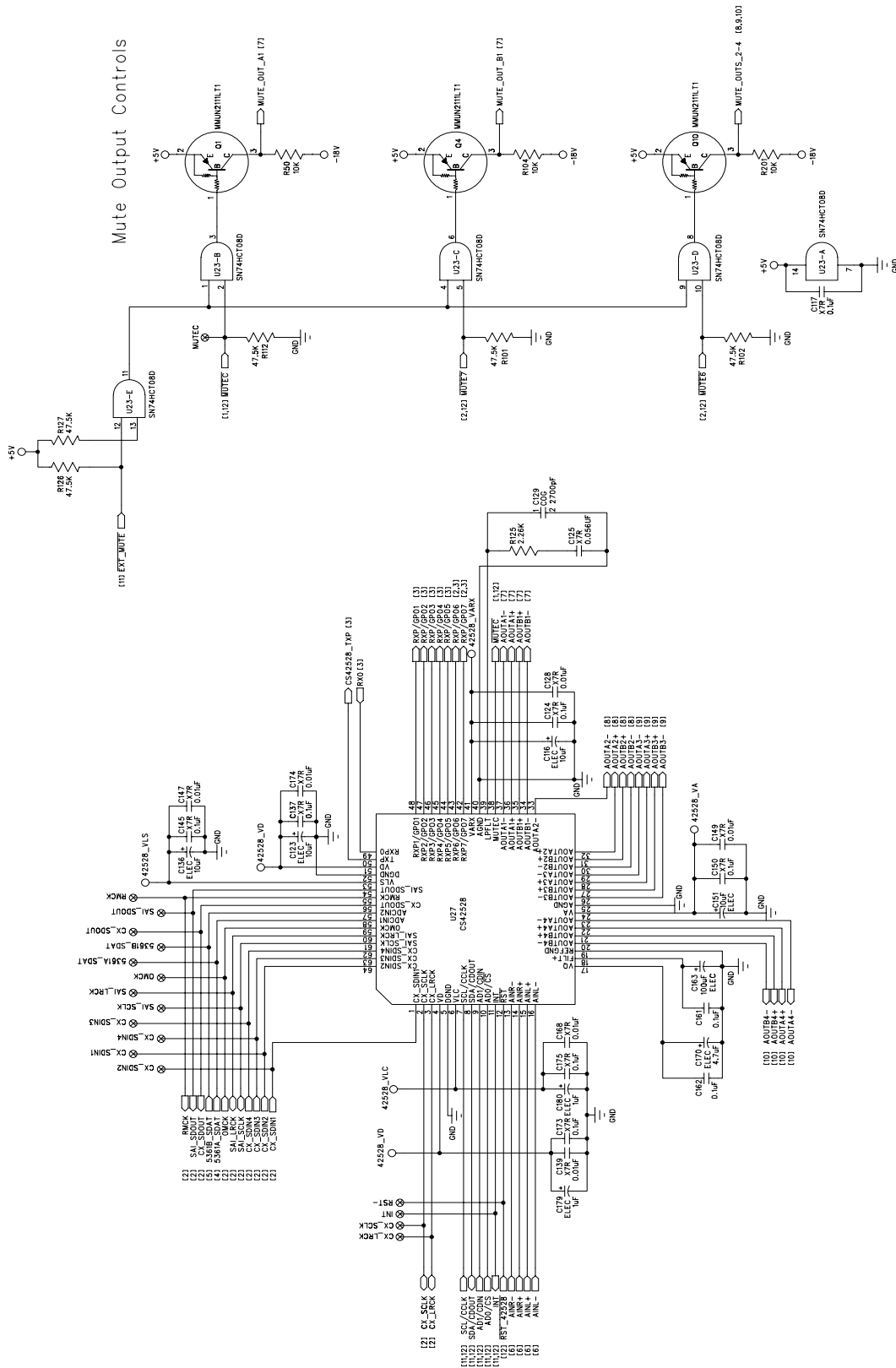


Figure 5. SPDIF Routing

5. SCHEMATICS AND LAYOUT

Figure 6. CS42518

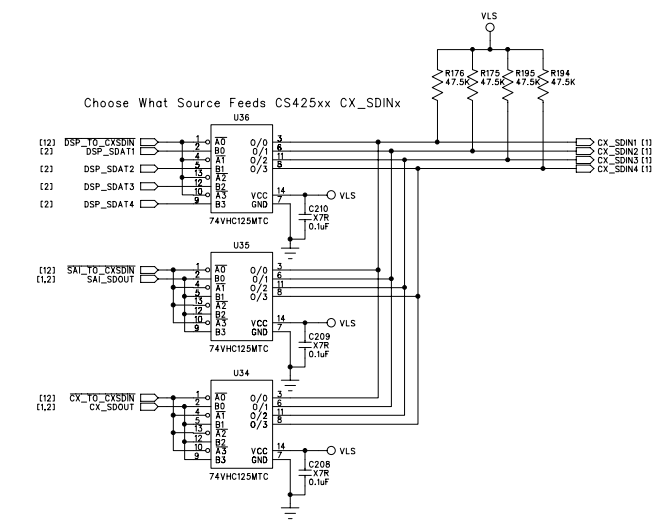
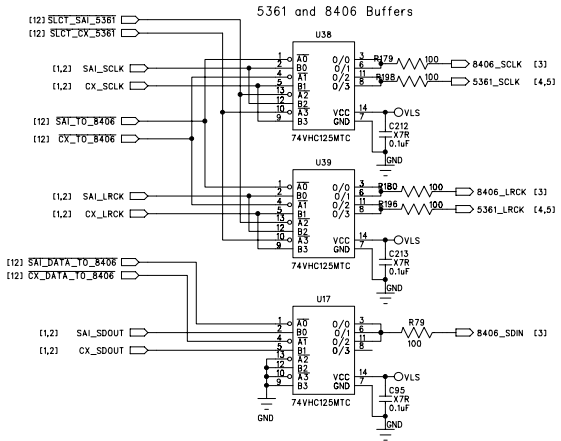
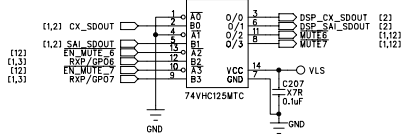
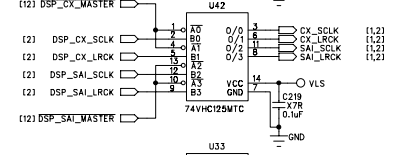
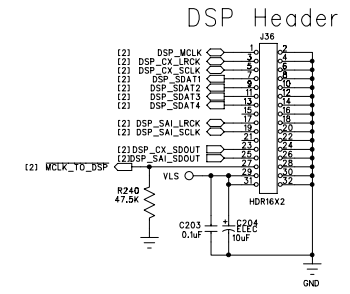
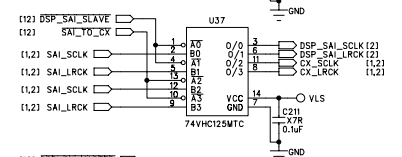
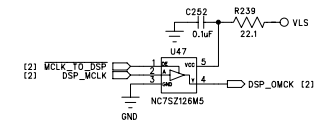
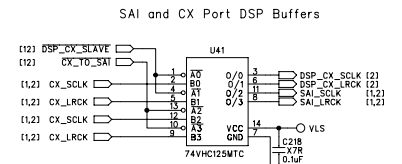
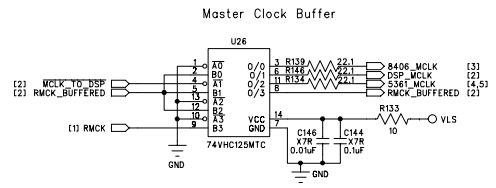
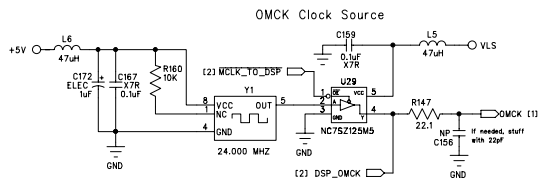
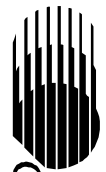
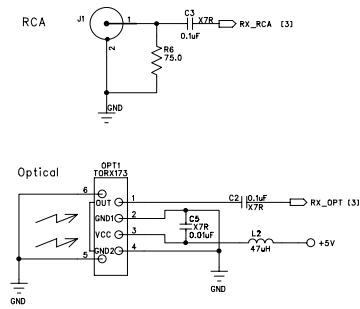
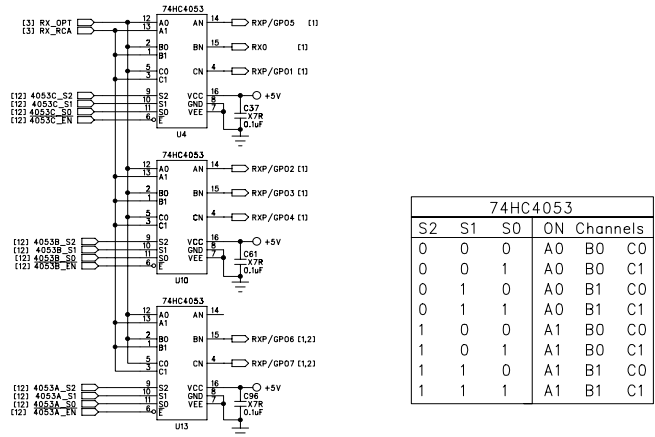


Figure 7. Clocks, Data, and DSP Header

S/PDIF Receive

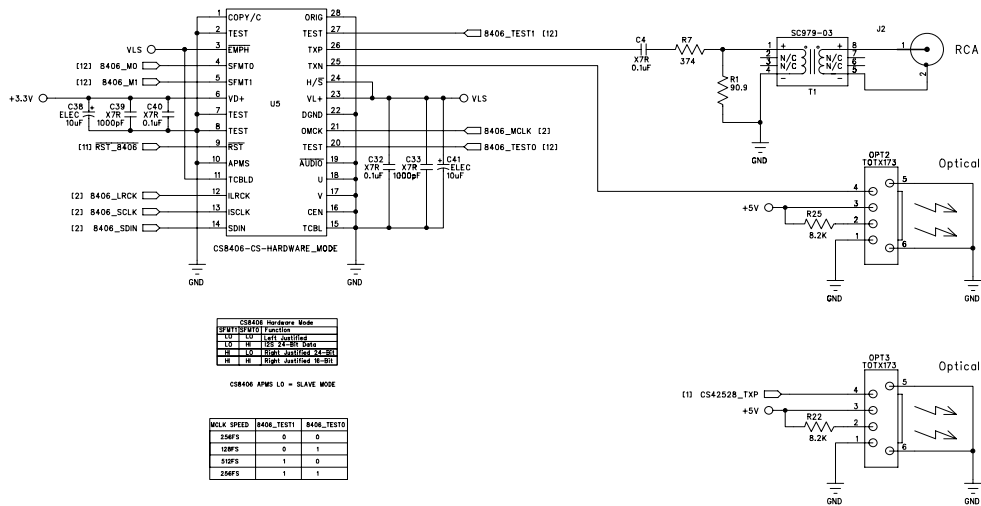


Choose What Source Feeds CS425xx SPDIF RXP1-7



74HC4053					
S2	S1	S0	ON Channels		
0	0	0	A0	B0	C0
0	0	1	A0	B0	C1
0	1	0	A0	B1	C0
0	1	1	A0	B1	C1
1	0	0	A1	B0	C0
1	0	1	A1	B0	C1
1	1	0	A1	B1	C0
1	1	1	A1	B1	C1

S/PDIF Transmit



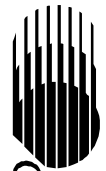
CS8406 Hardware Mode

SPDIF0/SPDIF10 Function	LO	HI	TEST	SPDIF0/SPDIF10
LO	H	L	TEST	SPDIF0/SPDIF10
HI	H	H	TEST	SPDIF0/SPDIF10
H	H	H	High Justified	LS-MSB
H	H	H	High Justified	MS-LSB

CS8406 APMS LO = SLAVE MODE

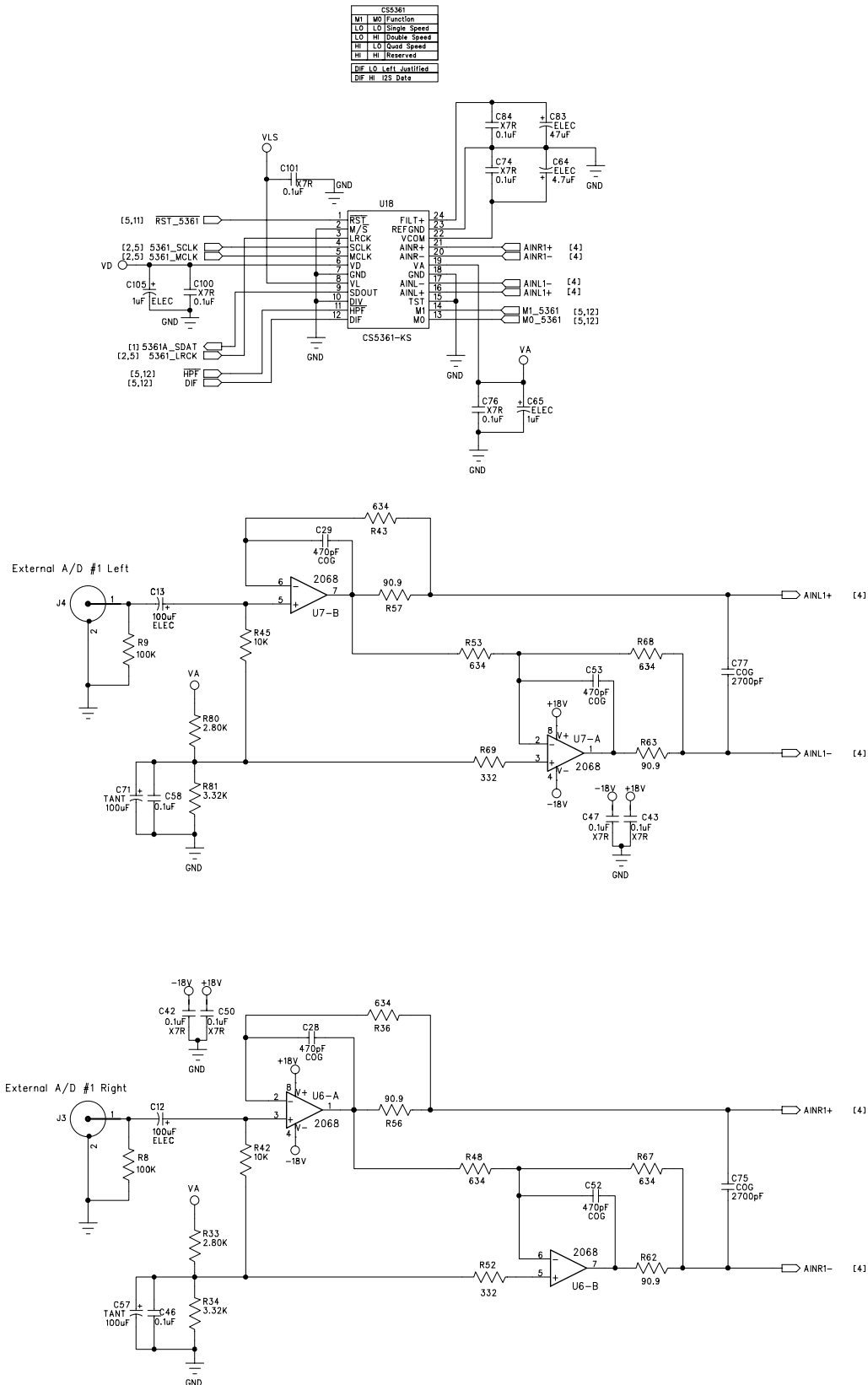
CLK SPEED	B406_TEST1	B406_TEST0
240FS	0	0
120FS	0	1
60FS	1	0
30FS	1	1

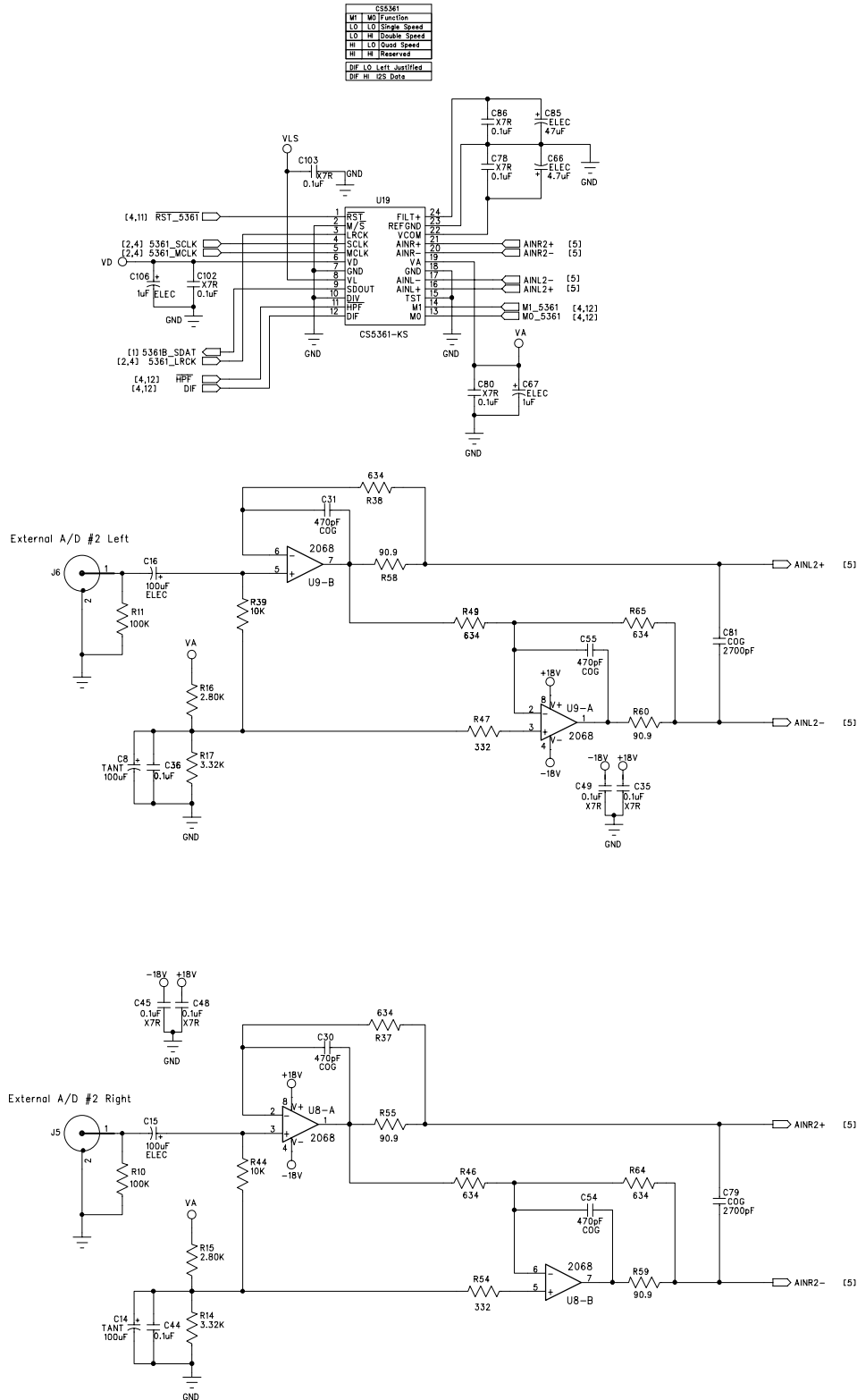
Figure 8. SPDIF



CIRRUS LOGIC®

CDB42518


Figure 9. CS5361 External ADC #1


Figure 10. CS5361 External ADC #2

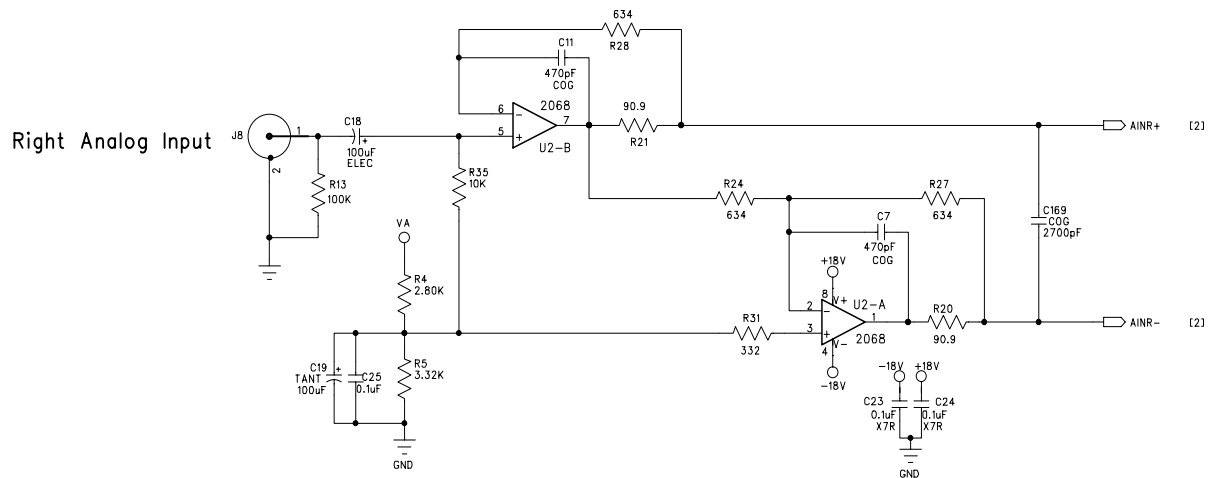
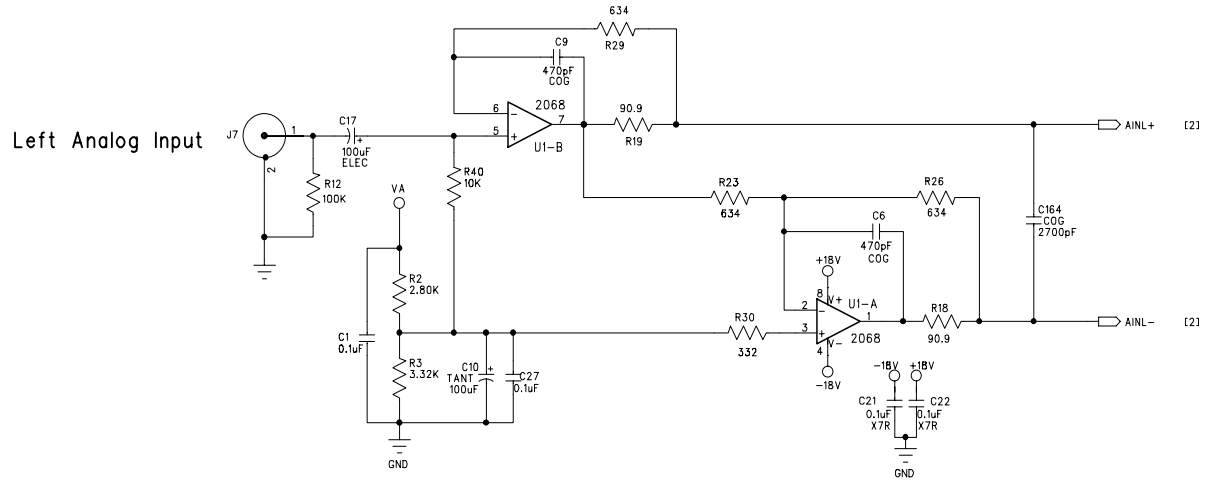


Figure 11. CS42518 Analog Inputs

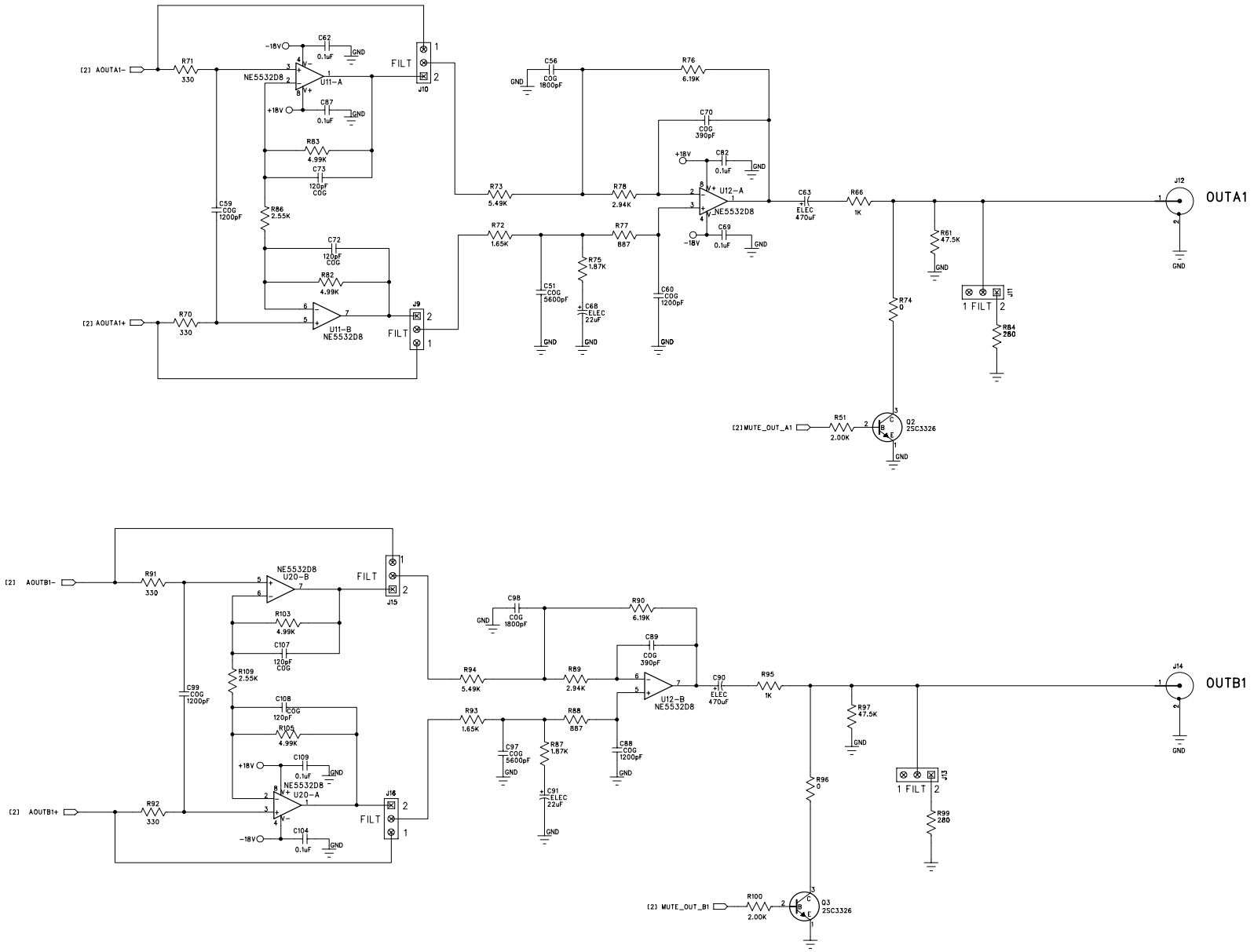


Figure 12. Analog Outputs A1 and B1



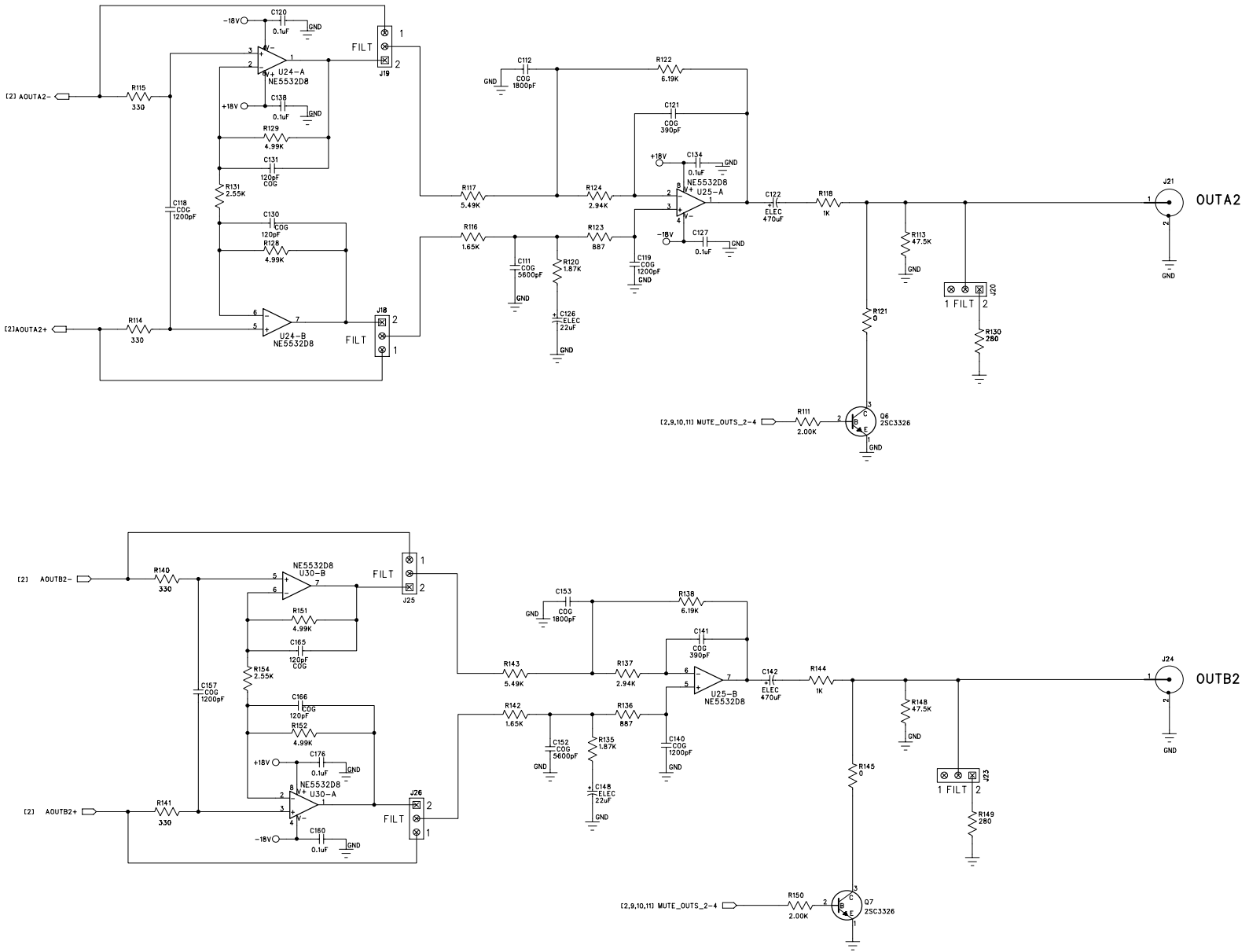
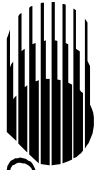


Figure 13. Analog Outputs A2 and B2

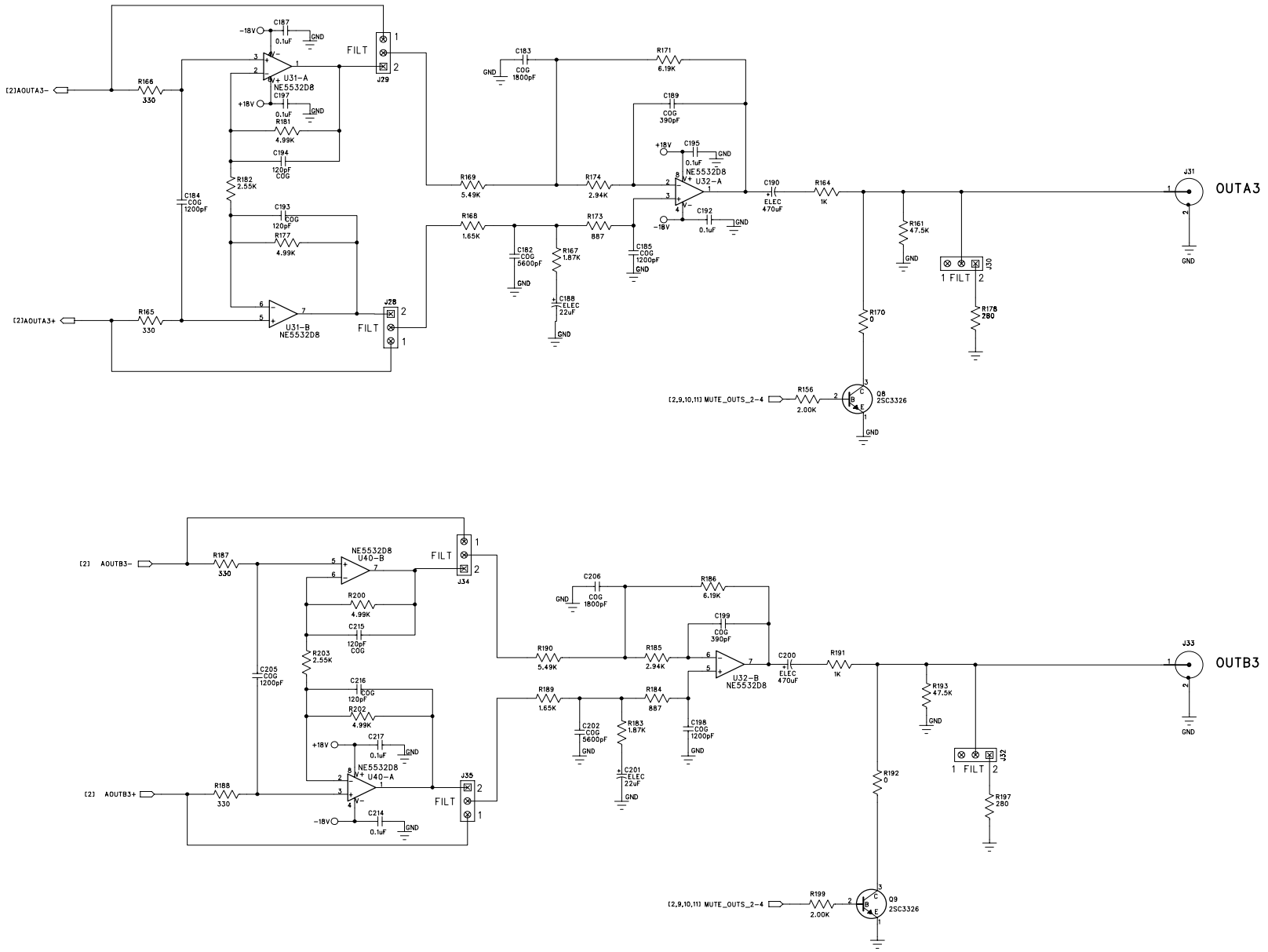


Figure 14. Analog Outputs A3 and B3



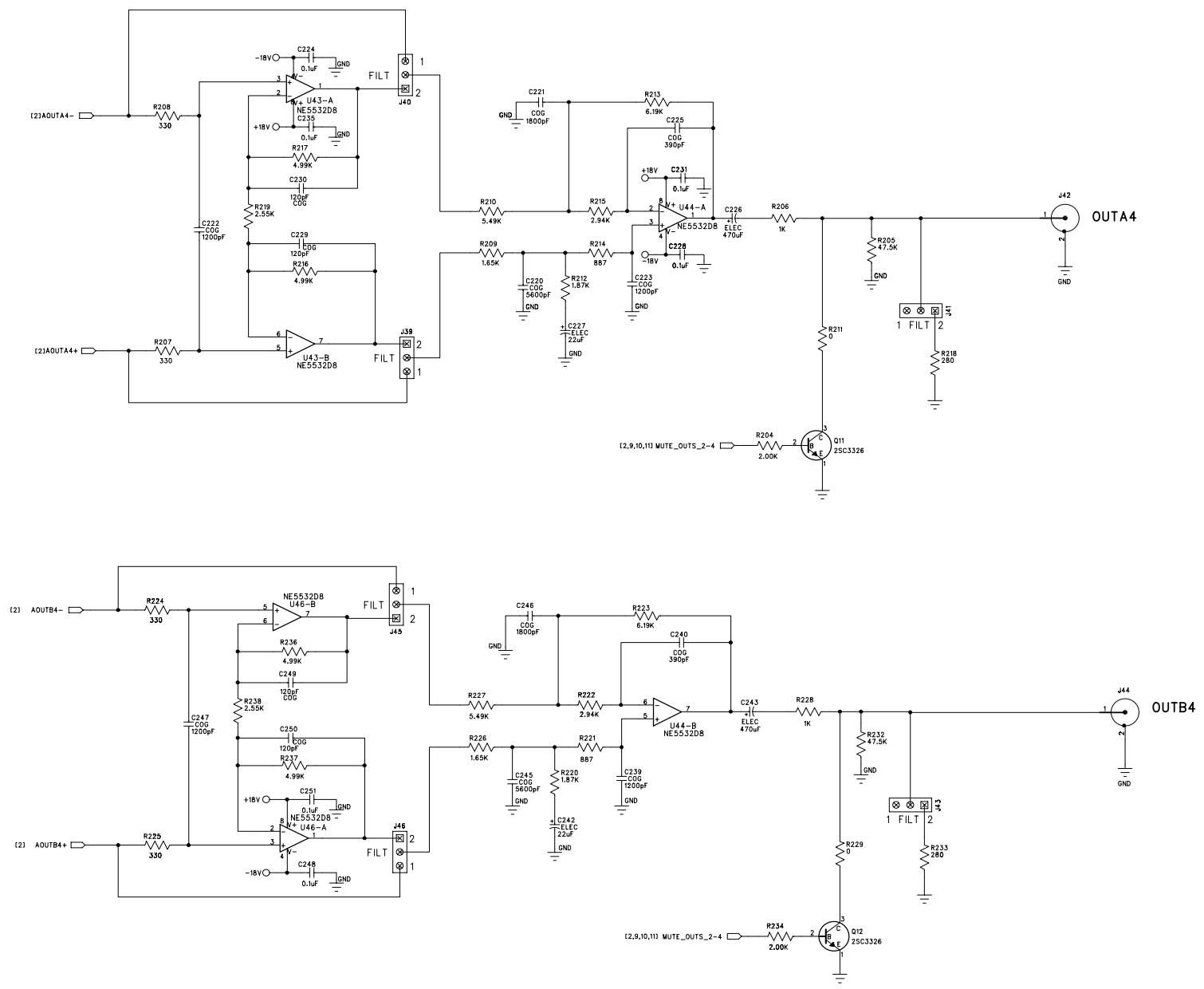
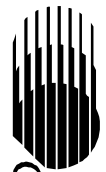


Figure 15. Analog Outputs A4 and B4