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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

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CDB4334/8/9

Evaluation Board for CS4334/8/9 Family of Products

Features

- Demonstrates recommended layout and grounding arrangements
- CS8414 Receives AES/EBU, S/PDIF, & EIAJ-340 Compatible Digital Audio
- Digital and Analog Patch Areas
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

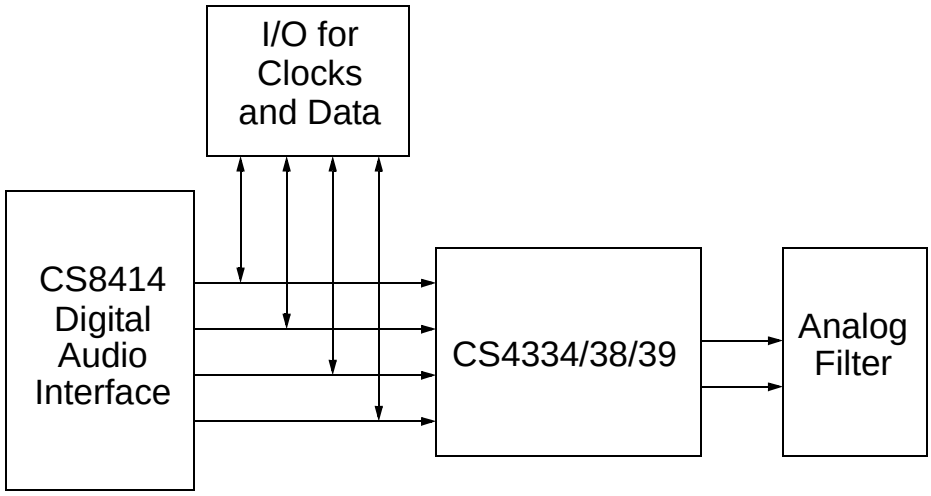
Description

The CDB4334/8/9 evaluation board is an excellent means for quickly evaluating the CS4334/8/9 family of 24-bit, stereo D/A converters. Evaluation requires an analog signal analyzer, a digital signal source and a power supply. Analog outputs are provided via RCA connectors for both channels.

The CS8414 digital audio receiver I.C. provides the system timing necessary to operate the Digital-to-Analog converters and will accept AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The evaluation board may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION

CDB4334, CDB4338, CDB4339



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

Cirrus Logic, Inc.
Crystal Semiconductor Products Division
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.crystal.com

CDB4334/8/9 SYSTEM OVERVIEW

The CDB4334/8/9 evaluation board is an excellent means of quickly evaluating the CS4334/8/9. The CS8414 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply clocks and data through a 10-pin header for system development.

The CDB4334/8/9 schematic has been partitioned into 7 schematics shown in Figures 2 through 8. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the the system diagram also includes the interconnections between the partitioned schematics.

The CS8414 does not support a compatible data format for the CS4335, CS4336 or CS4337. As a result, an evaluation board is not available for these devices. However, the evaluation board does allow external generation of clocks and data, bypassing the CS8414, and will support the CS4335/36/37 in this configuration.

CS4334/8/9 DIGITAL TO ANALOG CONVERTER

A description of the CS4334/5/6/7/8/9 is included in the CS4334/5/6/7/8/9 data sheet.

CS8414 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8414 Digital Audio Receiver, Figure 5. The outputs of the CS8414 include a serial bit clock, serial data, left-right clock (FSYNC), de-emphasis control and a 256 Fs master clock. The operation of the CS8414 and a discussion of the digital audio interface are included in the CS8414 Datasheet.

During normal operation, the CS8414 operates in the Channel Status mode where the LED's display channel status information for the channel selected by the CSLR/FCK jumper. This allows the CS8414 to decode the de-emphasis bit from the digital audio interface for control of the CS4334/8/9 de-emphasis filter.

When the Error Information Switch is activated, the CS8414 operates in the Error and Frequency information mode. The information displayed by the LED's can be decoded by consulting the CS8414 data sheet. It is likely that the de-emphasis control for the CS4334/8/9 will be erroneous and produce an incorrect audio output if the Error Information Switch is activated and the CS4334/8/9 is in the internal serial clock mode.

Encoded sample frequency information can be displayed provided a proper clock is being applied to the FCK pin of the CS8414. When an LED is lit, this indicates a "1" on the corresponding pin located on the CS8414. When an LED is off, this indicates a "0" on the corresponding pin. Neither the L or R option of CSLR/FCK should be selected if the FCK pin is being driven by a clock signal.

The evaluation board has been designed such that the input can be either optical or coax, Figure 6. However, both inputs can not be driven simultaneously.

CS8414 DATA FORMAT

The CS8414 data format can be set with jumpers M0, M1, M2, and M3, as described the CS8414 datasheet. The format selected must be compatible with the data format of the CS4334/8/9, shown in Figures 4-7 of the CS4334/8/9 datasheet. The default settings for M0-M3 on the evaluation board are given in Tables 2-4. The compatible data formats we have chosen for the CS8414 and CS4334/8/9 are:

CS8414 format 2 ; CS4334

CS8414 format 5 ; CS4338

CS8414 format 6 ; CS4339

ANALOG OUTPUT FILTER

The evaluation board includes a pair of single pole passive filters and a pair of 3-pole active filters. The passive filters are provided as an example for cost-sensitive desigins. The active filters demonstrate a higher performance alternative with better out-of-band noise rejection. The passive filters, Fig. 4, have a corner frequency of approximately 95 kHz with JP3 and JP6 installed and 190 kHz without JP3 and JP6. The 3-pole active filters are shown in Fig. 3. The output filter options are selected via the Left and Right Channel filter jumpers, Fig. 2.

INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow the interface to external systems via the 10-pin header, J9. This header allows the evaluation board to accept externally generated clocks and data. The schematic for the clock/data I/O is shown in Figure 10. The 74HC243 transceiver functions as an I/O buffer where jumpers HDR1-HDR6 determine if the transceiver operates as a transmitter or receiver. A transmit function is implemented with the HDR1-HDR6 jumpers in the 8414 position. LRCK, SDATA, and SCLK from the CS8414 will be outputs on J9. The transceiver operates as a receiver with jumpers HDR1-HDR6 in the EXTERNAL position. MCLK, LRCK, SDATA and SCLK on J9 become inputs.

GROUNDING AND POWER SUPPLY DECOUPLING

The CS4334/8/9 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 9 shows CDB power arrangements. The CDB4334/8/9 ground plane is divided in a manner to control to digital return currents in order to minimize noise. The decoupling capacitors are located as close to the CS4334/8/9 as possible. Extensive use of ground plane fill on both the analog and digital sections of the evaluation board yield large reductions in radiated noise effects.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5 V	input	+ 5 Volt power
GND	input	ground connection from power supply
Digital input	input	digital audio interface input via coax
Optical input	input	digital audio interface input via optical
Digital I/O	input/output	I/O for master, serial, left/right clocks and serial data
AOUTLA	output	left channel analog output with 3-pole active filter
AOUTRA	output	right channel analog output with 3-pole active filter
AOUTLP	output	left channel analog output with single-pole passive filter
AOUTRP	output	right channel analog output with single-pole passive filter

Table 1. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
CSLR/FCK	Selects channel for CS8414 channel status information	HI LO	See CS8414 Datasheet for details
M0 M1 M2 M3	CS8414 mode selection	*Low *High *Low *Low	See CS8414 Datasheet for details
SCLK	Selects SCLK Mode	INT *EXT	Internal SCLK Mode External SCLK Mode
DEM_8414	Selects source of de-emphasis control	*8414 DEM	CS8414 de-emphasis De-emphasis input static high
HDR1-6	Selects source of clocks and audio data	*8414 EXT	Selects CS8414 as source Digital I/O header becomes an source
MCLK	Selects High-Rate or Base-Rate Modes	x1 ÷2	Selects Base Rate Mode Selects High Rate Mode
Left Channel Filter	Selects Active 3-pole or passive single-pole filter	Active Passive	Selects 3-pole active filter Selects Single-pole passive filter
Right Channel Filter	Selects Active 3-pole or passive single-pole filter	Active Passive	Selects 3-pole active filter Selects Single-pole passive filter

*Default setting from factory

Notes: The CS8414 data format requires the CS4334 to operate in the external serial clock mode.

Table 2. CDB4334 Jumper Selectable Options

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
CSLR/FCK	Selects channel for CS8414 channel status information	HI LO	See CS8414 Datasheet for details
M0 M1 M2 M3	CS8414 mode selection	*High *Low *High *Low	See CS8414 Datasheet for details
SCLK	Selects SCLK Mode	INT *EXT	Internal SCLK Mode External SCLK Mode
DEM_8414	Selects source of de-emphasis control	*8414 DEM	CS8414 de-emphasis De-emphasis input static high
HDR1-6	Selects source of clocks and audio data	*8414 EXT	Selects CS8414 as source Digital I/O header becomes an source
MCLK	Selects High-Rate or Base-Rate Modes	x1 ÷2	Selects Base Rate Mode Selects High Rate Mode
Left Channel Filter	Selects Active 3-pole or passive single-pole filter	Active Passive	Selects 3-pole active filter Selects Single-pole passive filter
Right Channel Filter	Selects Active 3-pole or passive single-pole filter	Active Passive	Selects 3-pole active filter Selects Single-pole passive filter

*Default setting from factory

Notes: The CS8414 data format requires the CS4338 to operate in the external serial clock mode.

Table 3. CDB4338 Jumper Selectable Options

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
CSLR/FCK	Selects channel for CS8414 channel status information	HI LO	See CS8414 Datasheet for details
M0 M1 M2 M3	CS8414 mode selection	*Low *High *High *Low	See CS8414 Datasheet for details
SCLK	Selects SCLK Mode	INT *EXT	Internal SCLK Mode External SCLK Mode
DEM_8414	Selects source of de-emphasis control	*8414 DEM	CS8414 de-emphasis De-emphasis input static high
HDR1-6	Selects source of clocks and audio data	*8414 EXT	Selects CS8414 as source Digital I/O header becomes an source
MCLK	Selects High-Rate or Base-Rate Modes	x1 ÷2	Selects Base Rate Mode Selects High Rate Mode
Left Channel Filter	Selects Active 3-pole or passive single-pole filter	Active Passive	Selects 3-pole active filter Selects Single-pole passive filter
Right Channel Filter	Selects Active 3-pole or passive single-pole filter	Active Passive	Selects 3-pole active filter Selects Single-pole passive filter

*Default setting from factory

Table 4. CDB4339 Jumper Selectable Options

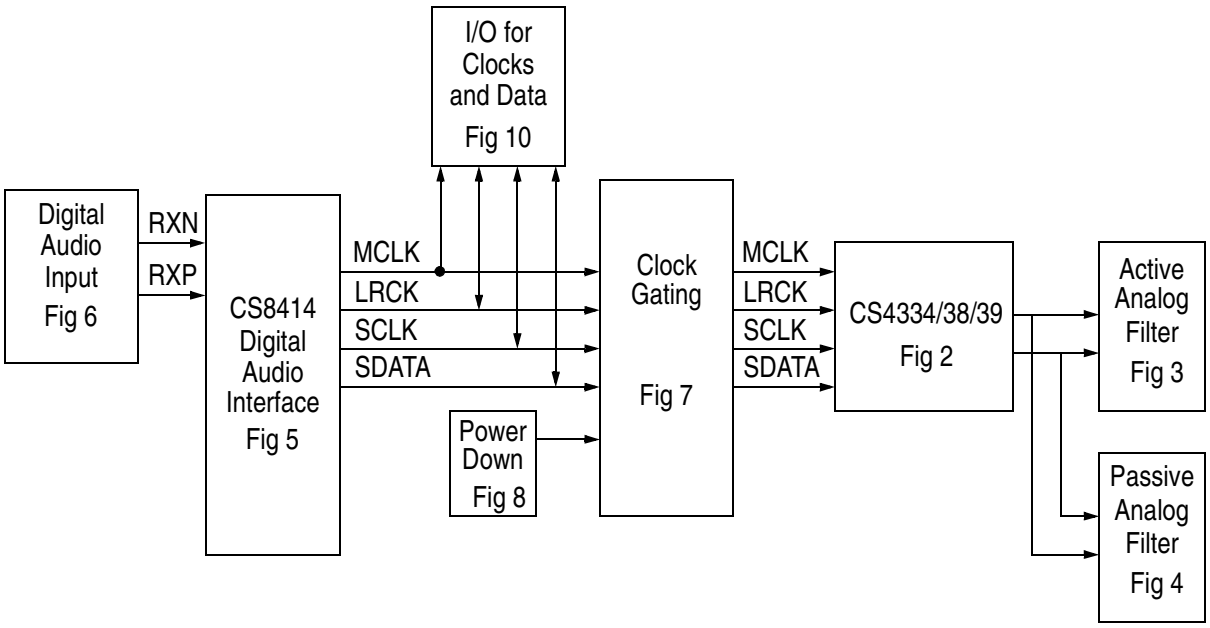


Figure 1. System Block Diagram and Signal Flow

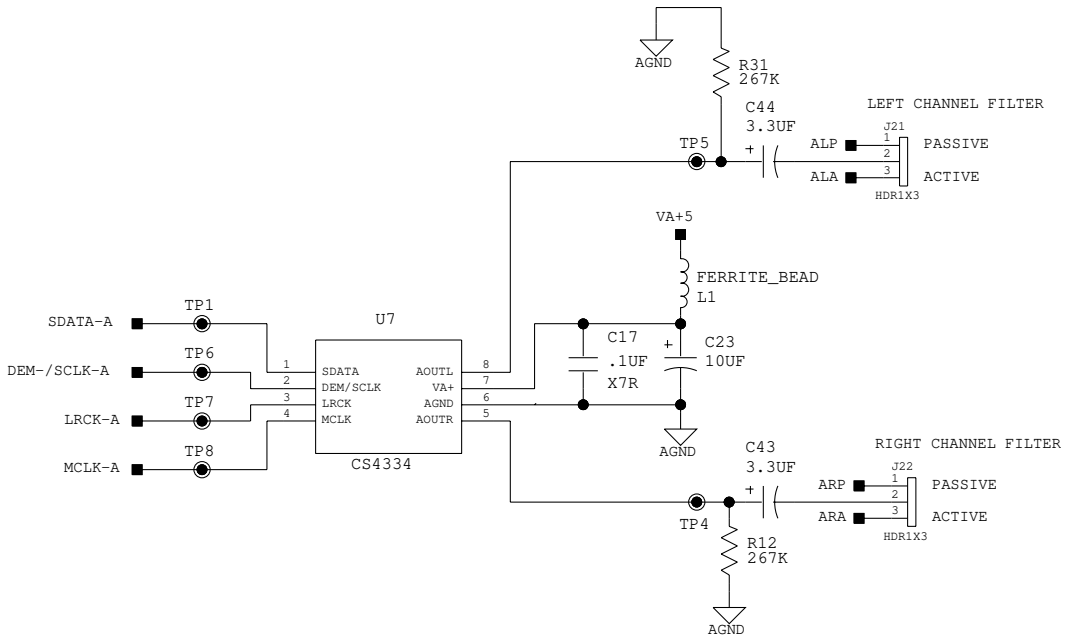


Figure 2. CS4334/5/6/7/8/9

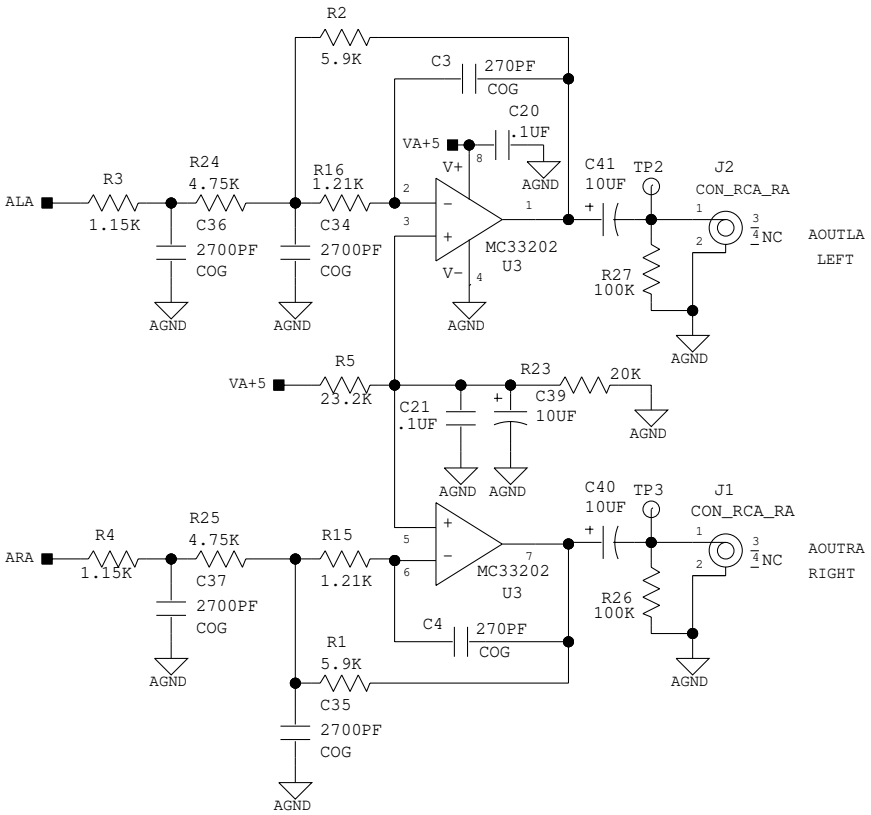


Figure 3. Analog Output Active Filter

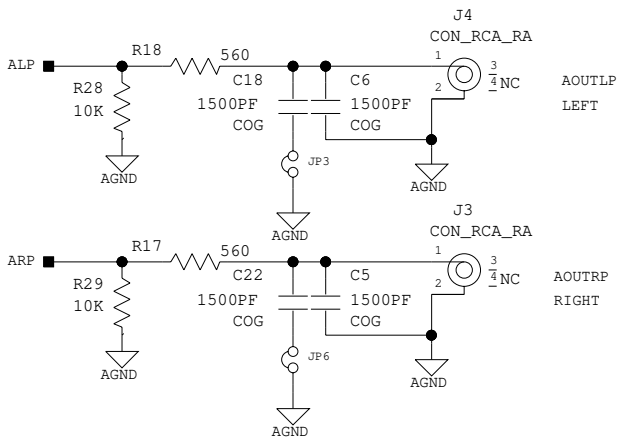


Figure 4. Analog Output Passive Filter

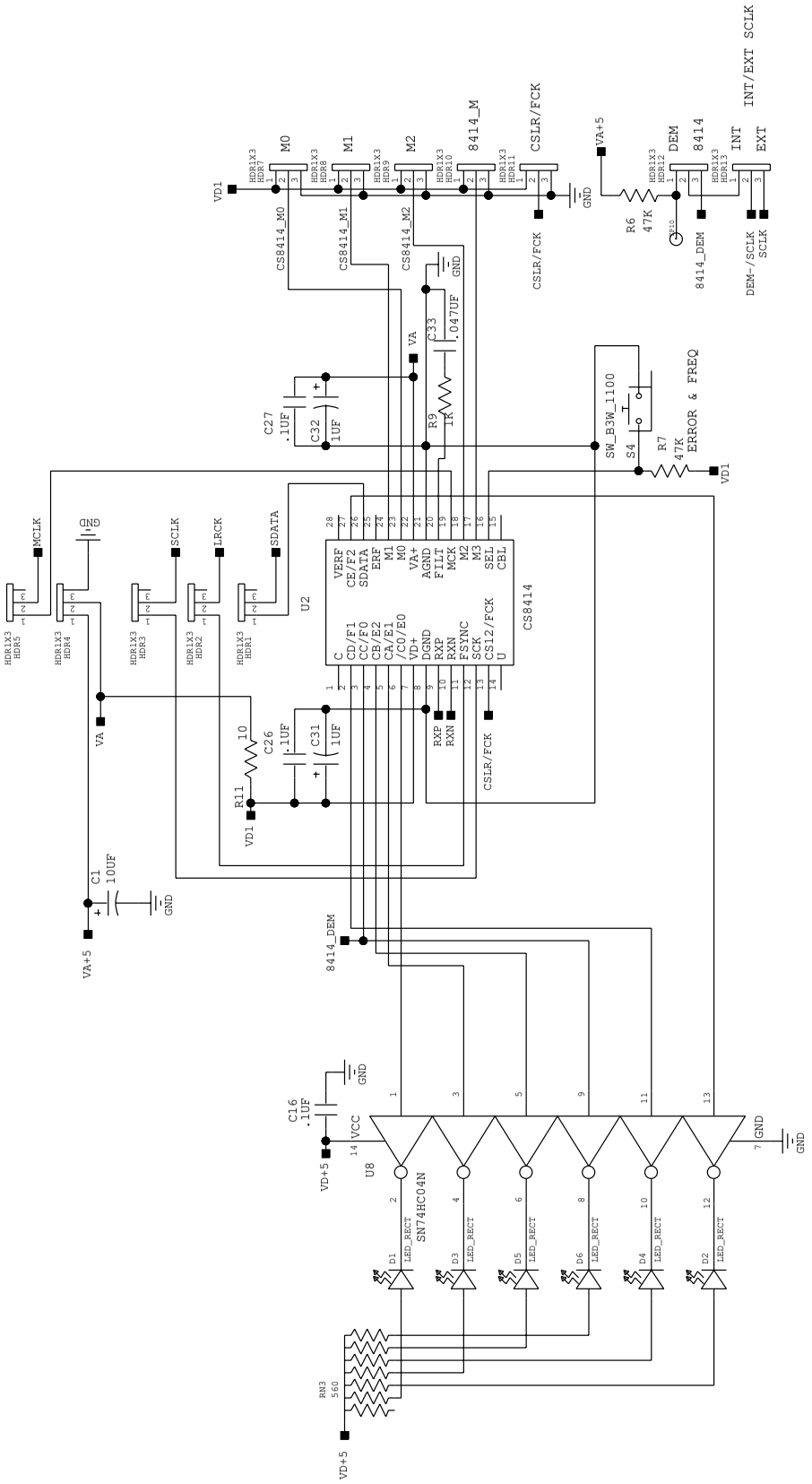


Figure 5. CS8414 Digital Audio Receiver Connections

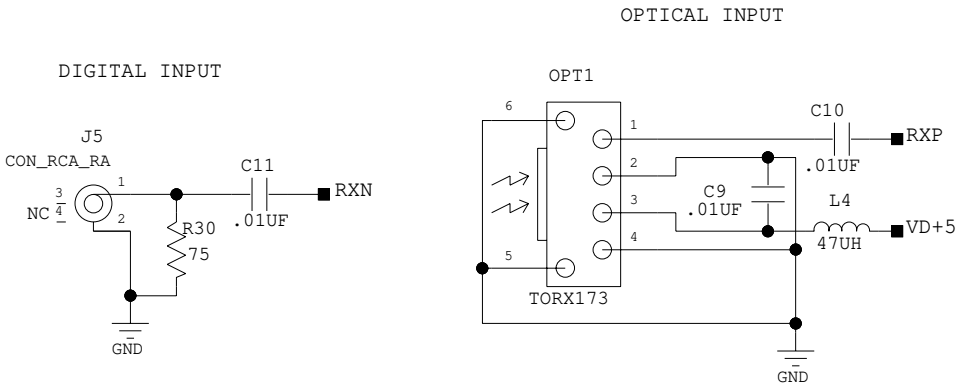


Figure 6. Digital Audio Inputs

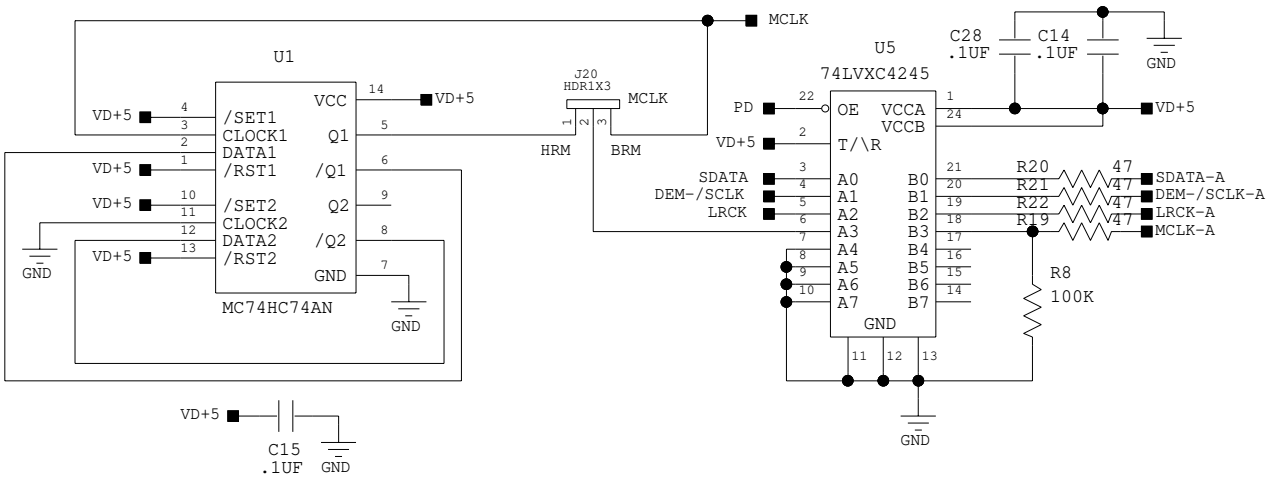


Figure 7. MCLK Divider and Clock Gating

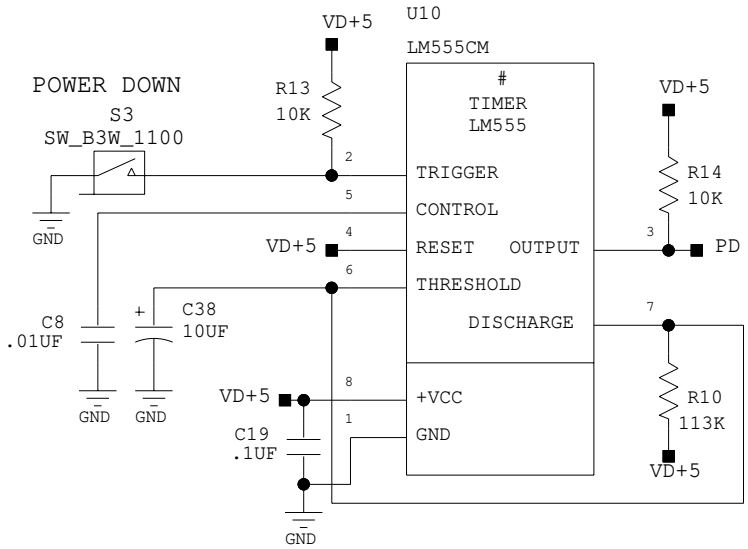


Figure 8. Power Down Circuitry

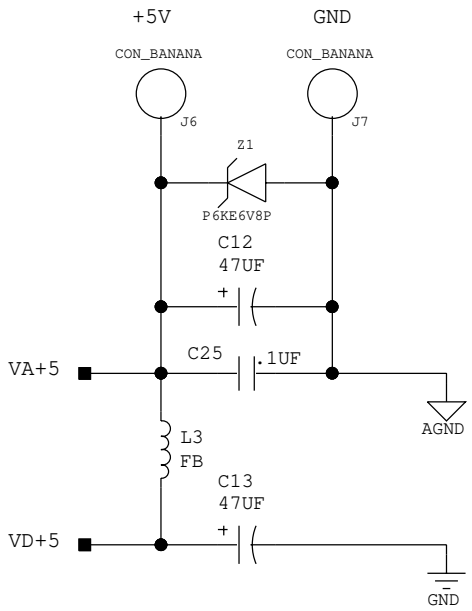


Figure 9. Power Supply

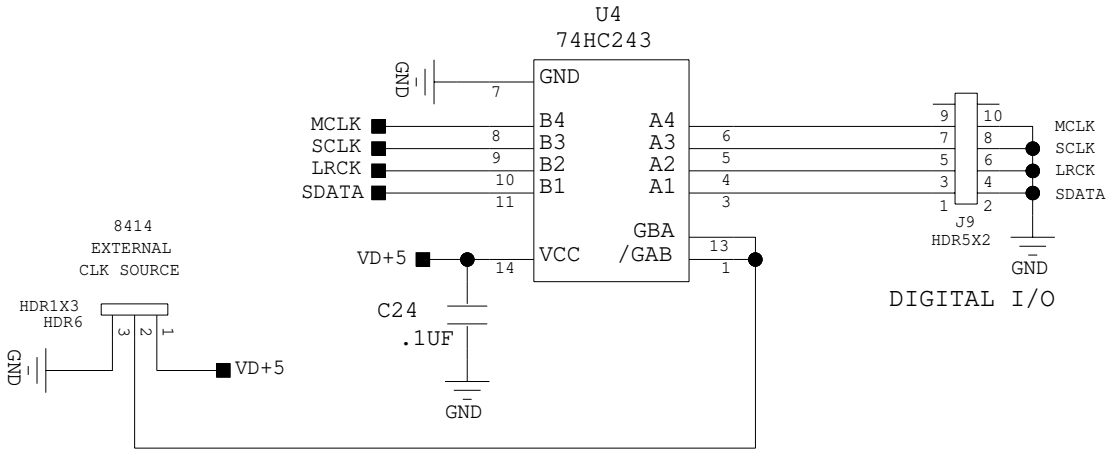


Figure 10. I/O for Clocks and Data

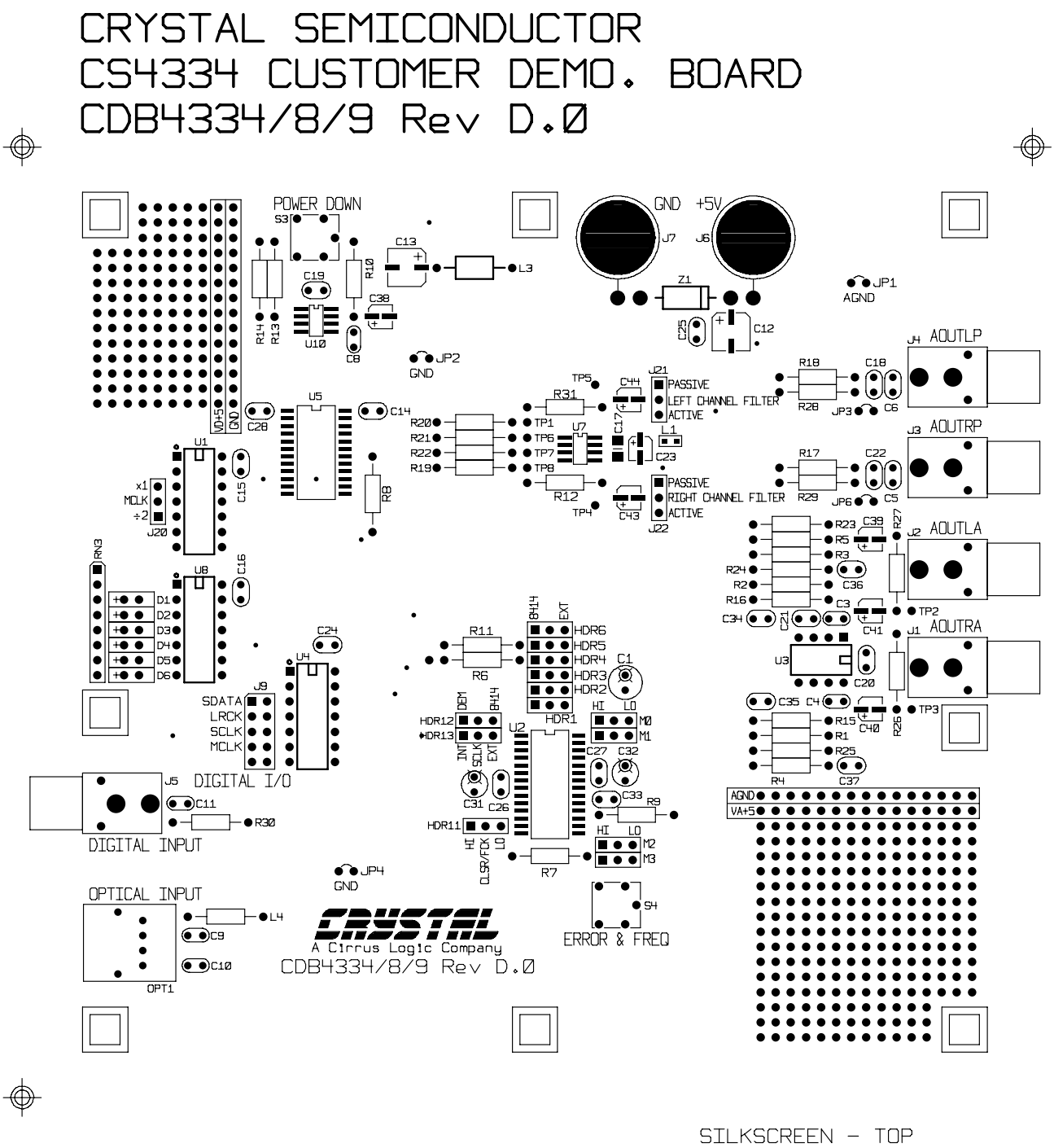
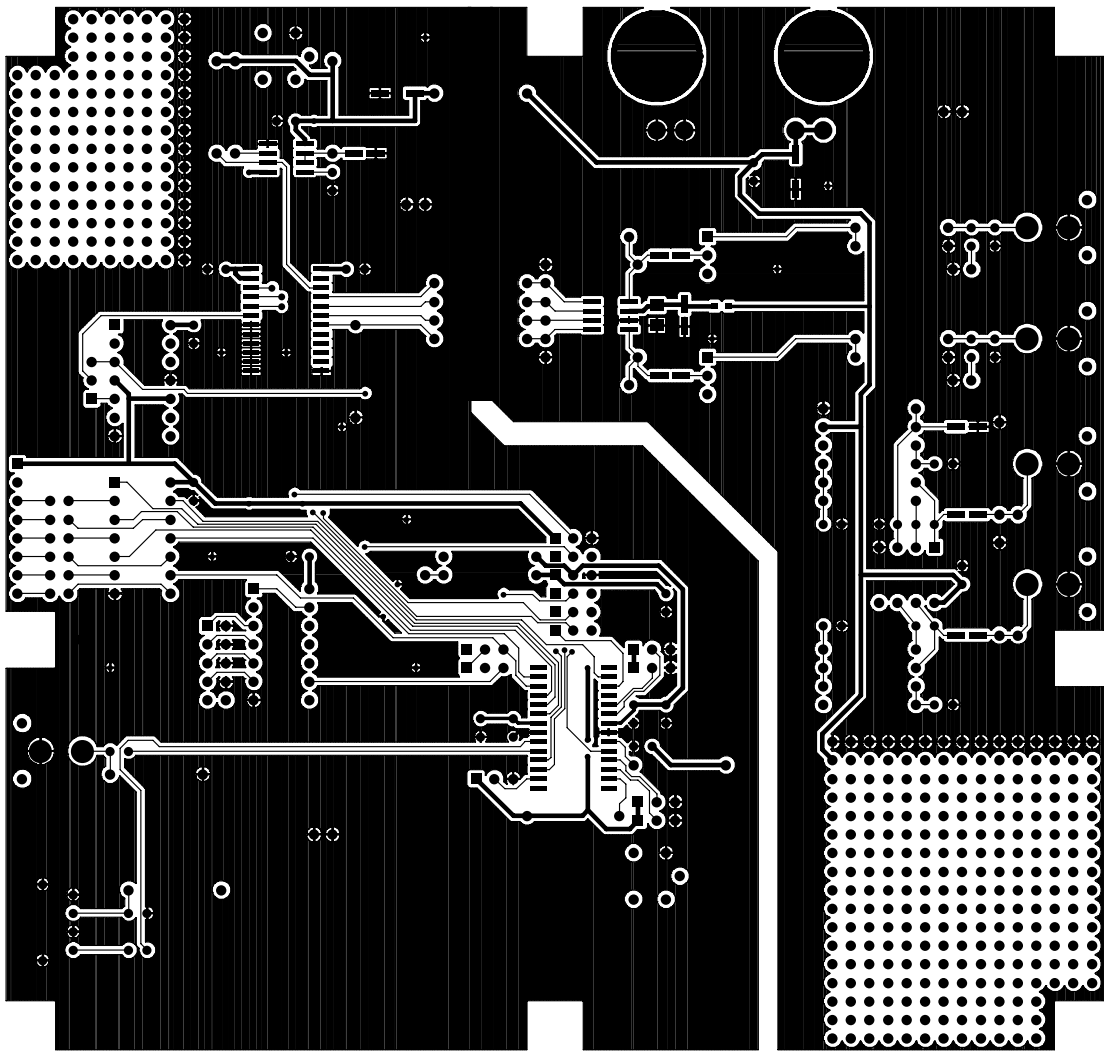


Figure 11. Silkscreen Top

CRYSTAL SEMICONDUCTOR
CS4334 CUSTOMER DEMO. BOARD
CDB4334/8/9 Rev D.0



TOP SIDE

Figure 12. Top Side

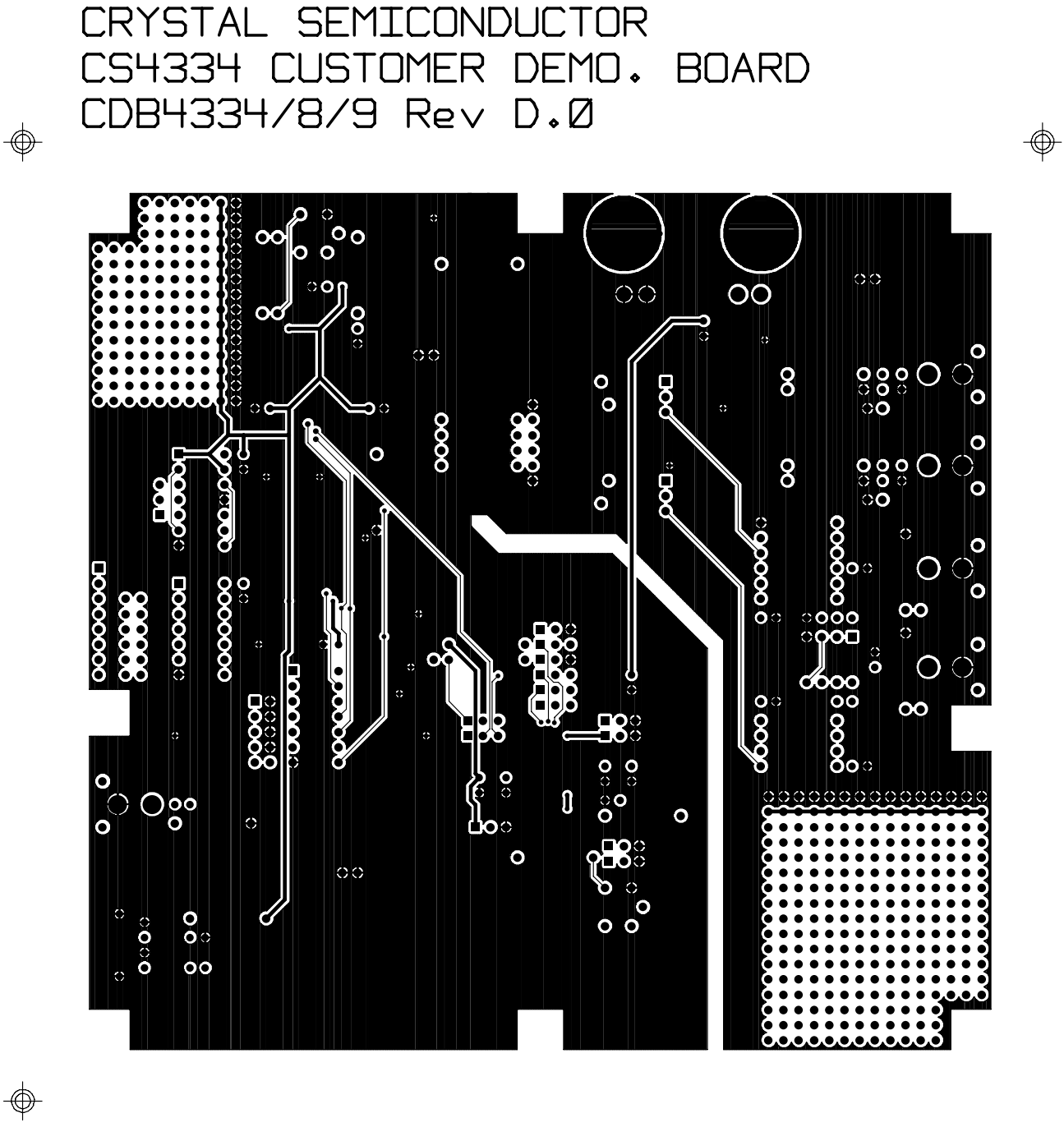


Figure 13. Bottom Side