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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## Evaluation Board for CS4344

### Features

- Demonstrates recommended layout and grounding arrangements
- CS8416 receives S/PDIF, & EIAJ-340 compatible digital audio
- Header for external PCM audio
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

### Description

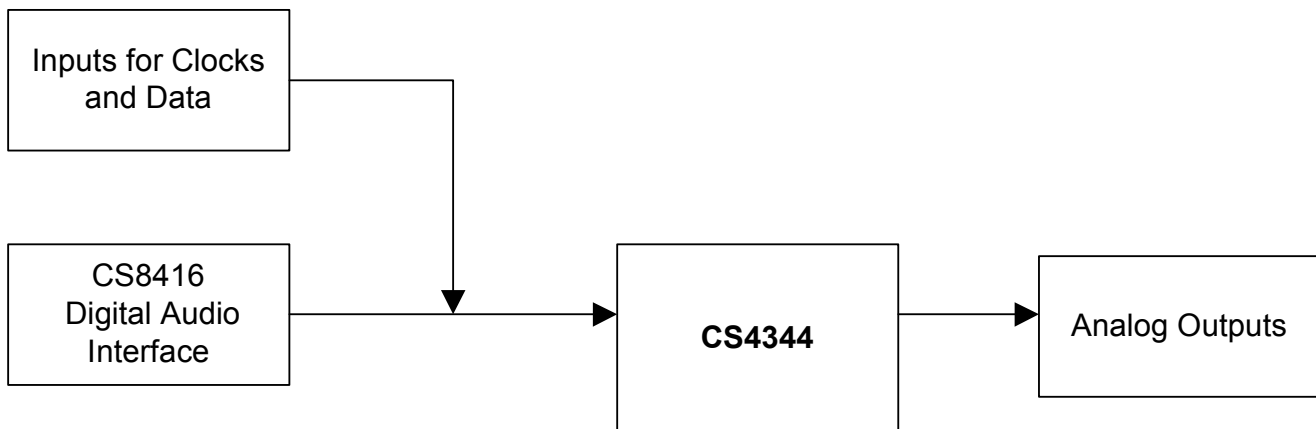
The CDB4344 evaluation board is an excellent means for quickly evaluating the CS4344 24-bit, 10 pin stereo D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, and a power supply. Analog line level outputs are provided via RCA phono jacks.

The CS8416 digital audio receiver I.C. provides the system timing necessary to operate the Digital-to-Analog converter and will accept S/PDIF, and EIAJ-340-compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

### ORDERING INFORMATION

CDB4344

Evaluation Board



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## CDB4344 SYSTEM OVERVIEW

The CDB4344 evaluation board is an excellent means of quickly evaluating the CS4344. The CS8416 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply external PCM clocks and data through a header for system development.

The CDB4344 schematic has been partitioned into 4 schematics shown in Figures 2 through 5. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

### 1. CS4344 DIGITAL TO ANALOG CONVERTER

A description of the CS4344 is included in the CS4344 datasheet.

### 2. CS8416 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8416 Digital Audio Receiver, Figure 3. The outputs of the CS8416 include a serial bit clock, serial data, left-right clock, and a 128/256 Fs master clock. The CS8416 data format is fixed to I<sup>2</sup>S (can be changed with R42 and R47). The operation of the CS8416 and a discussion of the digital audio interface is included in the CS8416 datasheet.

The evaluation board has been designed such that the input can be either optical or coax, see Figure 3. However, both inputs cannot be driven simultaneously.

The right hand switch of S2 sets the output MCLK to LRCK ratio of the CS8416. This switch should be set to 256 (closed) for inputs  $F_s \leq 96$  kHz and 128 (open) for  $F_s \geq 64$  kHz. The 8416 must be manually reset using RX\_RST (S1) when this switch is changed.

### 3. INPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the header J9. Header J9 allows the evaluation board to accept externally generated PCM clocks and data. The schematic for the clock/data input is shown in Figure 4. The left hand switch of S2 selects the source as either CS8416 (closed) or header J9 (open).

Please see the CS4344 datasheet for more information.

### 4. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by three binding posts (GND, +5V, and '+3.3V to +5V'), see Figure 5. The '+3.3V to +5V' which supplies VA can be jumpered to a +3.3 V regulator or the +5V binding post. The VA supply should be set to the recommended values stated in the CS4344 datasheet.

**WARNING:** Refer to the CS4344 datasheet for maximum allowable voltages levels. Operation outside of this range can cause permanent damage to the device.

## 5. GROUNDING AND POWER SUPPLY DECOUPLING

As with any high performance converter, the CS4344 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 2 details the connections to the CS4344 and Figures 6, 7, and 8 show the component placement and top and bottom layout. The decoupling capacitors are located as close to the CS4344 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

## 6. ANALOG OUTPUT FILTERING

The analog output on the CDB4344 has been designed according to the CS4344 datasheet. This output circuit includes an AC coupling cap and a single pole R and C. An additional load resistance may be added by stuffing R10 and R26 to test the CS4344's load driving capability.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5V	Input	+ 5 V power
GND	Input	Ground connection from power supply
+3.3V to +5V	Input	+3.3 V to +5 V positive supply for the CS4344 VA power
S/PDIF INPUT - J5	Input	Digital audio interface input via coax
S/PDIF INPUT - OPT1	Input	Digital audio interface input via optical
PCM INPUT - J9	Input	Input for master, serial, left/right clocks and serial data
LEFT_OUT and RIGHT_OUT	Output	RCA line level analog outputs

**Table 1. System Connections**

JUMPER / SWITCH	PURPOSE	POSITION	FUNCTION SELECTED
J4	Selects source of voltage for the CS4344 VA supply	VA +3.3V *+5V	Voltage source is the +3.3V to +5V binding post Voltage source is a +3.3V regulator Voltage source is +5V binding post
J7	Provides contact points to measure current	-	Measure voltage across these nodes and divide result by 10 to get current in Amps
S1	Resets CS8416		The CS8416 must be reset if switch S2 is changed
S2	Sets clock source	left	Sets clock source for CS4344 (open=J9, *closed = CS8416)
	Sets MCLK ratio of CS8416	right	Selects 128x (open) or 256x (*closed) MCLK/LRCK ratio output for CS8416

**Table 2. CDB4344 Jumper Settings**

\*Default Factory Settings.

## 7. ERRATA

### CDB4344 Revision B.0

Switch S2 is oriented incorrectly on some boards (if open is away from binding posts) and thus the 0 and 1 labels above and below are incorrect. Using closed for 0 and open for 1, the table next to the switch will be correct.

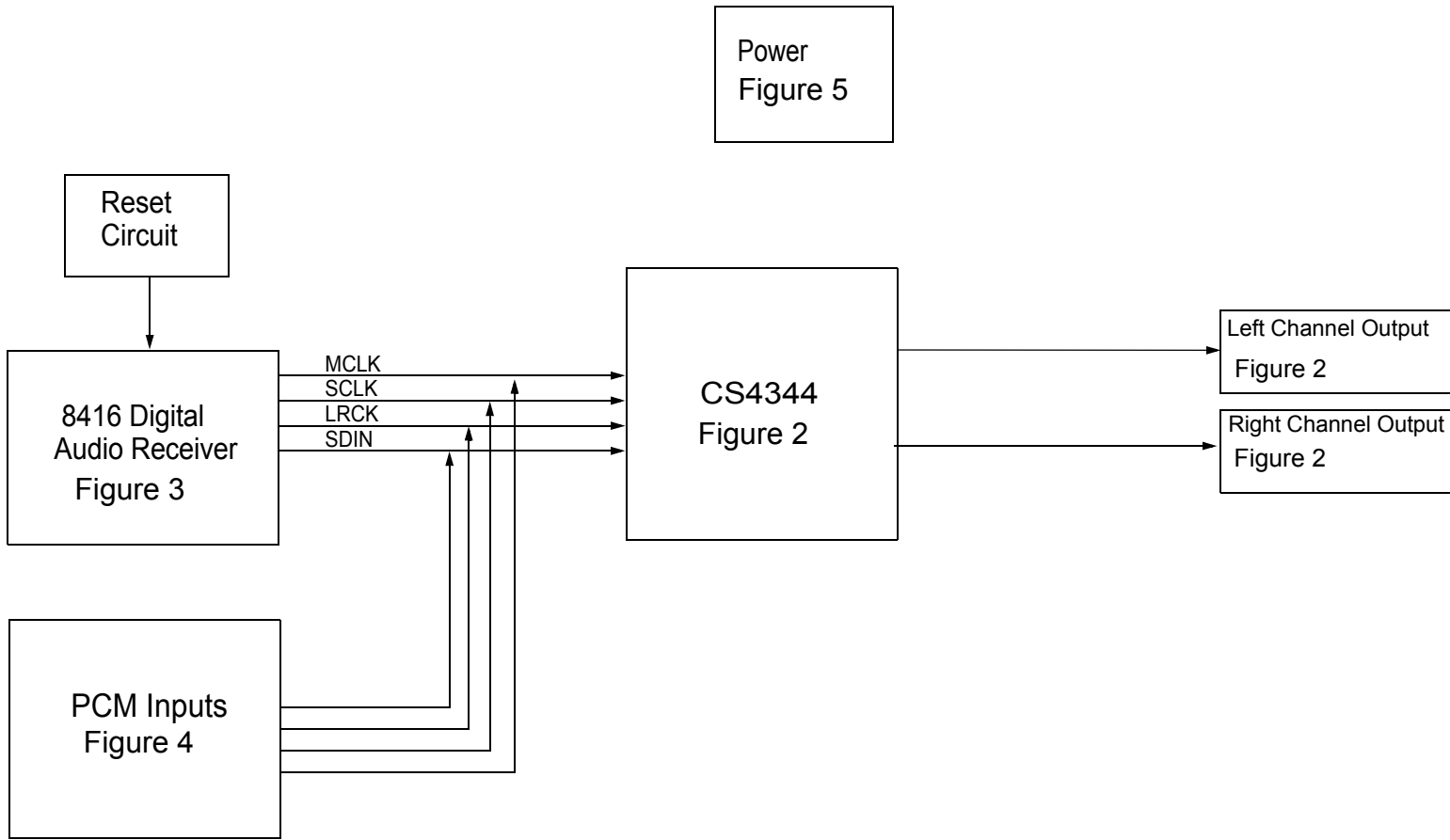
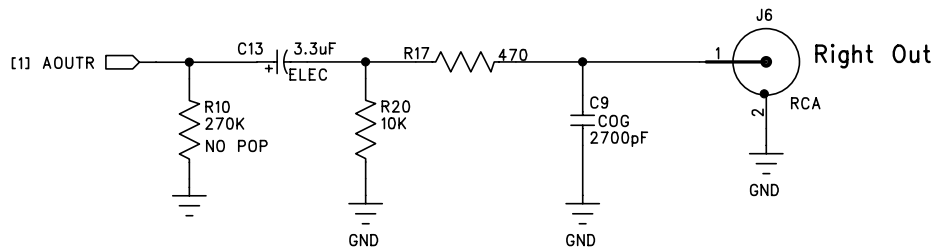
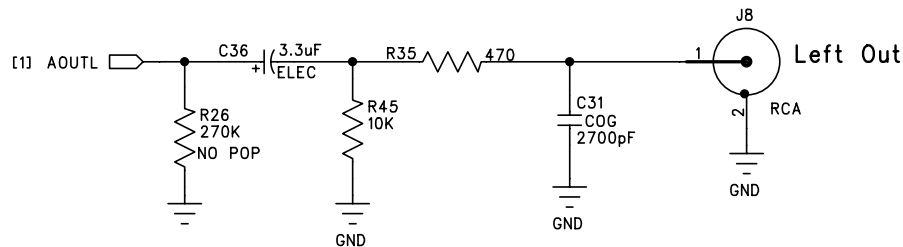
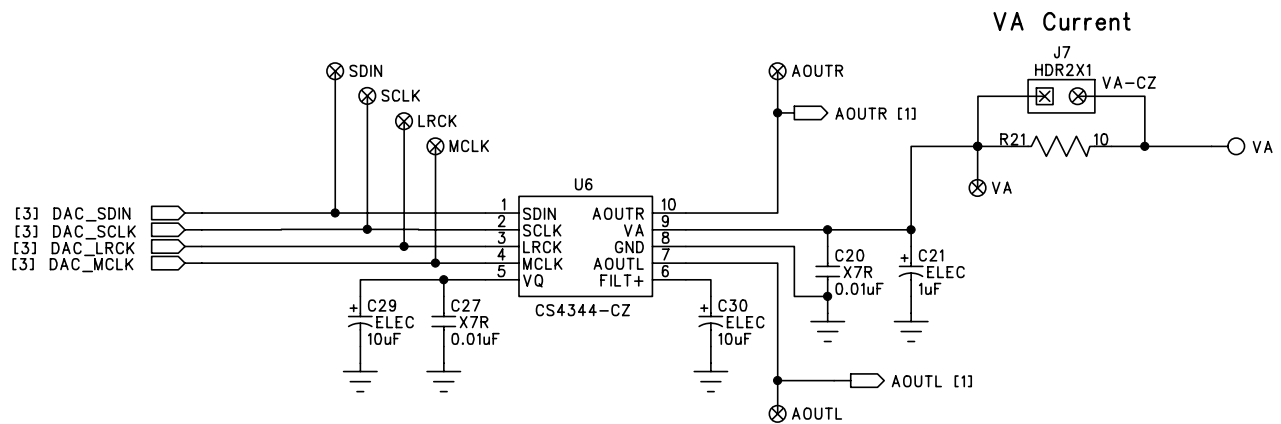


Figure 1. System Block Diagram and Signal Flow



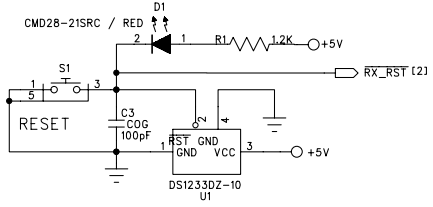
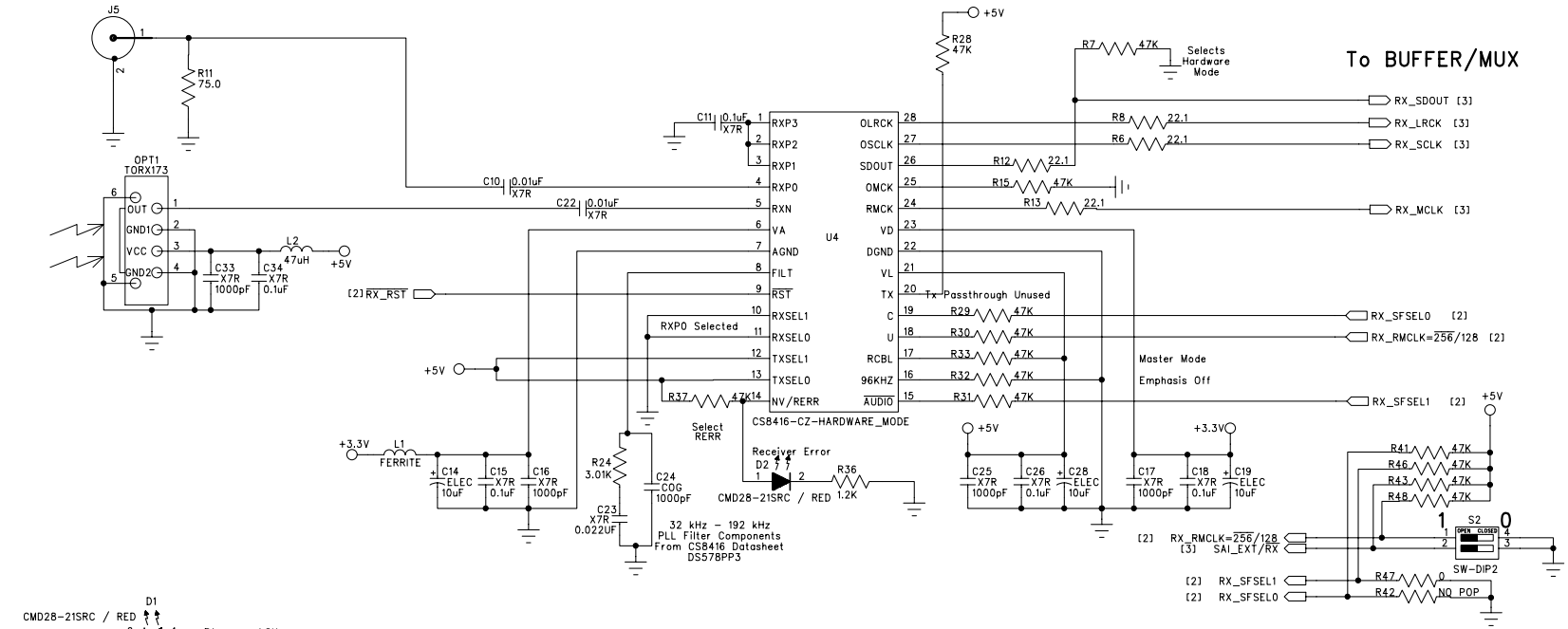


Single pole -3dB at 103kHz.  
 -0.1dB at 16kHz.  
 -0.18dB at 20kHz.

Substitute with 2.2nF  
 Single pole -3dB at 126kHz.  
 -0.1dB at 20kHz.

**Figure 2. CS4344 and outputs**

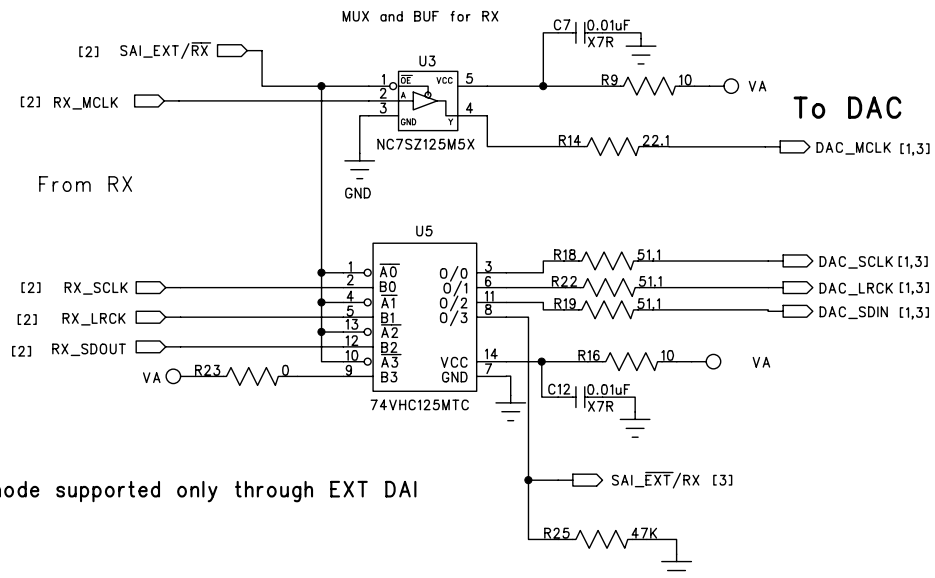
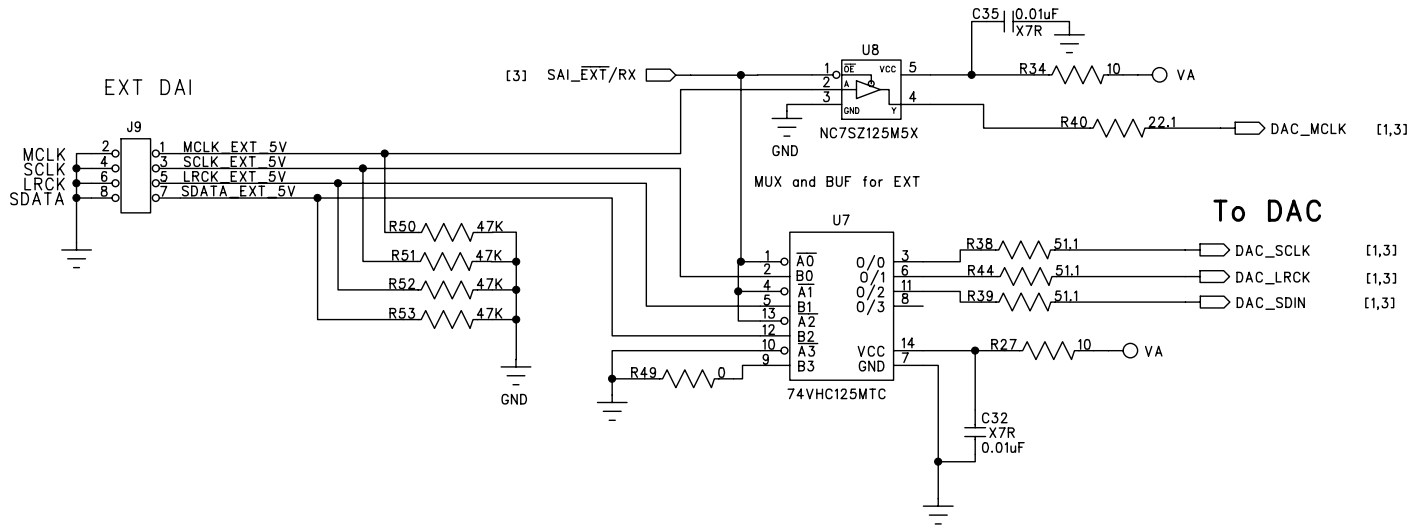




	RX_SFSEL0	RX_SFSEL1	RX_RMCLK	SAI	Notes:
CS4345	0	0	0	0	Left Justified 24bit
CS4344	0	1	0	0	I2S 24bit
CS4346	1	0	0	0	Right Justified 24bit
CS4348	d	d	0	1	Right Justified 16bit Only supported from externally supplied clocks through EXT PCM HDR

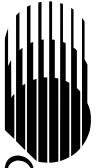
d = don't care  
 0 = 0 Ohm  
 1 = No Pop

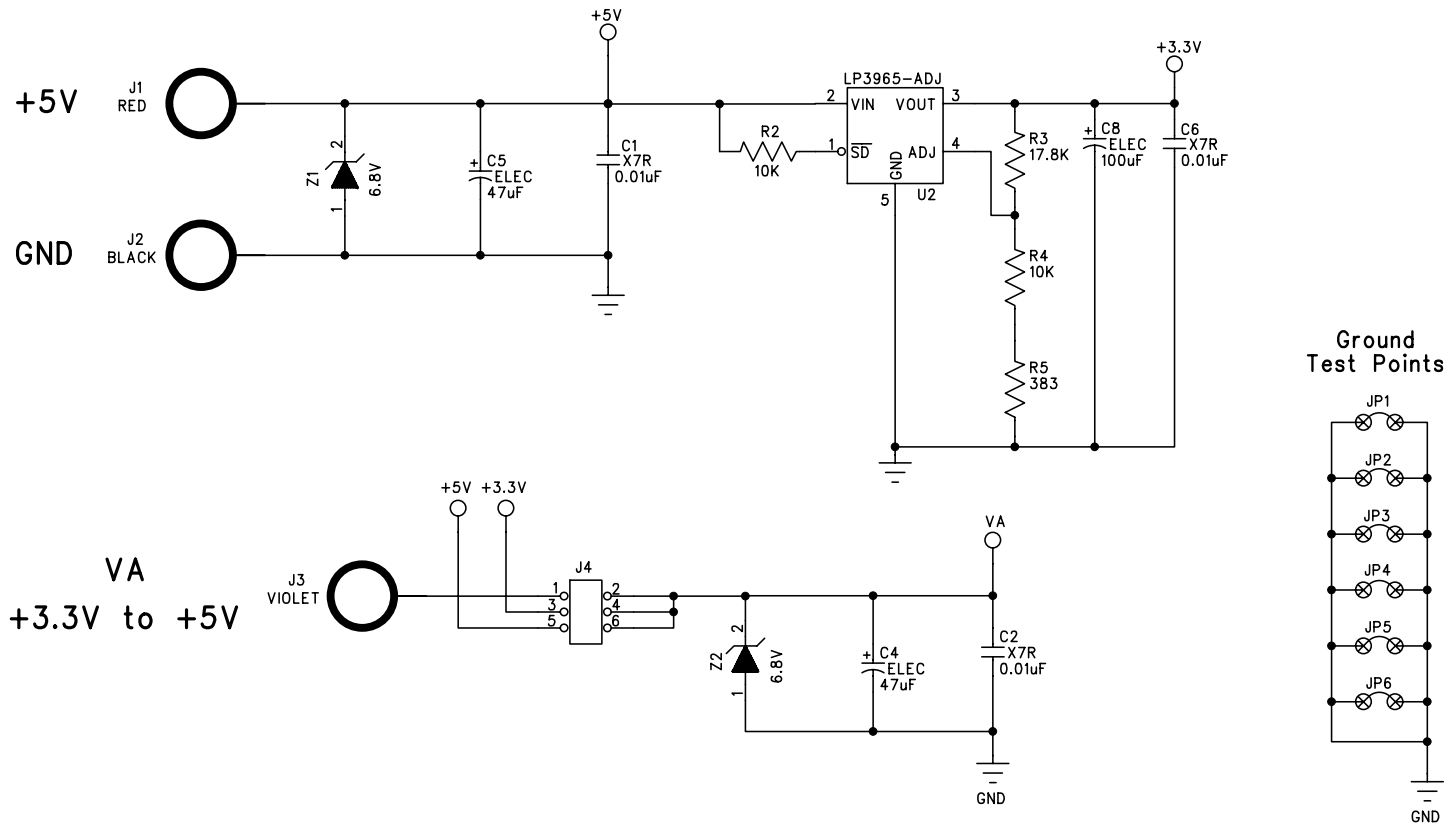
RX\_RMCLK must be 1 for 96k and 192kHz S/PDIF



\*Internal SCLK mode supported only through EXT DAI

Figure 4. PCM Input Header





Ground Test Points

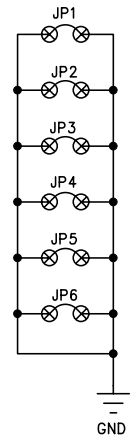
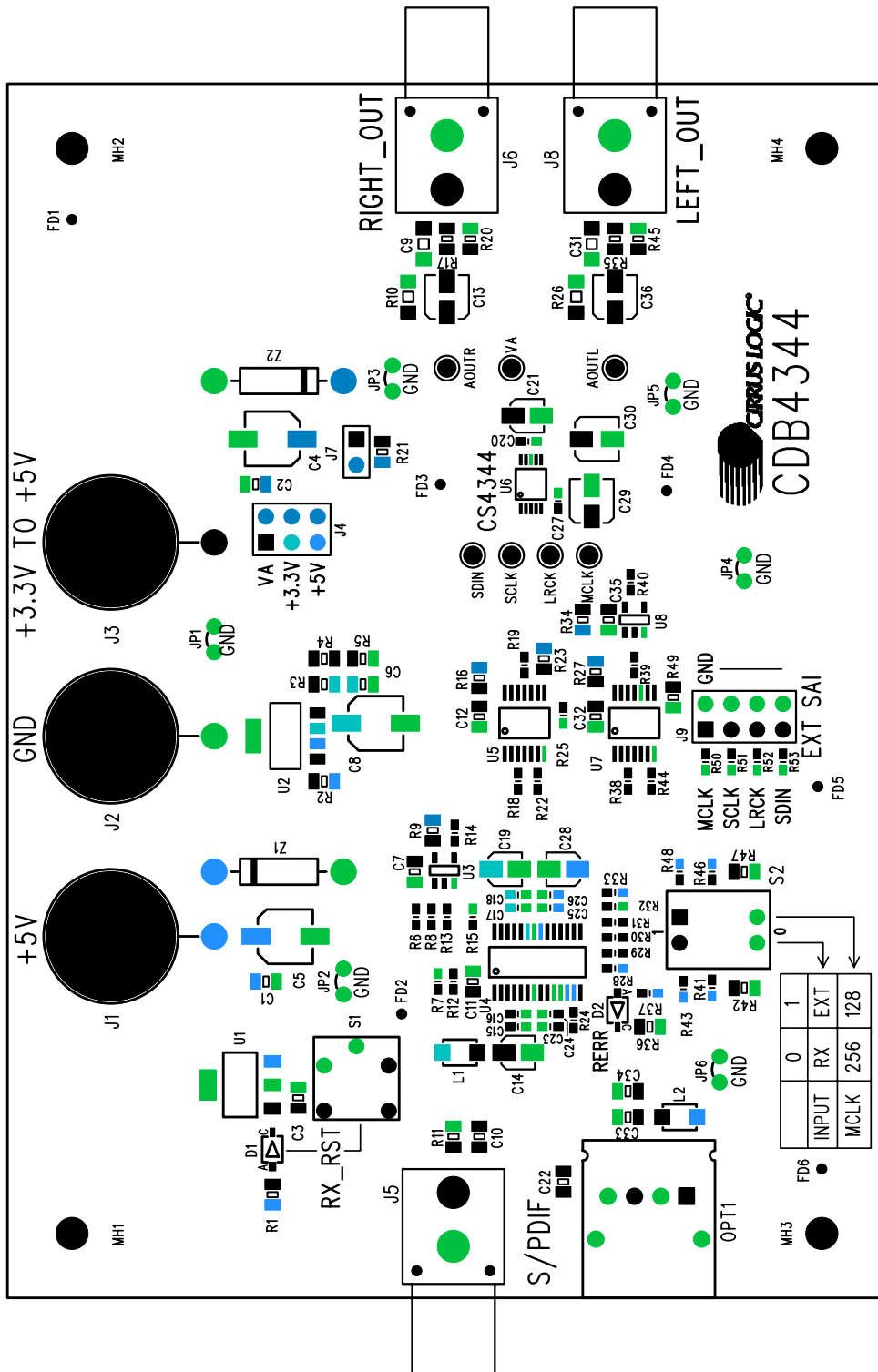


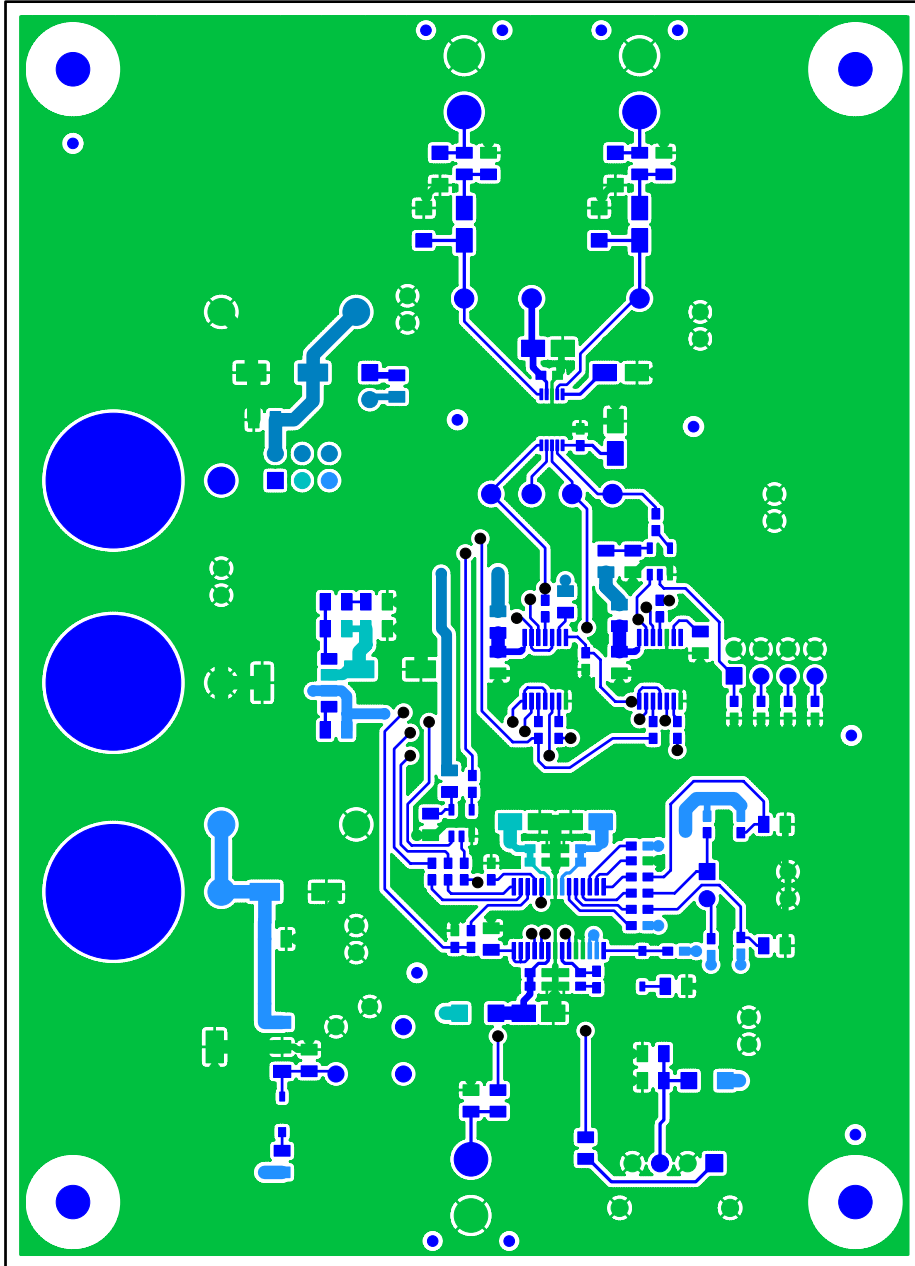
Figure 5. Power Supply Connections





SILKSCREEN TOP

Figure 6. Silkscreen Top

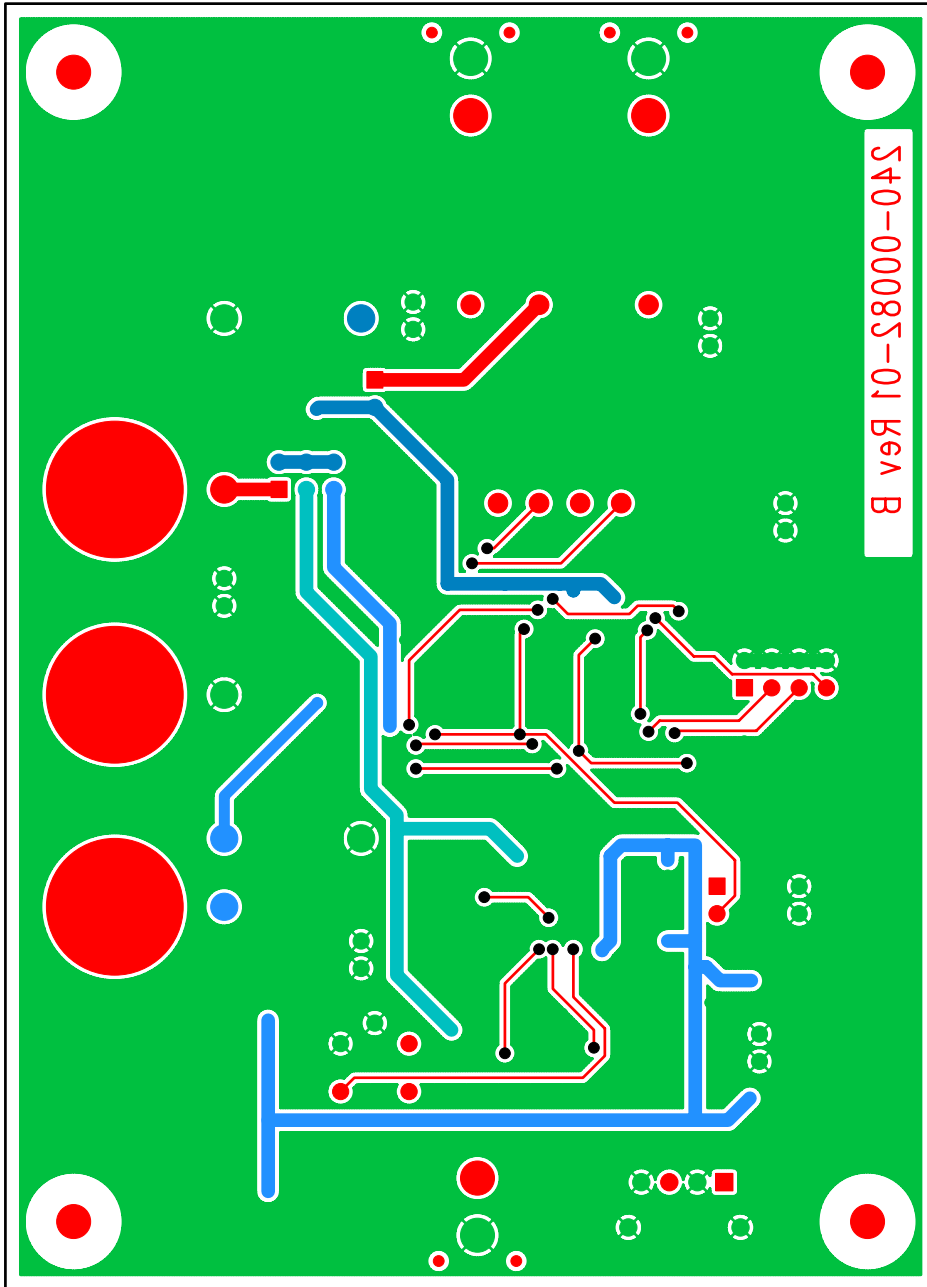


CIRRUS LOGIC CDB4344 PWB 240-00082-01 Rev B

TOP SIDE

Figure 7. Top Side





BOTTOM SIDE

Figure 8. Bottom Side

## REVISION HISTORY

Release	Date	Changes
DB1	DEC 2003	Initial Release
DB2	JUN 2004	Changed C29 in Figure 2 on page 7 from 3.3 to 10 $\mu$ F to improve popguard performance

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### Contacting Cirrus Logic Support

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