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CDB4392

Evaluation Board for CS4392

Features

- Demonstrates recommended layout and grounding arrangements
- CS8414 receives AES/EBU, S/PDIF, & EIAJ-340 compatible digital audio
- Digital and analog patch areas
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

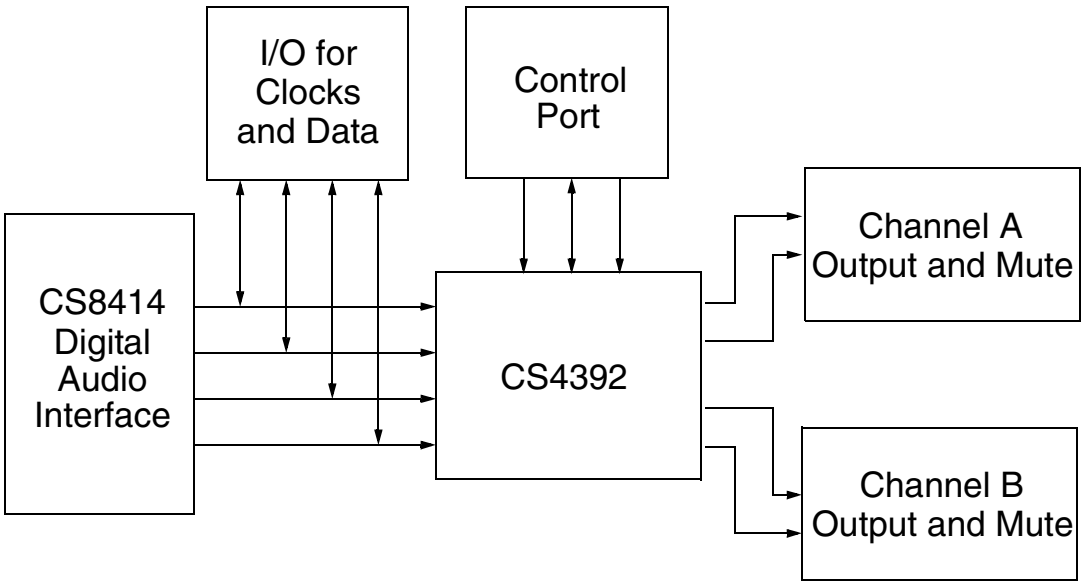
Description

The CDB4392 evaluation board is an excellent means for quickly evaluating the CS4392 24-bit, stereo D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, a PC for controlling the CS4392 (for control port mode only) and a power supply. Analog line level outputs are provided via RCA phono jacks.

The CS8414 digital audio receiver I.C. provides the system timing necessary to operate the Digital-to-Analog converter and will accept AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB4392 Evaluation Board



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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Contacting Cirrus Logic Support

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http://www.cirrus.com/corporate/contacts/sales.cfm

1. CDB4392 SYSTEM OVERVIEW

The CDB4392 evaluation board is an excellent means of quickly evaluating the CS4392. The CS8414 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply clocks and data through a 10-pin header for system development.

The CDB4392 schematic has been partitioned into 9 schematics shown in Figures 2 through 10. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

2. CS4392 DIGITAL TO ANALOG CONVERTER

A description of the CS4392 is included in the CS4392 datasheet.

3. CS8414 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8414 Digital Audio Receiver, Figure 5. The outputs of the CS8414 include a serial bit clock, serial data, left-right clock (FSYNC), de-emphasis control and a 256 Fs master clock. The operation of the CS8414 and a discussion of the digital audio interface are included in the CS8414 datasheet.

During normal operation, the CS8414 operates in the Channel Status mode where the LED's display channel status information for the channel selected by the CSLR/FCK jumper. This allows the CS8414 to decode the de-emphasis bit from the digital audio interface for control of the CS4392 de-emphasis filter, when the CS4392 is in stand-alone mode.

When the Error Information Switch is activated, the CS8414 operates in the Error and Frequency information mode. The information displayed by the LED's can be decoded by consulting the CS8414 datasheet. It is likely that the de-emphasis control for the CS4392 will be erroneous and produce an incorrect audio output if the Error Information Switch is activated and the CS4392 is in the stand-alone mode with the de-emphasis jumper selected.

Encoded sample frequency information can be displayed provided a proper clock is being applied to the FCK pin of the CS8414. When an LED is lit, this indicates a "1" on the corresponding pin located on the CS8414. When an LED is off, this indicates a "0" on the corresponding pin. Neither the L nor R option of CSLR/FCK should be selected if the FCK pin is being driven by a clock signal.

The evaluation board has been designed such that the input can be either optical or coax, see Figure 6. However, both inputs cannot be driven simultaneously.

4. CS8414 DATA FORMAT

The CS8414 data format can be set with switches M0, M1, M2, and M3, as described in the CS8414 datasheet. The format selected must be compatible with the data format of the CS4392, as shown in the CS4392 datasheet. Please note that the CS8414 does not support all the possible modes of the CS4392 and the Left-Justified Format for the CS8414 and the CS4392 have incompatible serial clocks, see Table 1. The default settings for M0-M3 on the evaluation board are given in Tables 3-4.

CS4392 CP Mode Format	CS4392 SA Mode Format	CS8414 Format
0	0	Unsupported
1	1	2
2	2	5
3	3	Unsupported
4	-	Unsupported
5	-	6

Table 1. CS8414 Supported Formats

5. INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the 10-pin header, J9. This header allows the evaluation board to accept externally generated clocks and data. The schematic for the clock/data I/O is shown in Figure 8. The 74HC243 transceiver functions as an I/O buffer where HRD1 through HRD6 determine if the transceiver operates as a transmitter or receiver. A transmit function is implemented with all jumpers, HRD1 through HDR6 in the 8414 position. LRCK, SDATA, and SCLK from the CS8414 will be outputs on J9. The transceiver operates as a receiver with HRD1 through HDR6 in the EXT_CLK position. MCLK, LRCK, SDATA and SCLK on J9 become inputs.

6. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by five binding posts (GND, +5V, VL, +12V and -12V), see Figure 10. The +5V input supplies power to the +5 volt digital circuitry (VA+5, VD+5, VDPC+5) and to VA on the CS4392, while the VL input supplies power to the Voltage Level Converters and the CS4392 VL pin. +12V and -12V supply power to the op-amp and can be +/-5 to +/-12 volts.

WARNING: Refer to the CS4392 datasheet for maximum allowable voltages levels. Operation outside of this range can cause permanent damage to the device.

7. GROUNDING AND POWER SUPPLY DECOUPLING

The CS4392 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 10 details the power distribution used on this board. The decoupling capacitors are located as close to the CS4392 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

8. CONTROL PORT SOFTWARE

The CDB4392 is shipped with Windows based software for interfacing with the CS4392 control port via the DB25 connector, P1. The software can be used to communicate with the CS4392 in either SPI® or Two Wire mode; however, in SPI mode the CS4392 registers are write-only.

Note: The Two Wire control port mode is compatible with the I^2C® protocol.

Further documentation for the software is available on the distribution diskette. The documentation is available in the plain text format file, README.TXT.

9. DSD OPERATION

The CDB4392 supports Direct Stream Digital (DSD) operation through the header for external clocks and data, J9. The CS4392 must be placed into the DSD mode and the jumpers HDR1 through HDR6 must be placed into the external clock positions.

10. ANALOG OUTPUT FILTER

The analog output filter on the CDB4392 has been designed to add flexibility when evaluating the CS4392. The output filter was designed in an optional two stage format, with the first optional stage being an instrumentation amplifier design and the second is a 2-pole butterworth filter.

The 2-pole filter is designed to have the in-band impedance matched between the positive and negative legs. It also provides a balanced to single ended conversion for standard un-balanced outputs.

The instrumentation amplifier is optionally inserted by changing the FILT jumpers (HDR13 and HDR15 for channel A, left, and HDR16 and HDR17 for channel B, right) to position 2. This instrumentation amplifier incorporates a 3x gain (+9.5dB) which effectively lowers the noise contribution of the 2-pole filter which improves the overall dynamic range of the system.

Resistors R16 and R21 can be adjusted to change the gain of the Instrumentation amp, and R2(R23) must equal R3(R22). The gain of this stage is determined from the following equation where R= R16(R21) and R_2= R2(R23)=R3(R22):

$$1 + \frac{2(R)}{R_2}$$

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5V	Input	+ 5 Volt power
+3/+5V **	Input	+ 5 Volt **ONLY** power for the CS4392
V_L	Input	+ 1.8 to +5.5 digital interface voltage (Note that V_L should not exceed the voltage applied to the+3/+5V terminal)
V_{EE}	Input	-12 to -5V negative supply for the op-amp
V_{CC}	Input	+5 to +12V positive supply for the op-amp
GND	Input	Ground connection from power supply
Coax Input	Input	Digital audio interface input via coax
Optical Input	Input	Digital audio interface input via optical
J9	Input/Output	I/O for master, serial, left/right clocks and serial data
Parallel Port	Input/Output	Parallel connection to PC for SPI / Two Wire control port signals
HDR9	Input/Output	I/O for SPI / Two Wire control port signals
AOUTA	Output	Channel A line level analog output
AOUTB	Output	Channel B line level analog output

Table 2. System Connections

JUMPER / SWITCH	PURPOSE	POSITION	FUNCTION SELECTED
SW1 - M0	CS8414 mode selection	*LO	See CS8414 datasheet for details
SW1 - M1	CS8414 mode selection	*HI	See CS8414 datasheet for details
SW1 - M2	CS8414 mode selection	*LO	See CS8414 datasheet for details
SW1 - M3	CS8414 mode selection	*LO	See CS8414 datasheet for details
SW1 - CSLR/FCK	Selects channel for CS8414 channel status information	*LO	See CS8414 datasheet for details
HDR8	External mute for AOUTA	*ON OFF	Mute Enabled Mute Disabled
HDR7	External mute for AOUTB	*ON OFF	Mute Enabled Mute Disabled
ENCTRL	Enables / Disables parallel port	ENABLE *DISABLE	Invalid for Stand-Alone Mode Disables parallel port
M0/AD0/CS	CS4392 Mode Selection	*HI LO	See CS4392 datasheet for details
M1/SDA/CDIN	CS4392 Mode Selection	HI *LO	See CS4392 datasheet for details
M2/SCL/CCLK	CS4392 Mode Selection	GND HI *DEM	See CS4392 datasheet for details Allows the CS8414 to control de-emphasis
M3	CS4392 Mode Selection	HI *LO	See CS4392 datasheet for details
HDR1 to HDR6	Selects source of clocks and audio data	*8414 EXT	Selects CS8414 as source Digital I/O header becomes source
HDR13,15 and HDR16,17	Selects whether the optional instrumentation amplifier is used or bypassed	1 *2	Bypassed Active

Table 3. CDB4392 Jumper and Switch settings - STAND-ALONE MODE

*Settings for Stand-Alone mode

Notes: The CDB4392 evaluation board is shipped from the factory configured for Control Port mode.

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
SW1 - M0	CS8414 mode selection	*LO	See CS8414 datasheet for details
SW1 - M1	CS8414 mode selection	*HI	See CS8414 datasheet for details
SW1 - M2	CS8414 mode selection	*LO	See CS8414 datasheet for details
SW1 - M3	CS8414 mode selection	*LO	See CS8414 datasheet for details
SW1 - CSLR/FCK	Selects channel for CS8414 channel status information	*LO	See CS8414 datasheet for details
HDR8	External mute for AOUTA	*ON OFF	Mute Enabled Mute Disabled
HDR7	External mute for AOUTB	*ON OFF	Mute Enabled Mute Disabled
ENCTRL	Enables / Disables parallel port	*ENABLE DISABLE	Enables parallel port Invalid for Control Port mode
M0/**AD0/CS**	AD0/$\overline{CS}$	*HI LO	“Don’t Care” for Control Port mode
M1/**SDA/CDIN**	SDA/CDIN Pull-Up	*HI LO	SDA/CDIN pulled high Invalid for Control Port mode
M2/**SCL/CCLK**	SCL/CCLK Pull-Up	GND *HI DEM	Invalid for Control Port mode SCL/CCLK pulled high Invalid for Control Port mode
M3	Not Functional	HI *LO	Must be low for Control Port mode
HDR1 to HDR6	Selects source of clocks and audio data	*8414 EXT	Selects CS8414 as source Digital I/O header becomes source
HDR13,15 and HDR16,17	Selects whether the optional instrumentation amplifier is used or bypassed	1 *2	Bypassed Active

Table 4. CDB4392 Jumper and Switch settings - CONTOL PORT MODE

*Settings for Control Port mode

Notes: The CDB4392 evaluation board is shipped from the factory configured for Control Port mode.

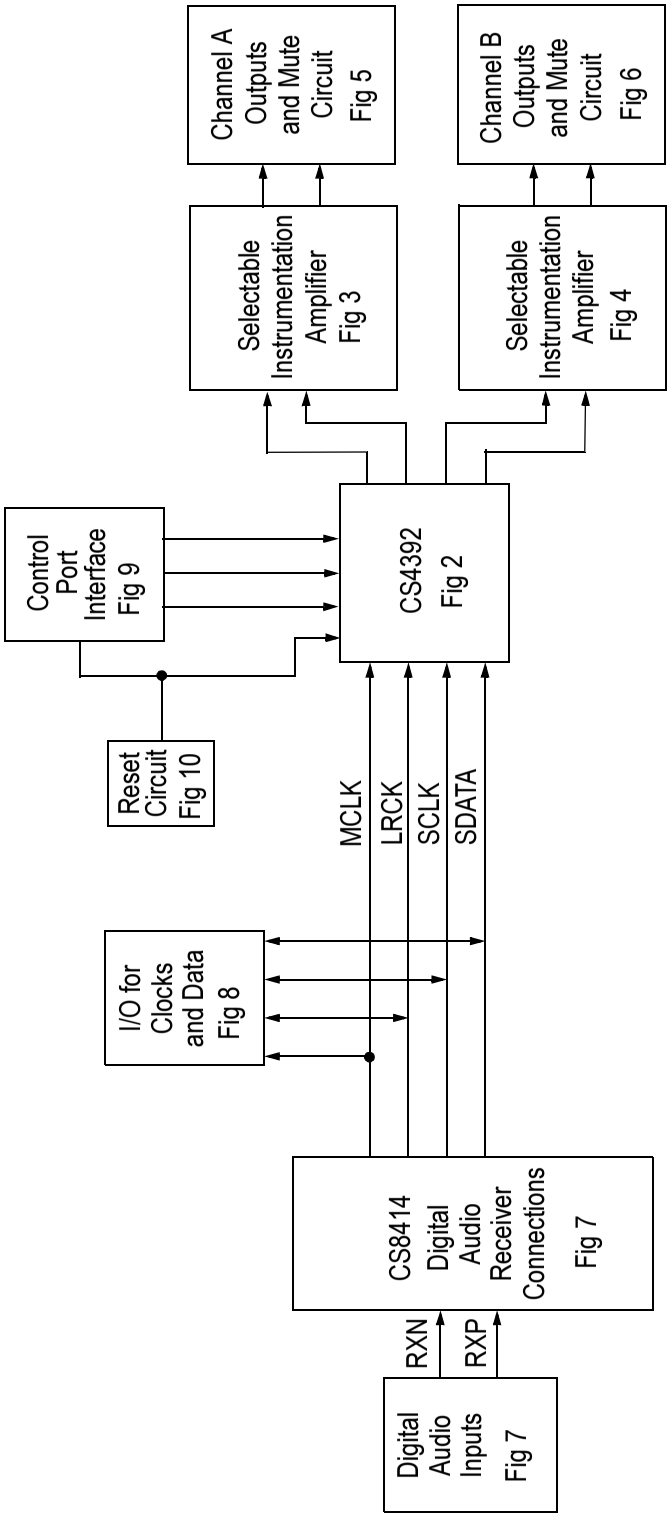

Figure 1. System Block Diagram and Signal Flow

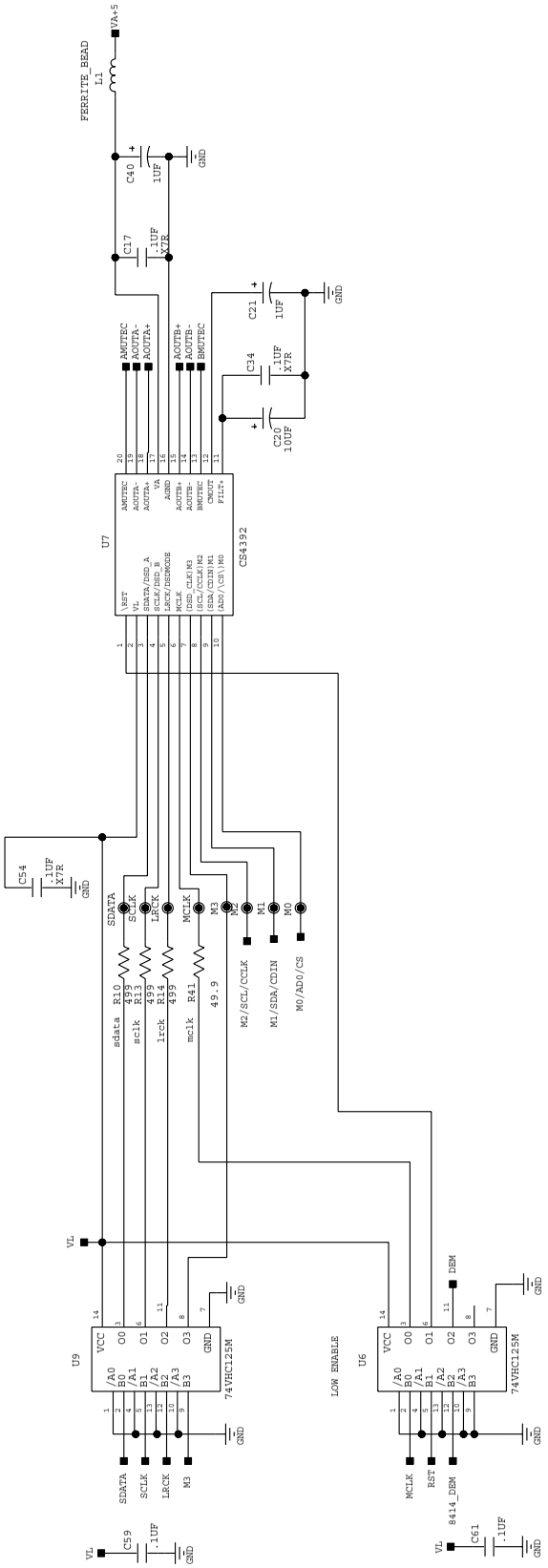

Figure 2. CS4392 and Level Shifters

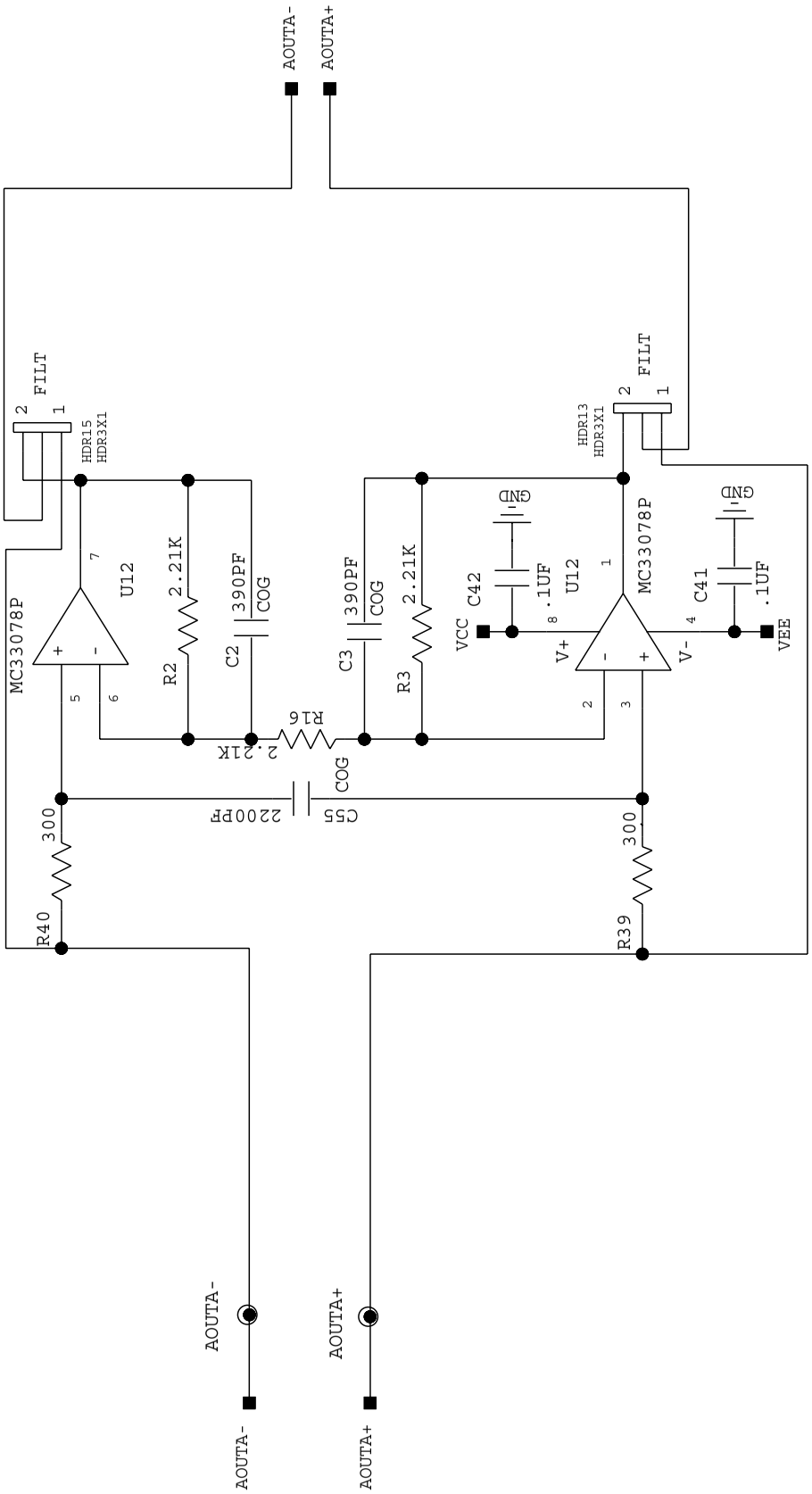

Figure 3. Channel A Selectable Instrumentation Amplifier

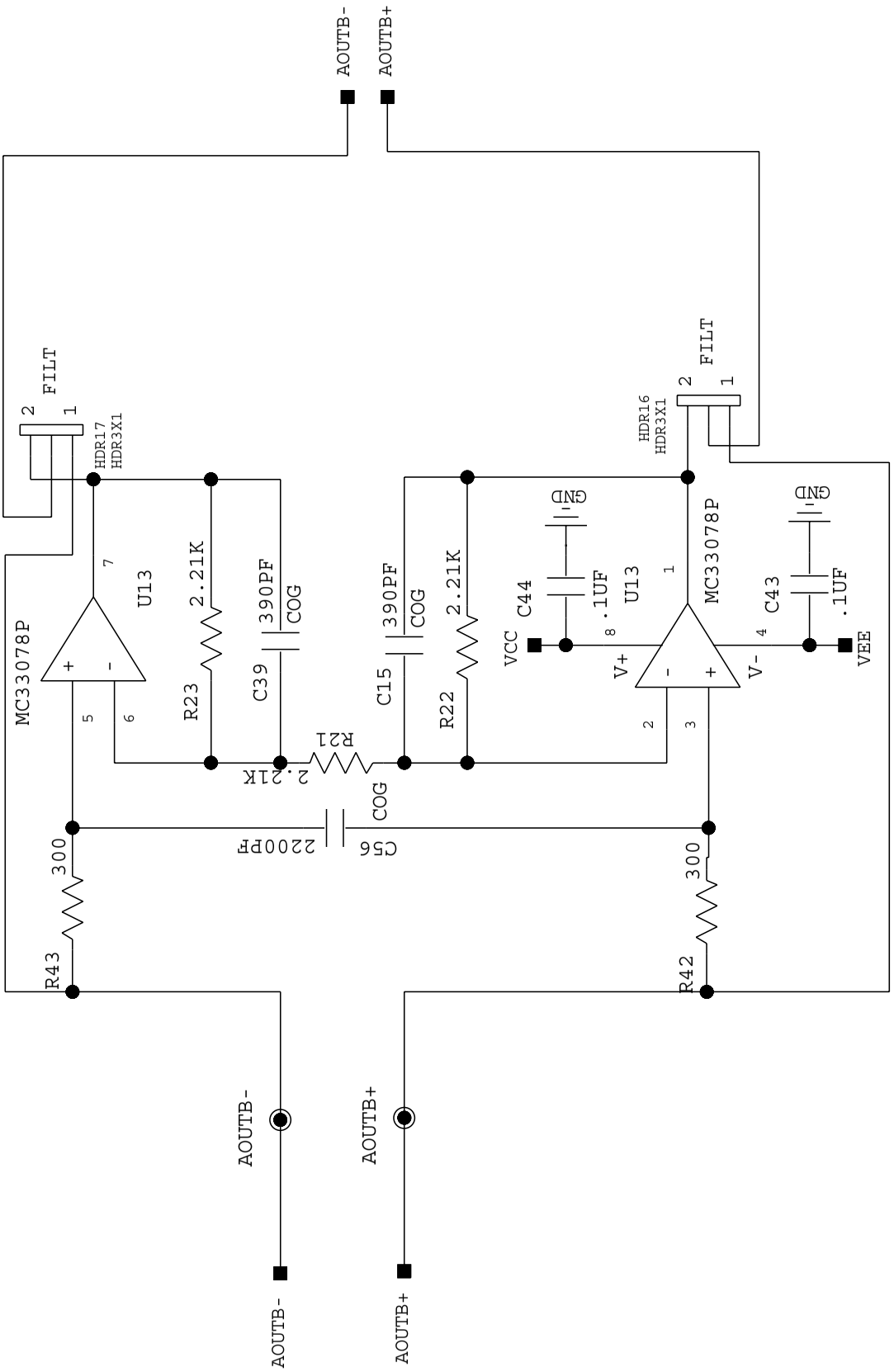

Figure 4. Channel B Selectable Instrumentation Amplifier

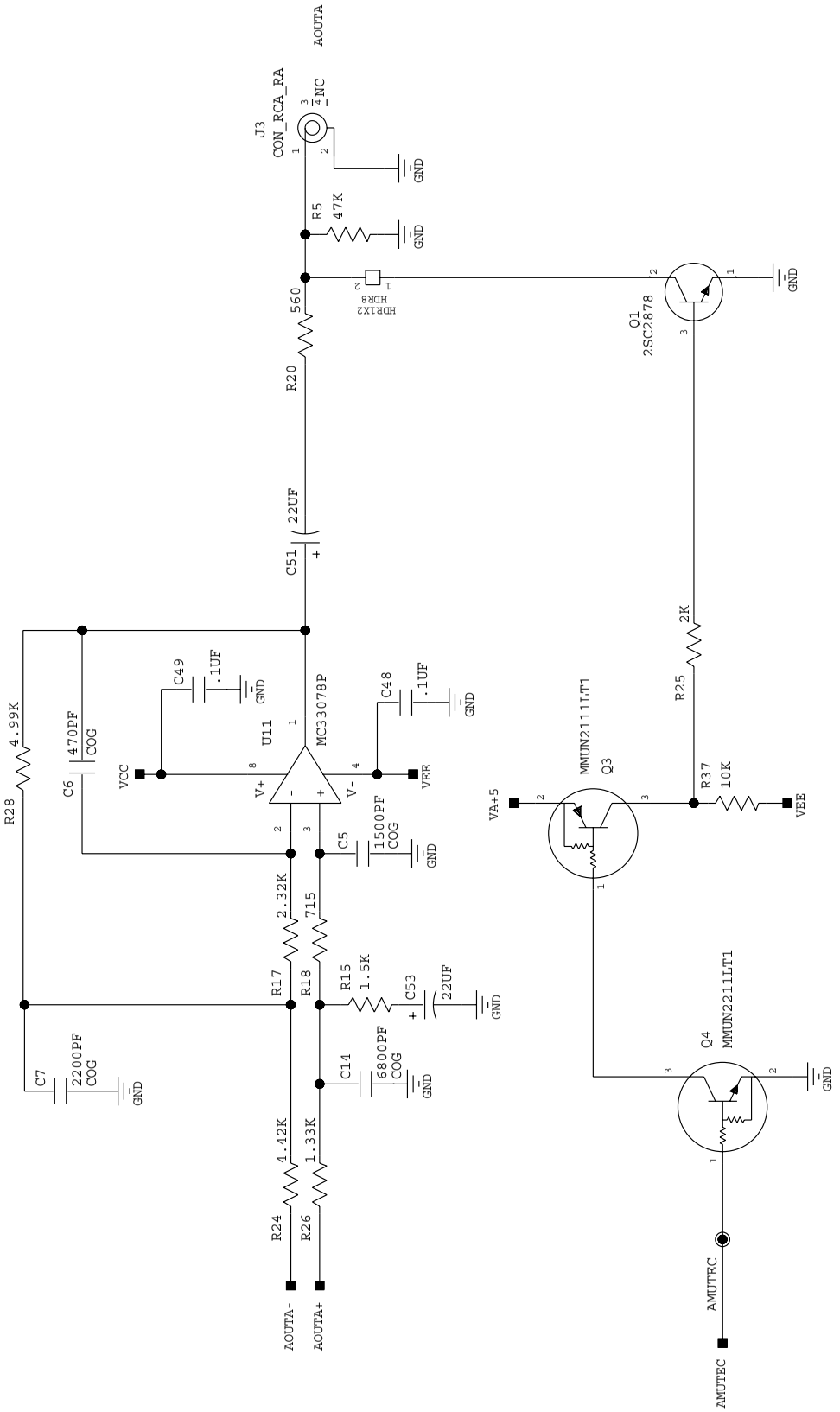

Figure 5. Channel A Audio Output and Mute Circuit

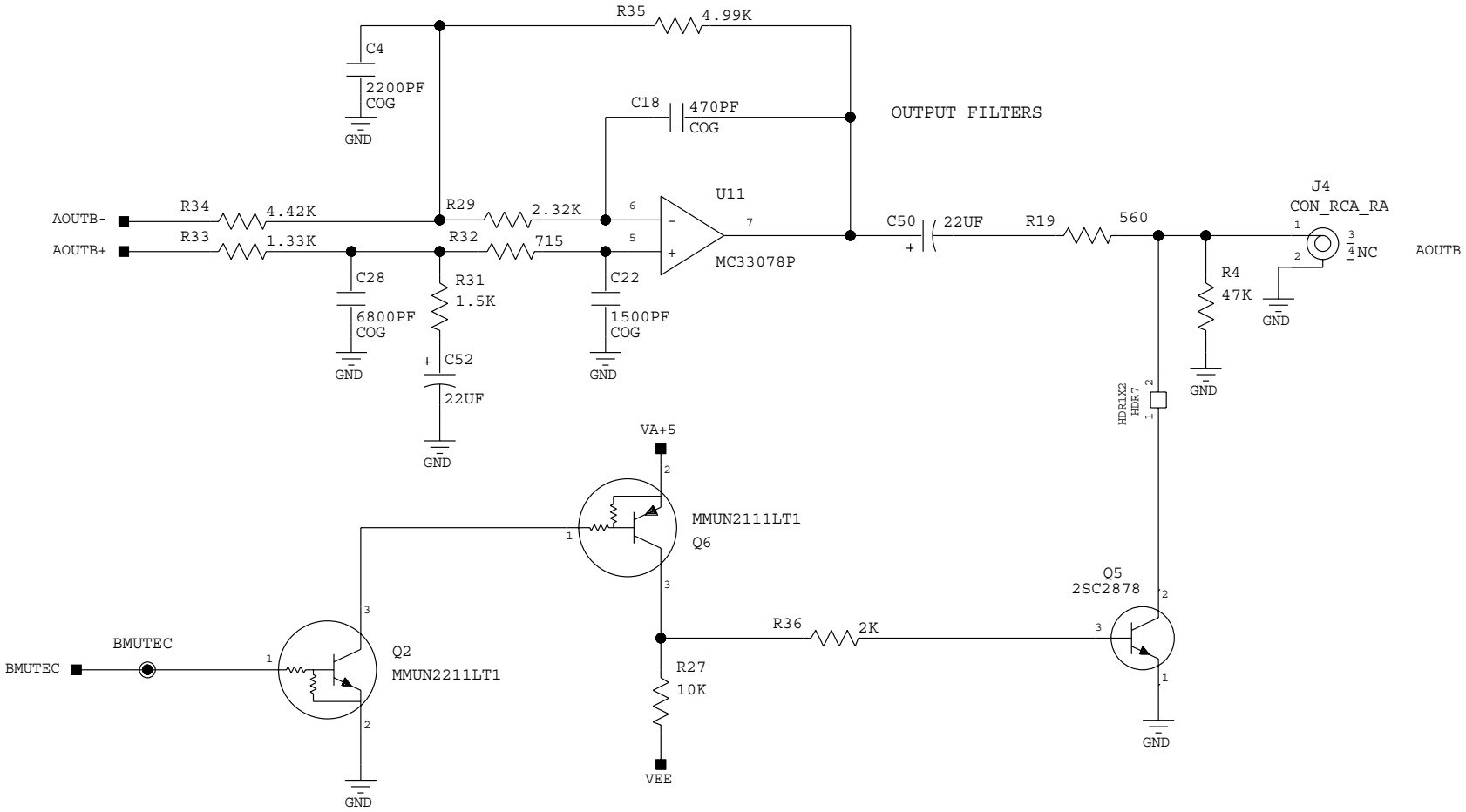

Figure 6. Channel B Audio Output and Mute Circuit

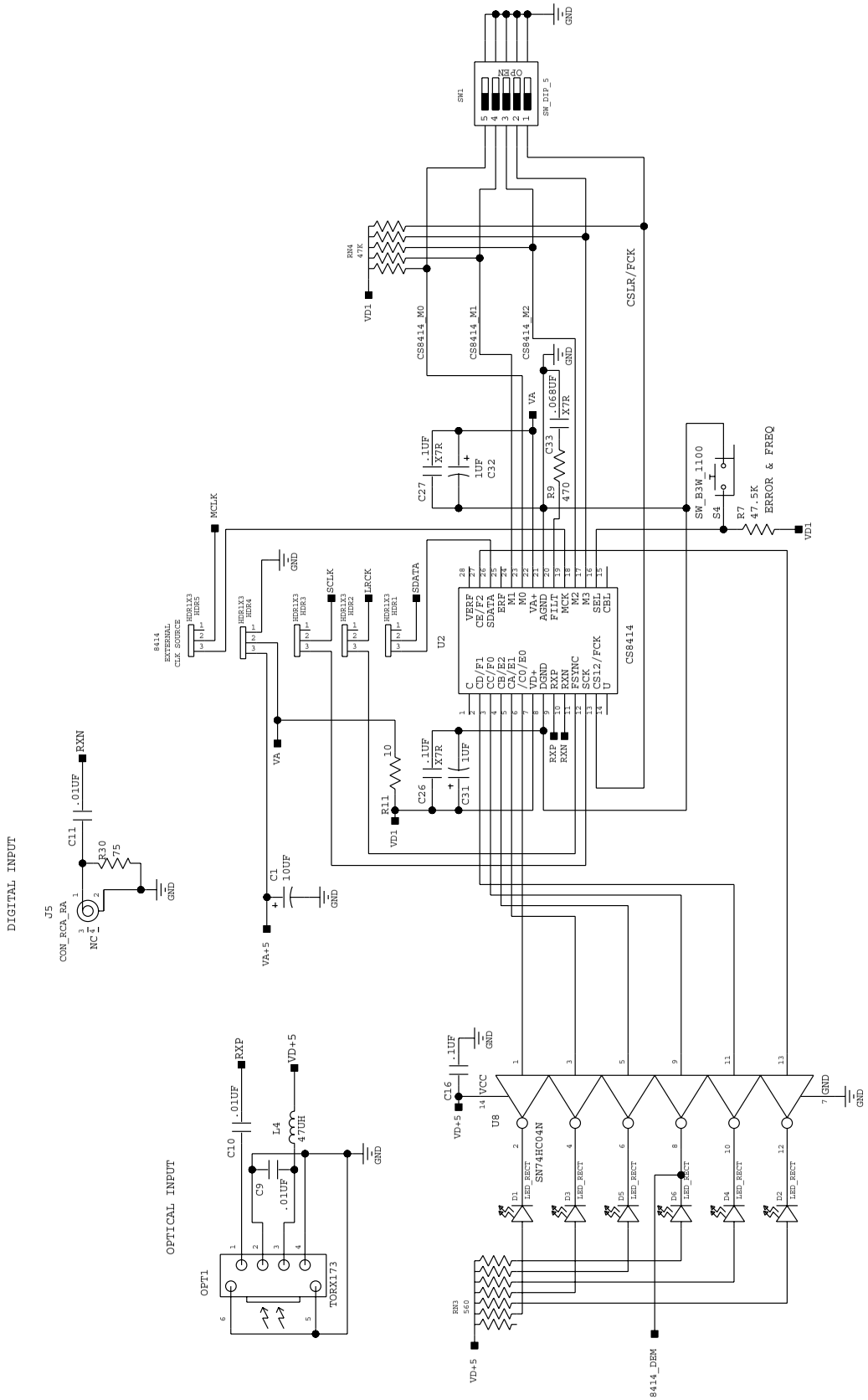

Figure 7. CS8414 Digital Audio Receiver

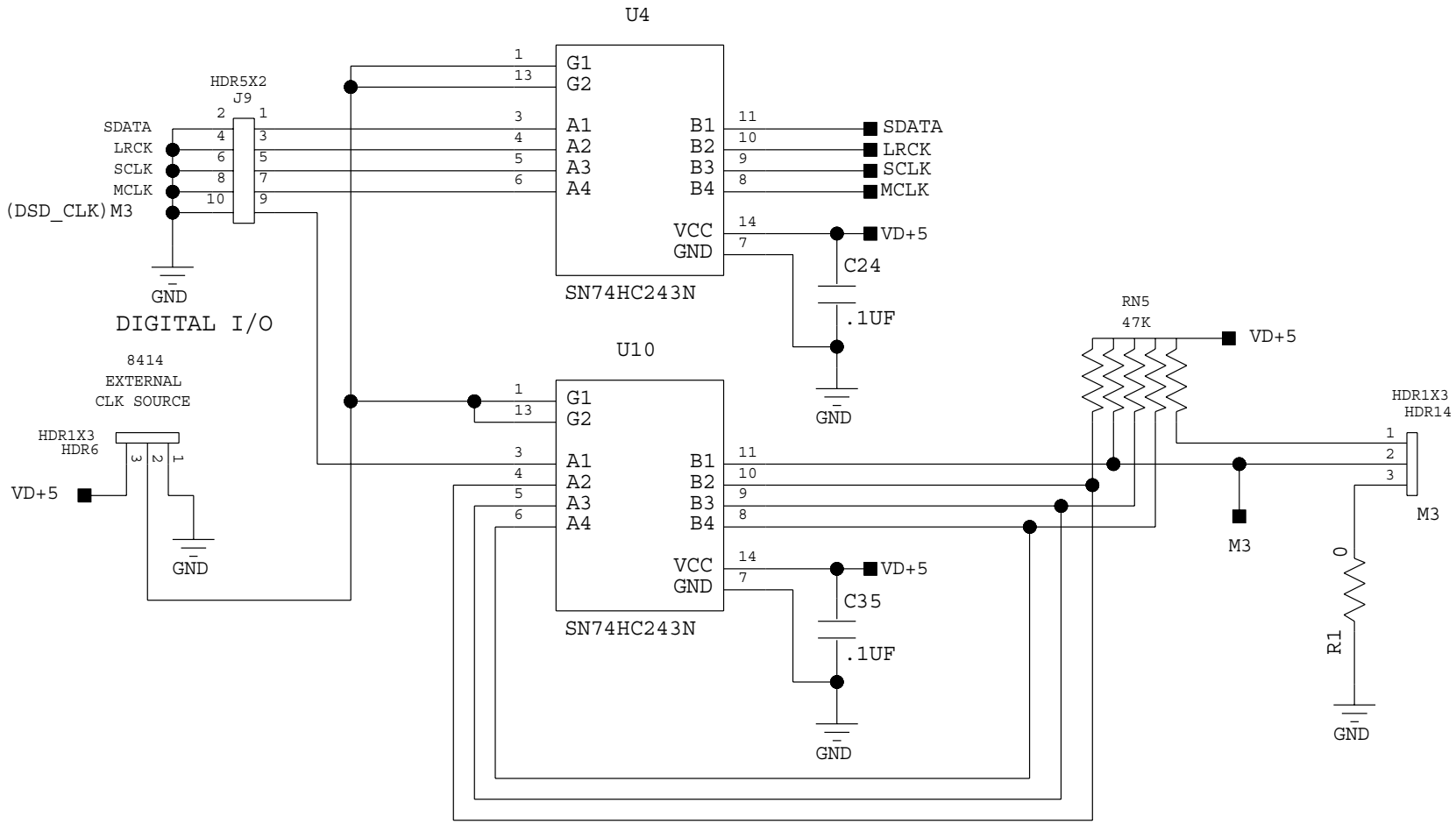

Figure 8. I/O for Clocks and Data

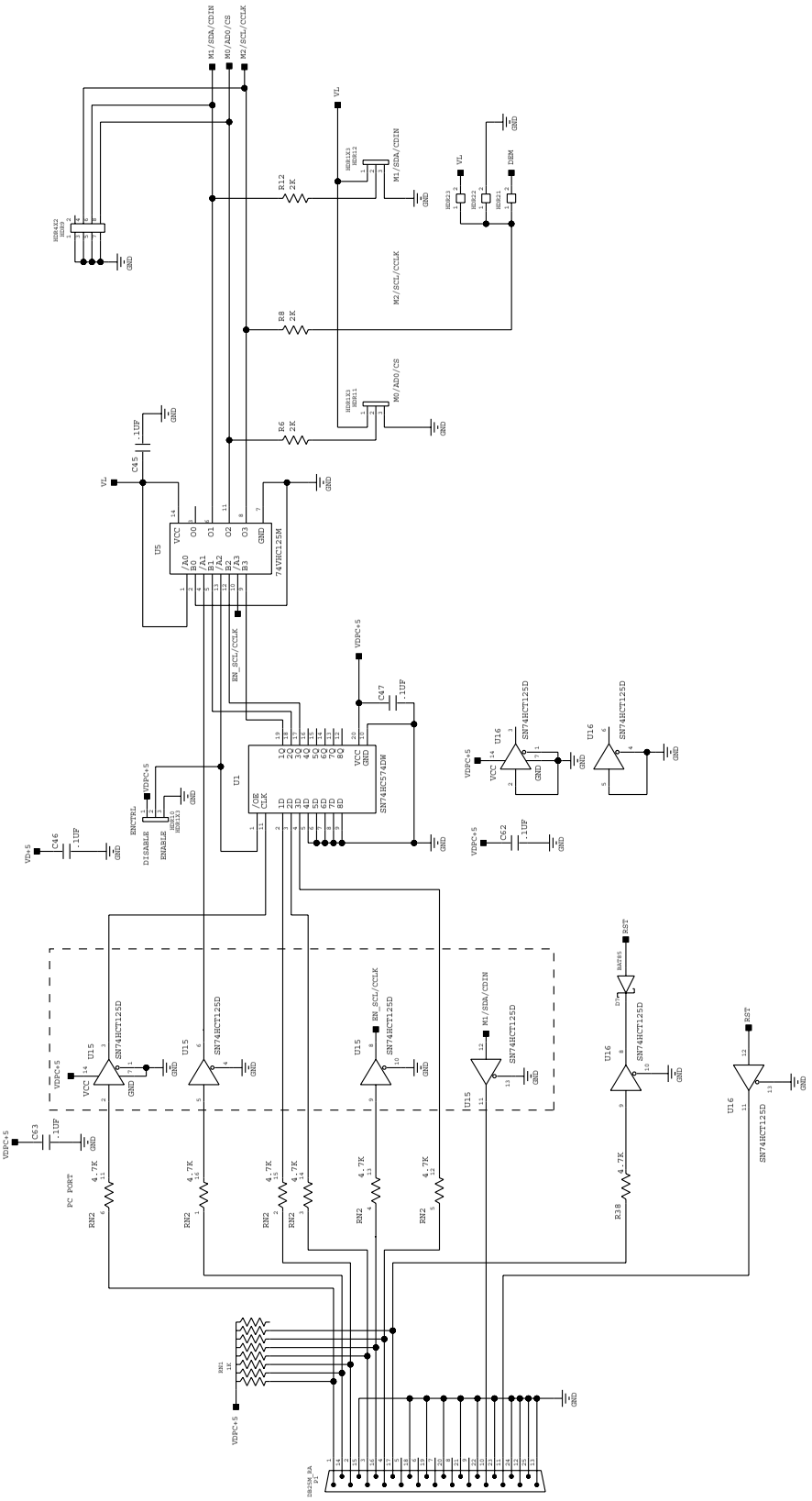

Figure 9. Control Port Interface

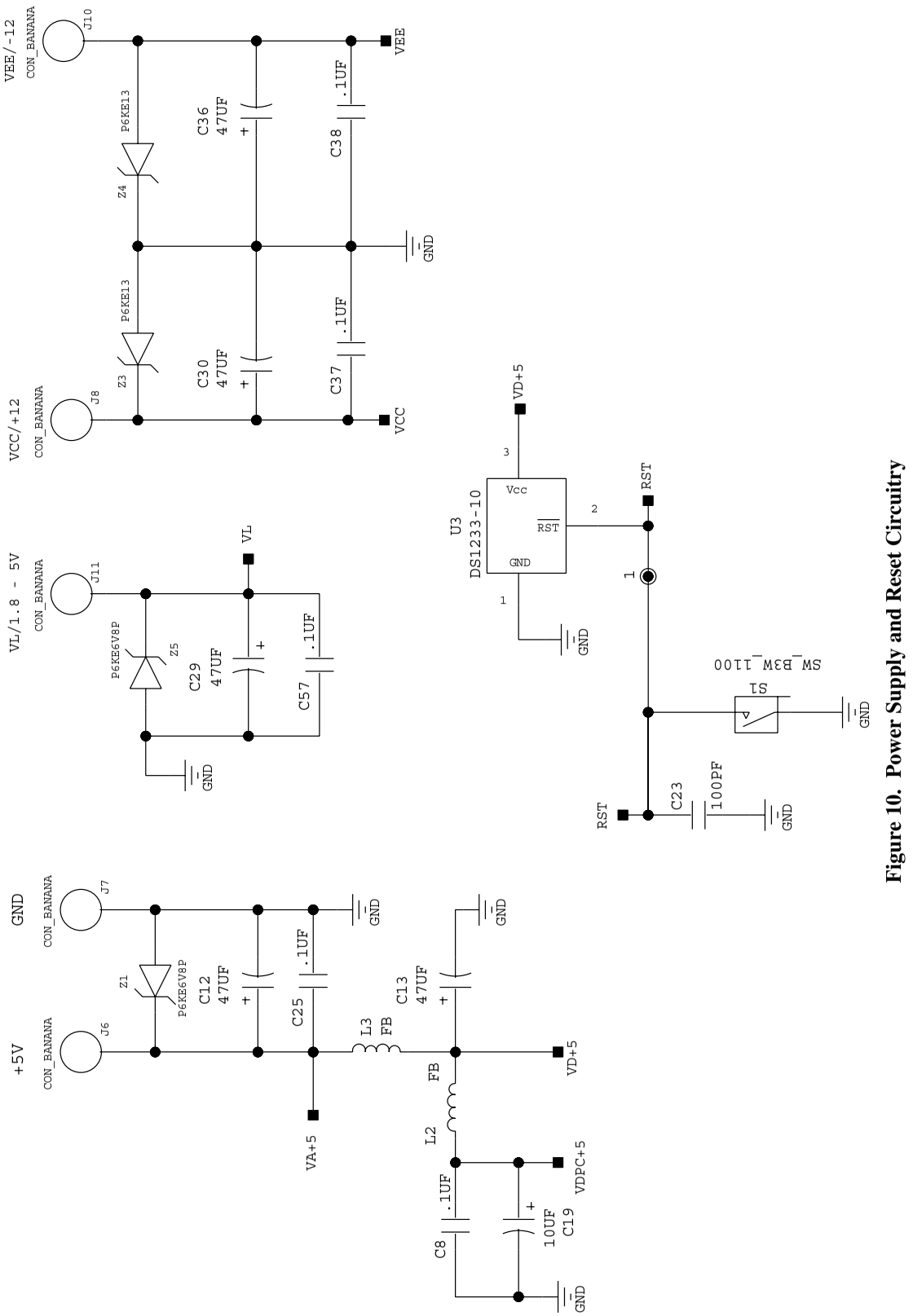

Figure 10. Power Supply and Reset Circuitry

CRYSTAL SEMICONDUCTOR
CS4392 Customer Demonstration Bd
CDB4392A.0

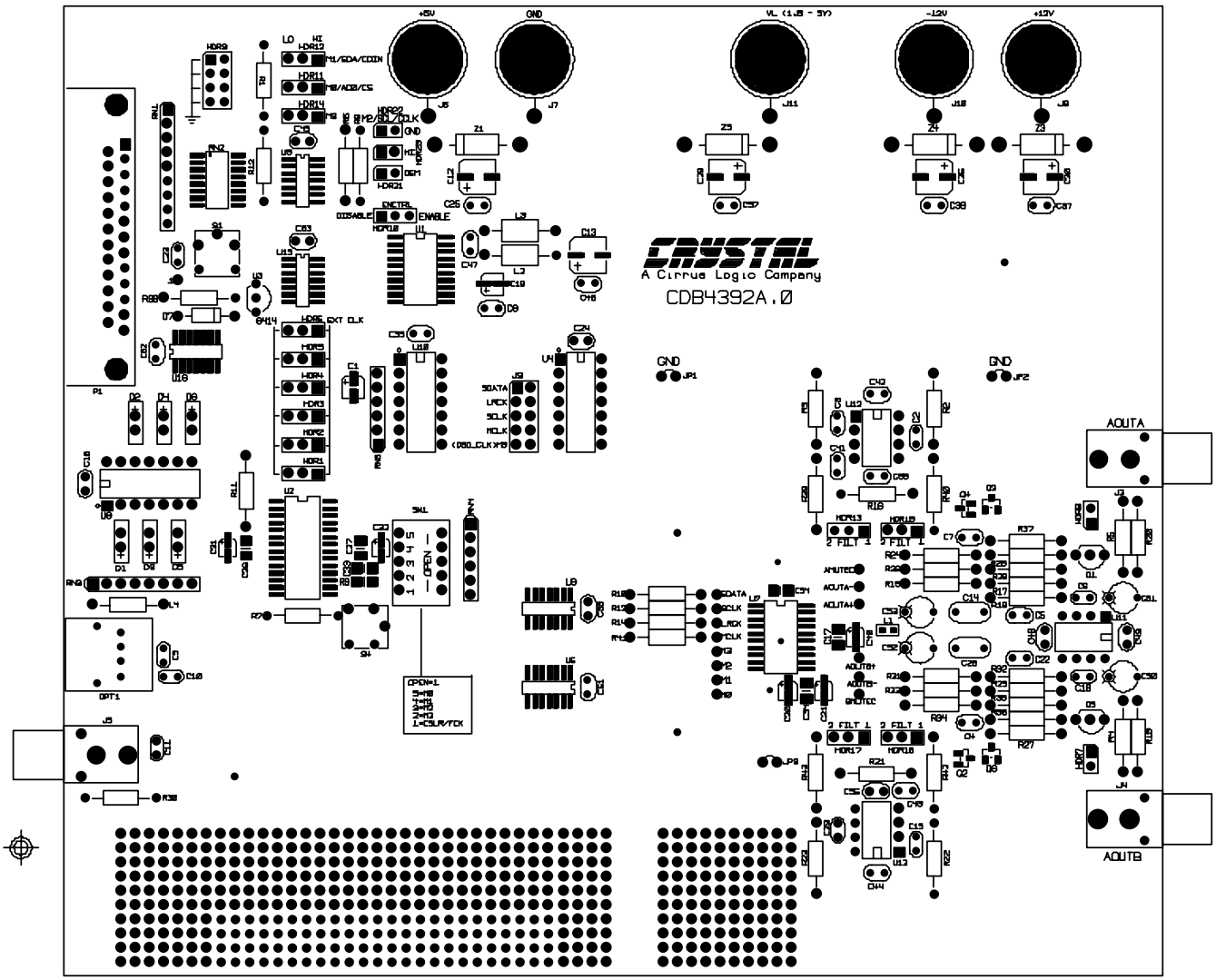

Figure 11. Silkscreen Top

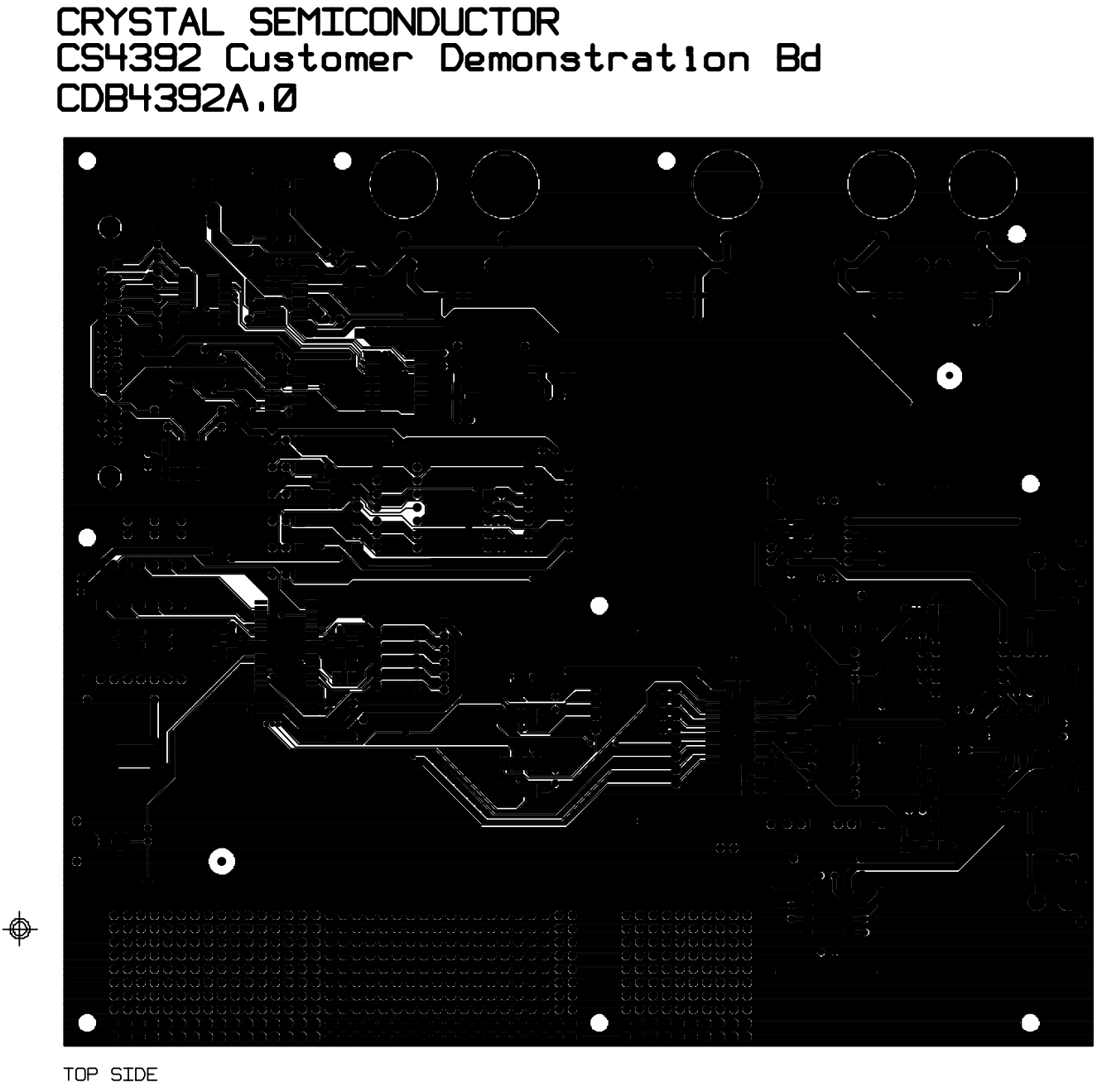

Figure 12. Top Side

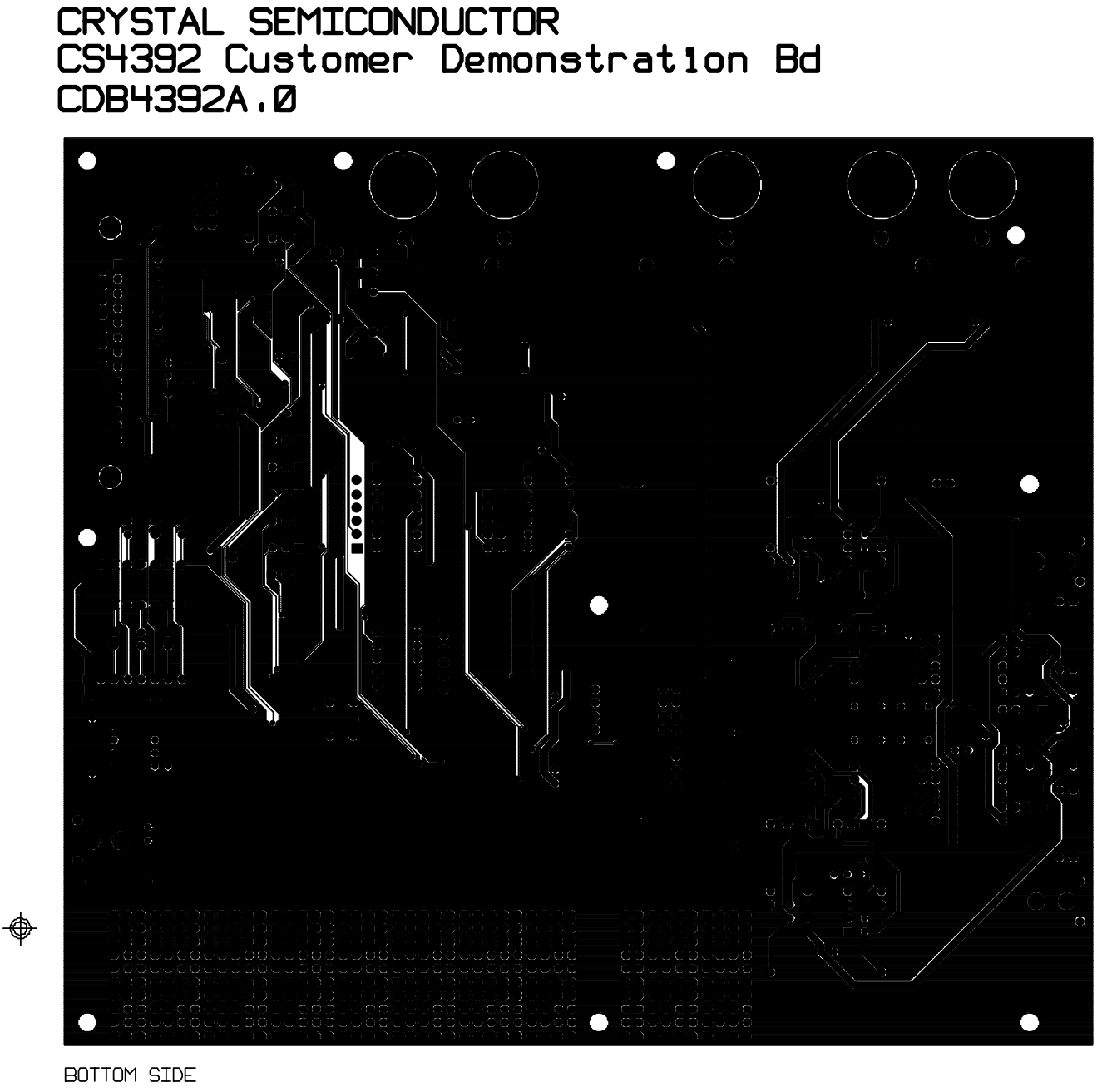

Figure 13. Bottom Side

• Notes •


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