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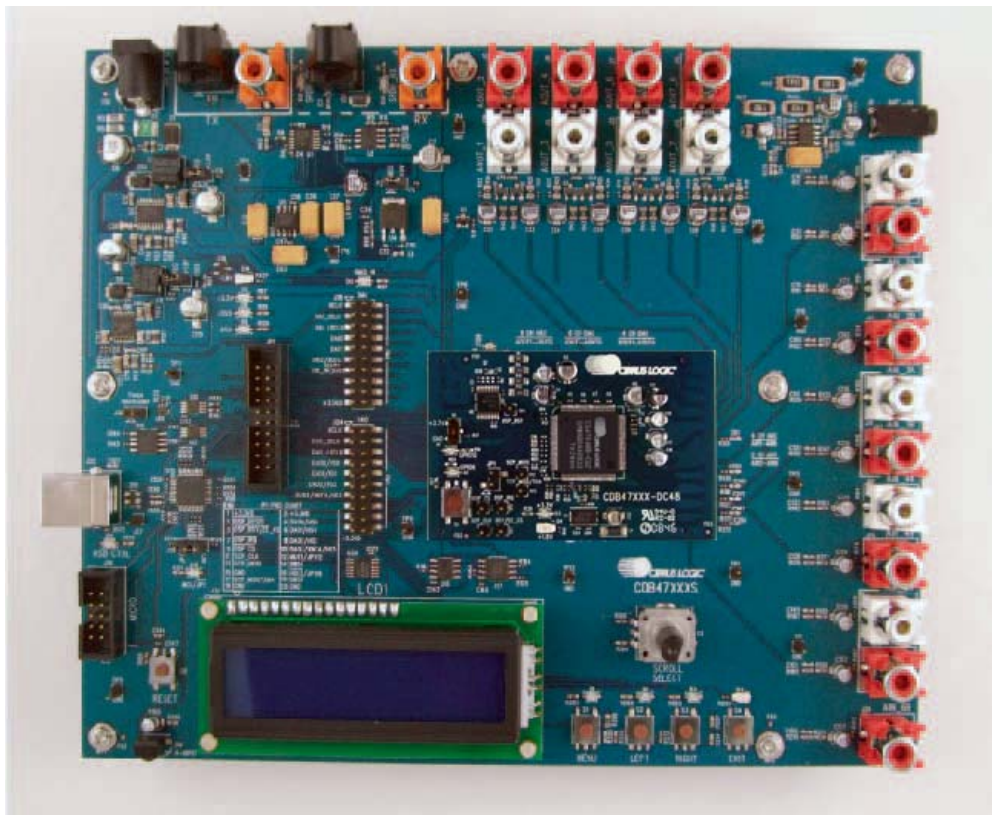
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CDB47xxx
Evaluation Kit

CDB47xxx

User's Manual



Contacting Cirrus Logic Support

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Chapter 1

Kit Contents and Requirements

1.1 CDB47xxx Kit Contents

Each CDB47xxx kit comes with the items listed in [Table 1-1](#).

Table 1-1. CDB47xxx Kit Contents

CRD Kit	Item	Quantity
CDB47xxxS-DC48 CDB47xxxS-DC28 CDB47xxxS-DC24	CDB47xxxS Single-Ended Development Board with integrated MCU & USB interface with daughtercard populated with either the CS47048, CS4028, or CS47024 DSP.	1
CDB47xxxD-DC48 CDB47xxxD-DC28 CDB47xxxD-DC24	CDB47xxxD Differential Development Board with integrated MCU & USB interface with daughtercard populated with either the CS47048, CS4028, or CS47024 DSP.	1
CDB47xxxS-DCxx CDB47xxxD-DCxx	Power Supply: +9V, 2A, 100V - 240V with AC Power Cord	1
CDB47xxxS-DCxx CDB47xxxD-DCxx	USB Cable	1
CDB47xxxS-DCxx CDB47xxxD-DCxx	Document Card explaining how to get the latest board software	1

[Figure 1-1](#) and [Figure 1-2](#) show the kit contents for the CDB47xxxS-DCxx (Single-ended) and CDB47xxxD-DCxx (Differential) development boards respectively.

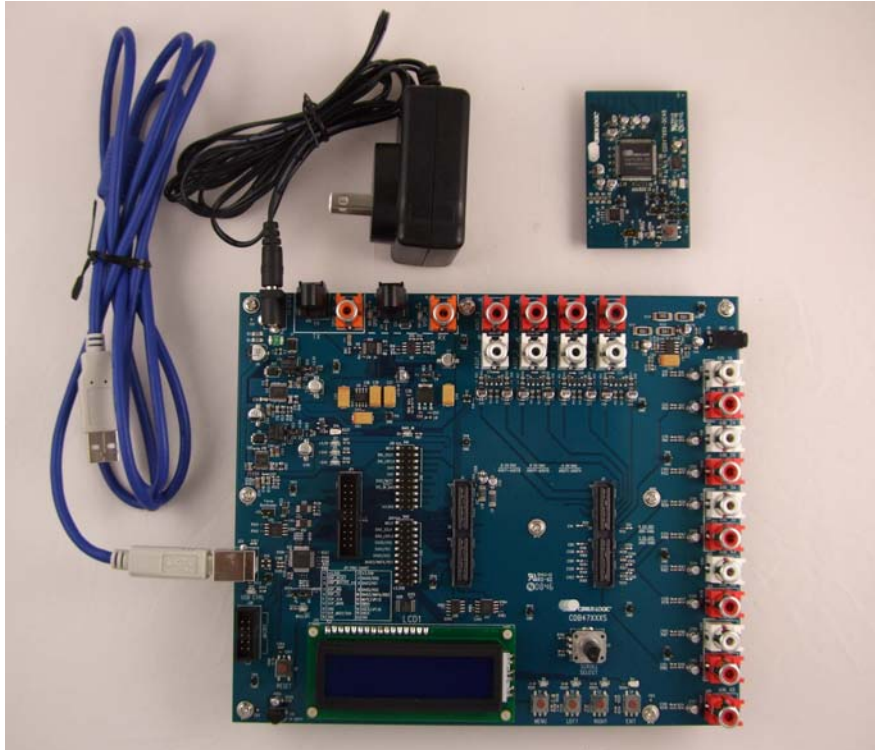


Figure 1-1. CDB47xxxS-DCxx Kit Contents

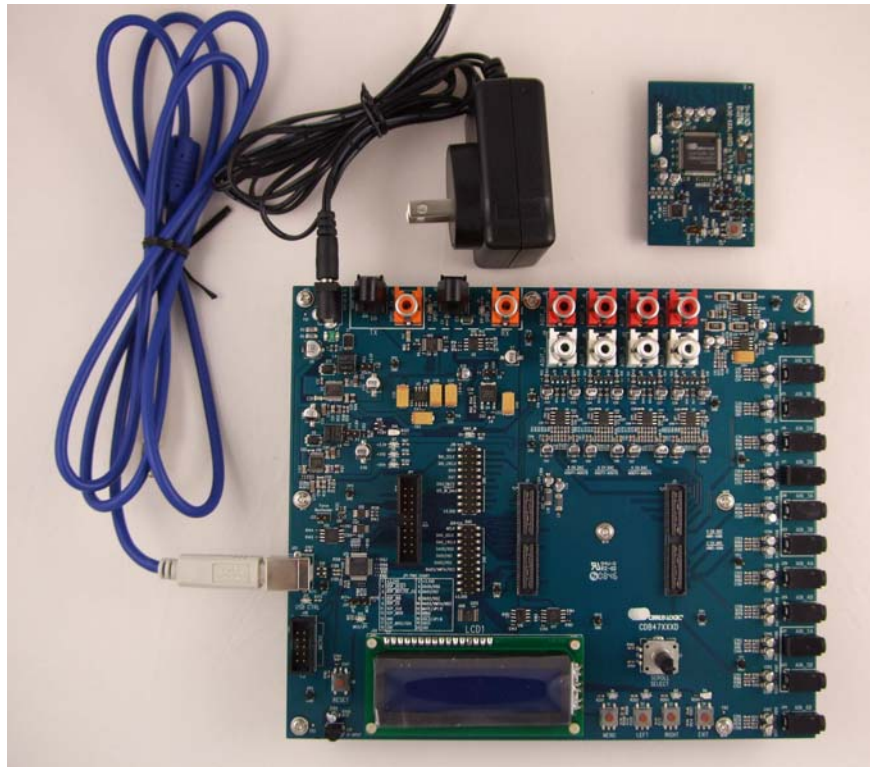


Figure 1-2. CDB47xxxD-DCxx Kit Contents

1.2 Requirements

1.2.1 PC Requirements

- Microsoft® Windows® XP with Service Pack 2 or higher or Windows 7 (32- or 64-bit) Operating System
- USB 2.0 Support

1.2.2 Software Requirements

- Cirrus® Evaluation Software Package (available from your local Cirrus Logic representative)

1.2.3 Support Hardware Requirements

- Digital or Analog Audio Source (for example, DVD player, PC with a digital audio card/device)
- Amplified Speakers for audio playback (for example, powered PC speakers, AVR/amp + speakers)

1.2.4 Cabling Requirements

- Digital Audio Inputs – S/PDIF optical cables, RCA audio cables (Connect to digital audio card, audio analyzer, or DVD player.)
- Digital Audio Output – S/PDIF Optical cable, RCA audio cable (Connect to digital audio card, audio analyzer, or AVR.)
- Analog Audio Inputs – 1/8" stereo plug microphone cable (Connect microphone to ADC), RCA audio cables (**CDB47xxxS only**), 1/8" stereo plug differential cable (**CDB47xxxD only**)
- Analog Audio Outputs – RCA audio cables (Connect CDB47xxx line-level outputs to powered speakers.)

1.3 CDB47xxx Main Board System Description

A detailed block diagram of the CDB47xxxS Development Board is shown in [Figure 1-3](#). The block diagram of the CDB47xxxD Development Board is shown in [Figure 1-4](#). The sections that follow provide a detailed description of each block.

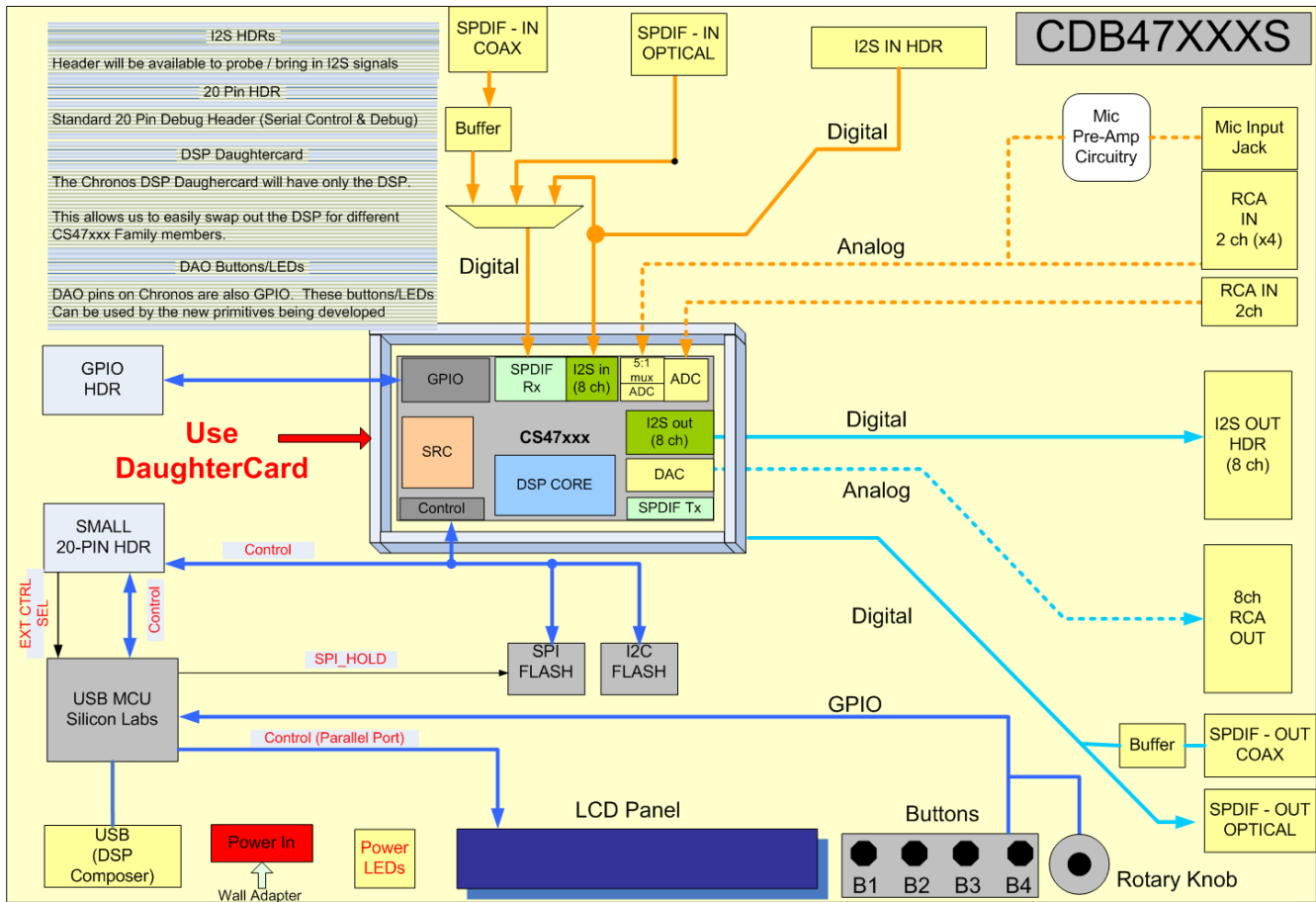


Figure 1-3. CDB47xxxS Main Board Block Diagram

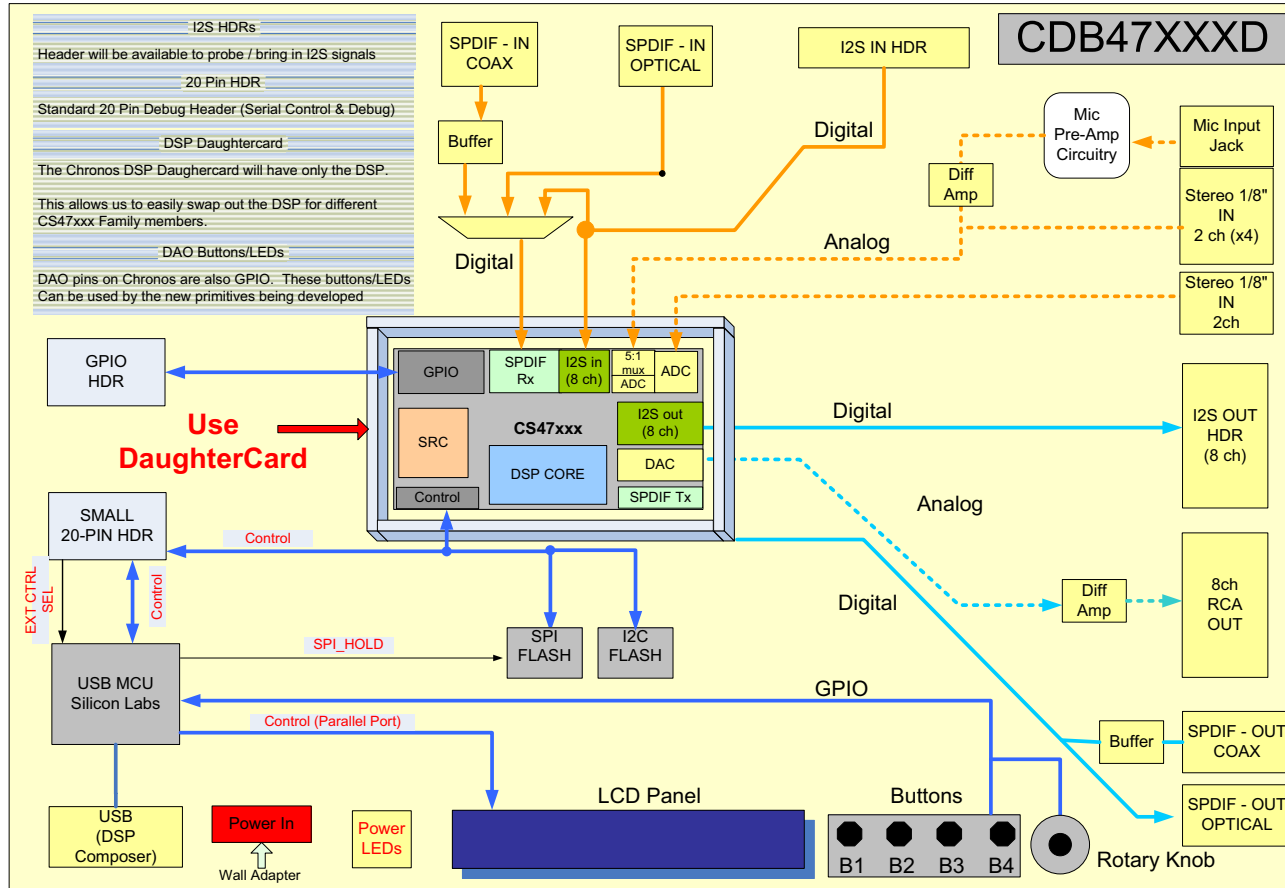


Figure 1-4. CDB47xxxD Main Board Block Diagram

1.3.1 Audio Inputs

1.3.1.1 Analog Line-level Inputs -- Single-Ended (CDB47xxxS only) (AIN1A - AIN5B, AIN6B)¹

Analog line-level inputs have the following characteristics:

- Connector Type: RCA Female
- Absolute Maximum Signal Level: 8Vp-p
- Full Scale Amplitude: 2VRMS

1.3.1.2 Analog Line-level Inputs -- Differential (CDB47xxxD only) (AIN1A - AIN5B, AIN6B)

Analog line-level inputs have the following characteristics:

- Connector Type: 3.5mm (1/8") Stereo Female
- Absolute Maximum Differential Signal Level: 16Vp-p
- Full Scale Differential Amplitude: 4VRMS

1. Reference designators are listed at the end of the heading for each board component listed in this chapter.

1.3.1.3 Optical Digital Input (J21)

Optical digital inputs have the following characteristics:

- Connector Type: Fiber Optic RX for Digital Audio, JIS F05 (TOSLINK)

1.3.1.4 Coaxial Digital Input (J4)

Coaxial digital inputs have the following characteristics:

- Connector Type: RCA Female
- Input Impedance: 75Ω
- Maximum Signal Level: 1.5Vp-p
- The CDB47xx-S, CDB47xx-D Rev B can accept 500mV Vpp signal to be amplified so that the S/PDIF Rx pin on the DSP gets a digital signal with 2V swing compatible with Vih and Vil input voltage thresholds of the DSP.

1.3.1.5 Microphone Input (J9)

The microphone input has a stereo connector, but only the LEFT channel is used for the microphone input. This input has the following characteristics:

- Connector Type: 3.5mm (1/8") Stereo Female
- Absolute Maximum Signal Level: 8Vp-p
- Full Scale Amplitude: 20mVp-p

1.3.1.6 DSP Digital Audio Input (DAI) (J18 or DAI)

The DAI connector has the following characteristics:

- Connector Type: 2x10, 0.100 inch Male Header
- Absolute Maximum Signal Level: +3.6V
- Absolute Minimum Signal Level: -0.3V

1.3.2 Audio Outputs

1.3.2.1 Main Analog Line-level Outputs (CDB47xxxS and CDB47xxxD) (J5-J8, J10-J13, or AOUT_1 - AOUT_8)

Analog line-level outputs are RCA connectors on both the single-ended and differential boards. The CDB47xxxD board has a differential to single-ended amplifier that feeds the RCA connectors. The outputs have the following characteristics:

- Connector Type: RCA Female
- Full Scale Amplitude: 2VRMS

1.3.2.2 Optical Digital Output (J1)

The optical digital output has the following characteristics:

- Connector Type: Fiber Optic TX for Digital Audio, JIS F05 (TOSLINK)

1.3.2.3 Coaxial Digital Output (J35)

The coaxial digital output has the following characteristics:

- Connector Type: RCA Female
- Maximum Signal Output Level: 1Vp-p into 75Ω load

1.3.2.4 DSP Digital Audio Output (DAO) (J24 or DAO)

The DAO connector has the following characteristics:

- Connector Type: 2x10, 0.100 inch Male Header
- Absolute Maximum Signal Level: +3.6V
- Absolute Minimum Signal Level: -0.3V

1.3.3 DC Power Input (J2)

The DC power input has the following characteristics:

- Voltage Range: +9VDC TO +12VDC
- Minimum Power: 18W supply (2A @ 9V)
- Connector Type: 2mm female barrel connector with a positive center pin

1.3.4 External Control Header (JP1)

The control header has the following characteristics:

- Connector Type: 2x10, 0.100 inch Shrouded Male
- Absolute Maximum Signal Level: +3.6V
- Absolute Minimum Signal Level: -0.3V

This connector is the interface between the CS470xx DSP and an external host. This connector is used to control the DSP when the on-board MCU is bypassed.

1.3.5 USB Connector (J25)

The control header has the following characteristics:

- Connector Type: USB Connector
- Absolute Maximum Signal Level: +5V
- Absolute Minimum Signal Level: -0.3V

1.3.6 On-Board Voltage Selection Headers (P1-P3)

The on-board voltage selection headers have the following characteristics:

- Connector Type: 1x2, 0.100 inch, Stake Header

The CDB47xxx is designed to operate from a single DC power input. The 9V power supply provided with the kit is connected to the DC power input jack (J22) and is regulated down to the system voltages (5V, 3.3V, 1.8V). The power selection headers should be installed when using the DC wall supply. This is the default mode of operation and should not need to be changed for most applications.

It is possible to bypass the regulated power supplies for any of the voltages by removing the jumper from the appropriate power selection header, and connecting an external voltage supply to pin 2 of that

selection header. Pin 1 of each header is marked with a triangle and the word "REG". Pin 2 of each header is labeled with the voltage required for that pin (+5V, +3.3V, or +1.8V).

1.3.7 Digital Audio Input Source Multiplexer (U1)

The audio input source multiplexer has the following characteristics:

- Source 1: Optical S/PDIF Input
- Source 2: Coaxial S/PDIF Input
- Source 3: Digital Audio Input (DAI) Header

This multiplexer is used to select which audio source feeds the CS470xx DAI3 pin. When the CS470xx has DAI3 configured as a S/PDIF receiver, either Source 1 or Source 2 can be selected by the MCU. When DAI3 is configured as a standard I2S input, Source 3 can be selected as the data source.

The CDB47xxx has been designed to indicate which input is currently selected by illuminating a specific LED for each Source, as described below:

- Source 1 selected: D12 will be on
- Source 2 selected: D51 will be on
- Source 3 selected: D5 will be on

1.3.8 CS470xx Audio System-On-a-Chip (ASOC)

The CS470xx ASOCs are a family of ICs designed specifically for audio applications. The CDB47xxx allows a designer to evaluate the CS470xx ASOCs in many different modes of multi-channel input and output. The 100-pin footprint on the daughtercard is compatible with any CS470xx chip that uses the LQFP100 package.

Audio input data to the ASOC can come from any of the following sources:

- Line-Level Analog Audio Input Connectors
- Optical S/PDIF Input Connector
- Coaxial S/PDIF Input Connector
- DAI Header

Audio output data from the ASOC can be sent to the following destinations:

- Line-Level Analog Audio Output Connectors
- Optical S/PDIF Output Connector
- Coaxial S/PDIF Input Connector
- DAO Header

The CS470xx can be booted from external serial Flash for custom applications in which a host MCU is not desired.

The CDB47xxx also allows the PC to act as a host to boot and configure the DSP through the GUI software for real-time configuration of the audio processing.

1.3.9 C8051 MCU

The C8051 (U15) is a USB slave controller and general purpose MCU used to control the CDB47xxx Board in stand-alone applications, and also used to interface to the PC through the USB port (DSP Composer). Standalone applications can be as simple as using the MCU to configure the inputs on the board to feed the DSP and provide a power-on-reset (POR) to the DSP. But standalone applications can also take advantage of the LCD display, buttons, and rotary encoder to provide a user interface that is managed by the C8051.

When DSP Composer is needed to perform real-time application development on the CS470xx, the USB port should be used to connect the CDB47xxx Board to a PC that has DSP Composer™ installed.

1.3.10 MCU Input: Push Buttons(S1-S4) and Rotary Encoder (S5)

The C8051 can accept user input through the buttons on the CDB47xxx when USB is not connected.

There are 4 momentary contact push-buttons provided.

There is also a rotary encoder knob that can be used to scroll up and down through options provided through the MCU interface. The rotary encoder has an integrated momentary contact push-button that is activated by pushing down on the knob.

1.3.11 MCU Output (LCD) (LCD1)

The C8051 can provide feedback to the user through the on-board LCD when USB is not connected.

1.3.12 Memory (U17, U16 and U14))

The CDB47xxx is assembled with a 32-Mbit SPI Flash (U17) and a 512-kbit I²C Flash (U16) which are dedicated for DSP firmware and configuration data. The serial control lines are routed down from the DSP through the daughter-card connectors.

There is an additional 32-Mbit SPI Flash component on the board (U14) that is used only to store MCU firmware, and it is not required by the DSP.

1.4 CDB47xxx Daughtercard System Description

The CS470xx Audio SOC Daughtercard is exactly the same for both the CDB47xxxS and CDB47xxxD evaluation kits. All of the analog and digital audio signals are fed to the CS470xx (U1) through the daughtercard connectors (J2 - J3). All of the analog pins of the CS470xx are connected to the analog daughtercard connector (J3). The distinction between a differential system and single-ended system is made on the main board where either the full differential pair is used, or only the positive (+) half of the pair.

A detailed block diagram of the CDB47xxxD(or S)-DC48 daughtercard for single-ended or differential platforms is shown in [Figure 1-5](#). The CDB47xxxD (or S)-DC28 and CDB47xxxD (or S)-DC24 daughtercards for single-ended or differential platforms are shown in [Figure 1-6](#) and [Figure 1-7](#) respectively. The sections that follow provide a detailed description of each block.

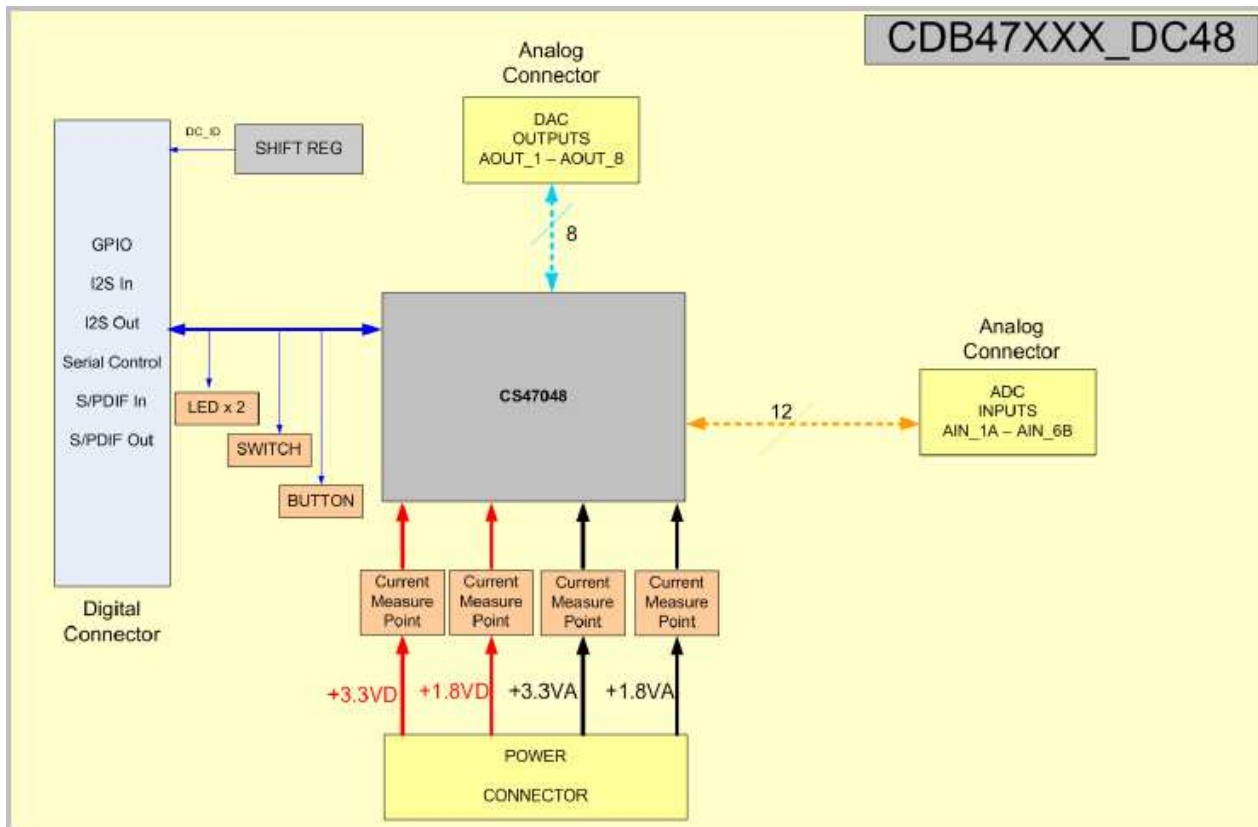


Figure 1-5. CDB47xxx-DC48 Daughtercard Block Diagram

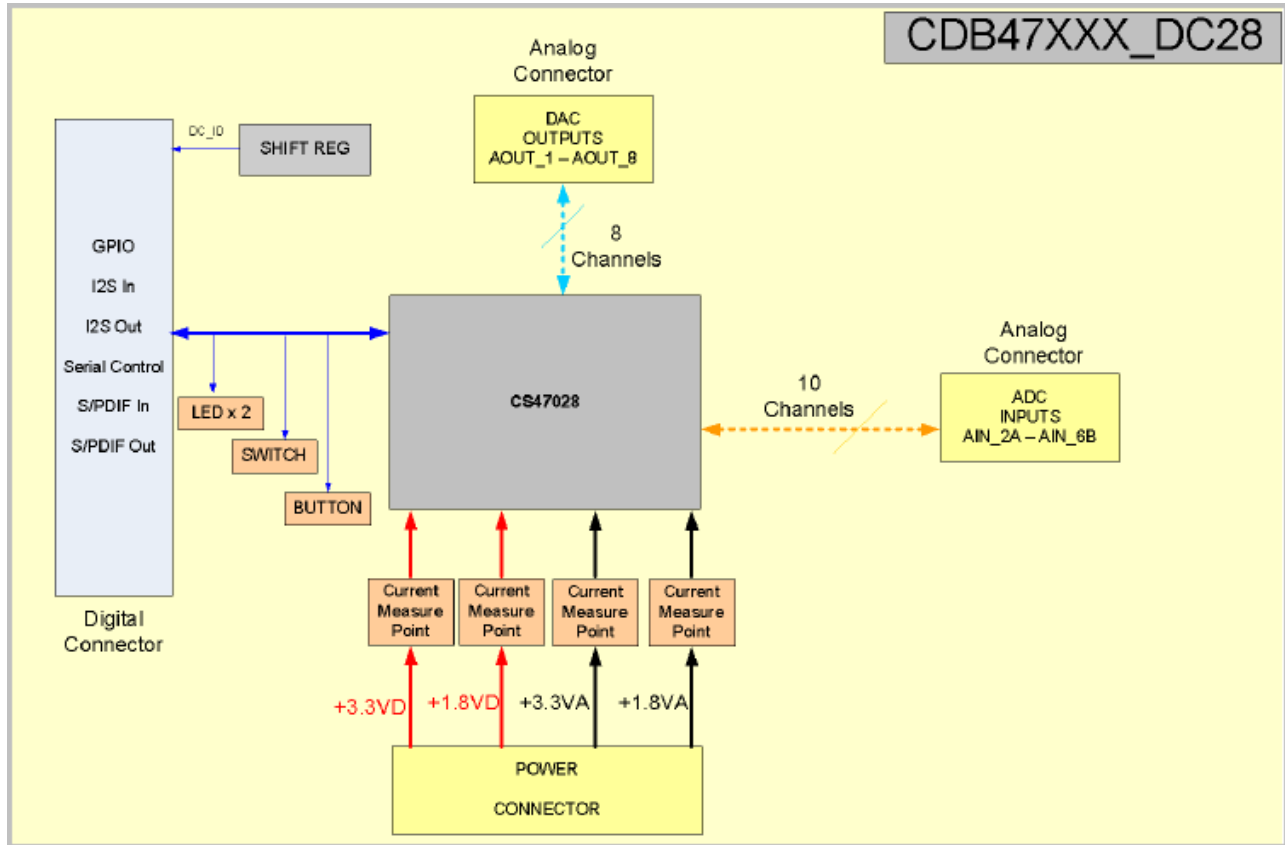


Figure 1-6. CDB47xxx-DC28 Daughtercard Block Diagram

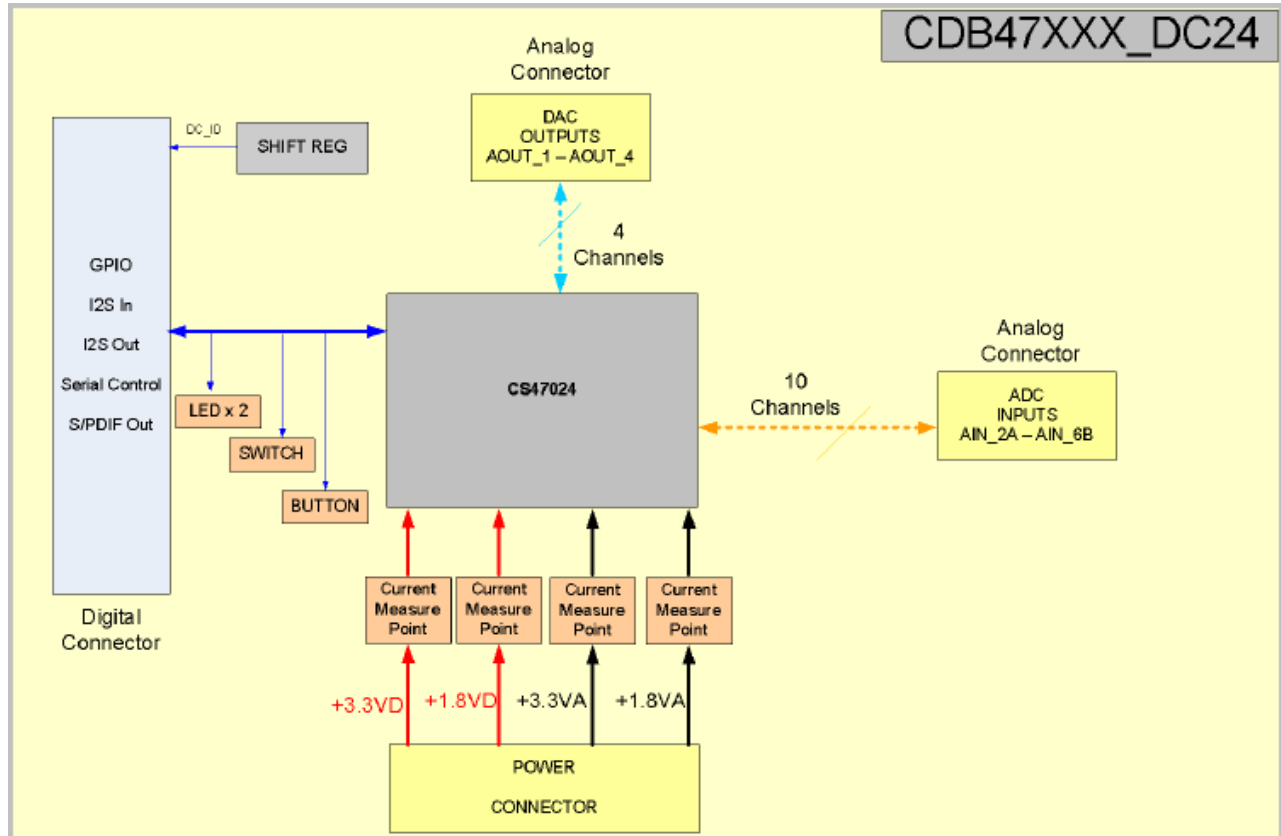


Figure 1-7. CDB47xxx-DC24 Daughtercard Block Diagram

1.4.1 Audio Inputs

1.4.1.1 Analog Line-level Inputs (J3)

Analog line-level inputs have the following characteristics:

- Connector Type: High-Density High-Speed Shrouded Female Connector
- Absolute Maximum Signal Level: These signals should only be driven from the connectors on the main board. Voltages should comply with the Max Signal Level specification for the main board circuitry.

1.4.1.2 Digital Audio Inputs (DAI) (J2)

The DAI connector has the following characteristics:

- Connector Type: High-Density High-Speed Shrouded Female Connector
- Absolute Maximum Signal Level: +3.6V
- Absolute Minimum Signal Level: -0.3V

This connector passes all serial audio data and clock signals up from the main CDB47xxx board.

1.4.2 Audio Outputs from the CS470xx DSP

1.4.2.1 Analog Line-level Outputs (J3)

Analog line-level outputs have the following characteristics:

- Connector Type: High-Density High-Speed Shrouded Female Connector
- Maximum Signal Output Level: These signals should only be driven from the connectors on the main board. Voltages will comply with the Max Signal Level specification for the main board circuitry.

1.4.2.2 Digital Audio Outputs (DAO) (J2)

The DAO connector has the following characteristics:

- Connector Type: High-Density High-Speed Shrouded Female Connector
- Absolute Maximum Signal Level: +3.6V
- Absolute Minimum Signal Level: -0.3V

This connector passes all serial audio data and clock signals up from the main CS47xxx board.

1.4.3 Control Header (J2)

The control header has the following characteristics:

- Connector Type: High-Density High-Speed Shrouded Female Connector
- Absolute Maximum Signal Level: +3.6V
- Absolute Minimum Signal Level: -0.3V

This connector passes all serial control signals up from the main CS47xxx board.

1.4.4 User Input (S1 and S2)

The CS470xx can be configured to accept user input through the slide switch and button on the daughtercard. The button and switch are connected to GPIO pins on the ASOC which are monitored by the DSP. This feature is firmware dependent and may not be available in all applications.

There is a slide switch (S1) provided. It can connect Pin 7 (GPIO0) of the DSP to either 3.3V or ground through a 10K resistor on the DSP.

There is a momentary contact push-button (S2) provided. When pressed it connects Pin 19 (GPIO3) to 3.3V through a pull-up resistor.

1.4.5 User LED Output (D1 and D2)

The CS470xx can be configured to provide user feedback through LEDs on the daughtercard. This feature is firmware dependent and will not be available in all applications.

There are 2 LEDs provided for user feedback. These LEDs light up when their associated GPIO pin is driven low by the DSP. The LEDs map to their pins as follows:

- LED D1 is connected to pin 7 (GPIO16) of the DSP.
- LED D2 is connected to pin 18 (GPIO6) of the DSP.

1.5 Audio Clocking

Clocking architecture is one of the most important aspects of an audio system. This can also be one of the most complicated parts of a system design to insure that clocking is valid and stable for all scenarios. This is one of the major advantages of the CS470xx Audio System On-a-Chip (ASOC). Because of the integrated ADC and DAC along with the integrated SRCs, the CS470xx makes audio clocking very simple. For analog-only systems, the clocking architecture is as simple as a crystal feeding the CS470xx.

Traditionally the input and output clock domains of the DSP needed to be synchronous when delivering audio data in an isochronous fashion (constant bitrate delivery), even if the input/output domains operate at different frequencies (e.g. 48 kHz input/96 kHz output). Systems utilizing serial audio data (I²S) delivery would thus use isochronous delivery.

The CS470xx's integrated SRCs remove this requirement because the CS470xx can rate match the input (DAI) Fs to any Fs on the output side (DAO). The examples below show configurations that support an Fs that is synchronized between DAI and DAO, as well as an output Fs that is independent of the input Fs.

1.5.1 Clock and Data Flow for ADC Input

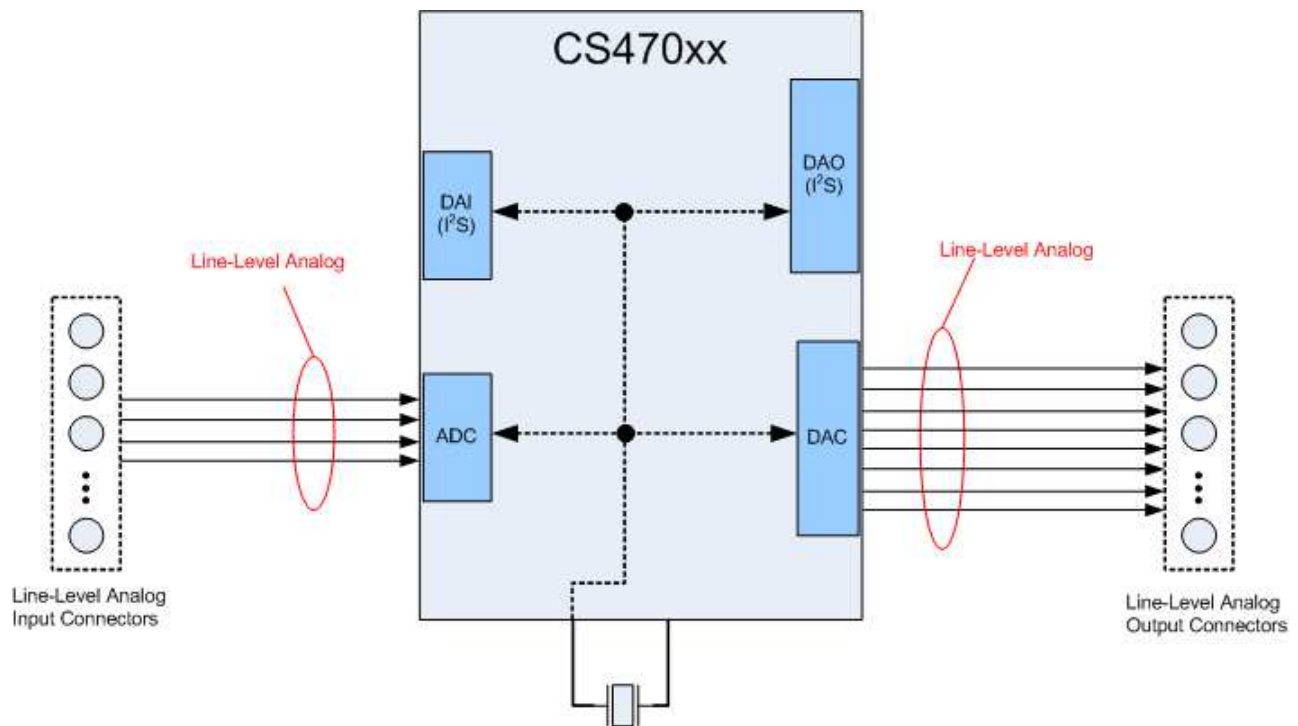


Figure 1-8. ADC Clocking

The ADC clocking architecture is used when the internal ADCs are used as the only audio input (that is, SPDIF is disabled and there are no serial audio signals connected to DAI or DAO). In this scenario, the CS470xx has all audio clocking self contained. [Figure 1-8](#) illustrates this clocking configuration.

The clock fed to XTI of the CS470xx is MCLK for the system, and the ASOC masters clocks to DAC and ADC. The user need only route in analog signals and route out the processed analog signals.

1.5.2 Clock and Data Flow for S/PDIF Input

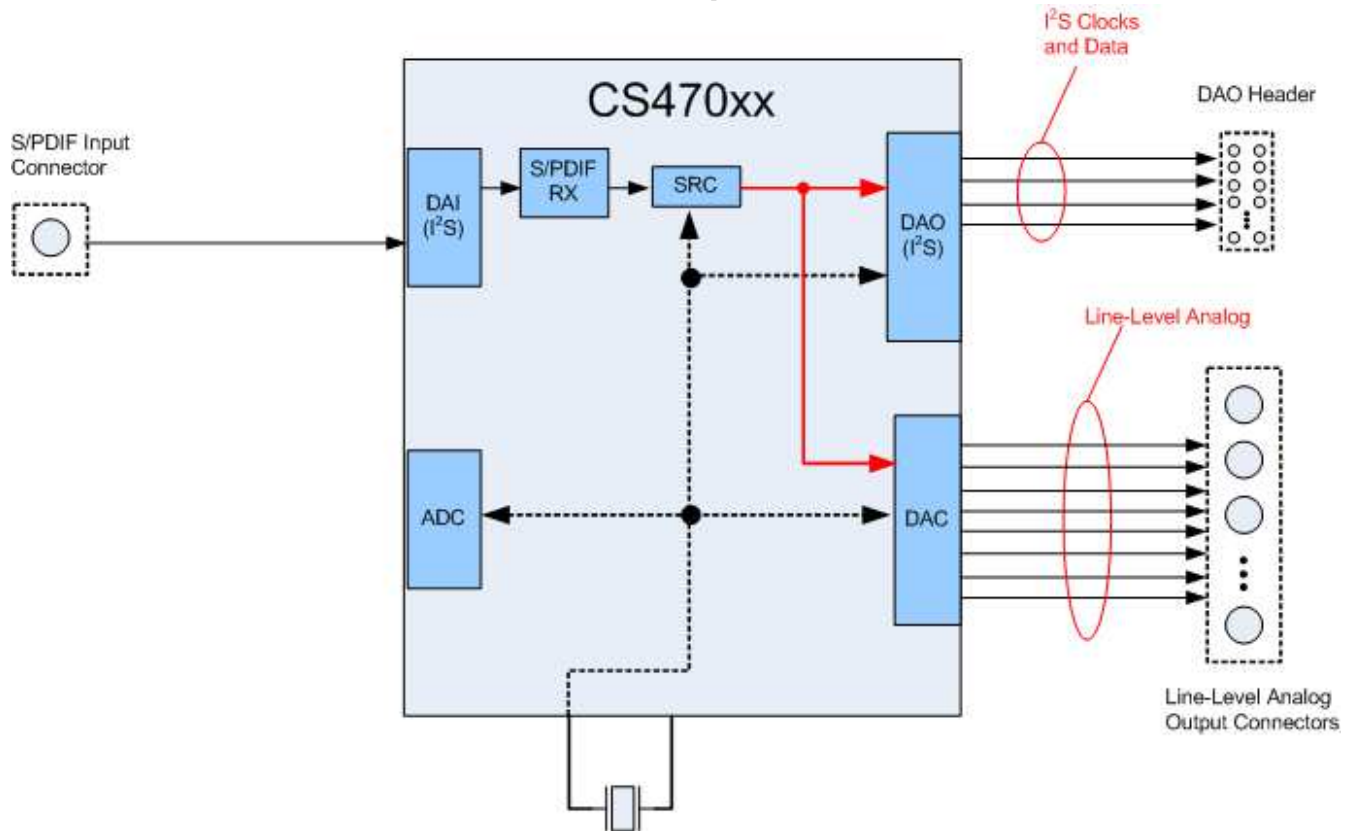


Figure 1-9. S/PDIF Clocking

The S/PDIF clocking architecture is used when any S/PDIF RX is used as an audio source, whether from the optical RX, coaxial RX, or brought in on the DAI header. [Figure 1-9](#) illustrates this clocking configuration.

The incoming S/PDIF stream is always rate matched to another MCLK in the system through an SRC. This means that the DAO can be run at a constant F_s that is independent of the incoming S/PDIF F_s . This is useful in systems with digital amplifiers and wireless audio transmitter modules that requires a fixed F_s .

The CS470xx can master its output clocks, or slave to clocks from another source.

1.5.3 Clock and Data Flow for DAI Input with Fixed Output Fs

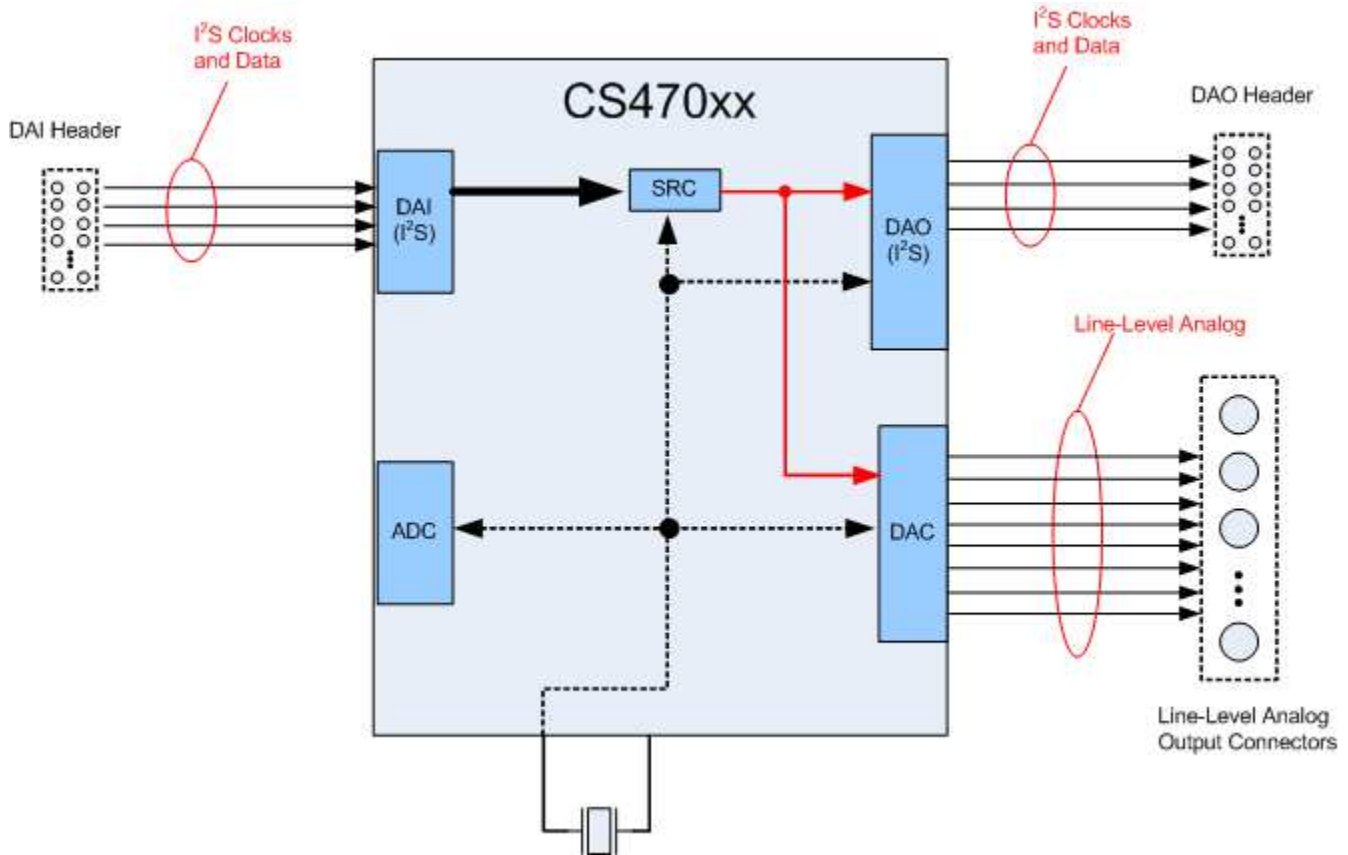


Figure 1-10. DAI Clocking with Variable Input Fs and Fixed Output Fs

The DAI clocking architecture is used when any serial audio data source is connected to the DAI header. [Figure 1-10](#) illustrates this clocking configuration. Note that the incoming DAI data is passed out of the CS470xx at the Fs of the crystal connected to the ASOC.

Like the S/PDIF clocking configuration, this allows the DAI to be rate matched to another MCLK in the system through an SRC. This means that the DAO can be run at a constant Fs that is independent of the incoming DAI Fs. This is useful in systems with a digital amplifier that requires a fixed Fs.

The CS470xx can masters its output clocks, or slave to clocks from another source.

1.5.4 Clock and Data Flow for DAI Input with Matched DAO Fs

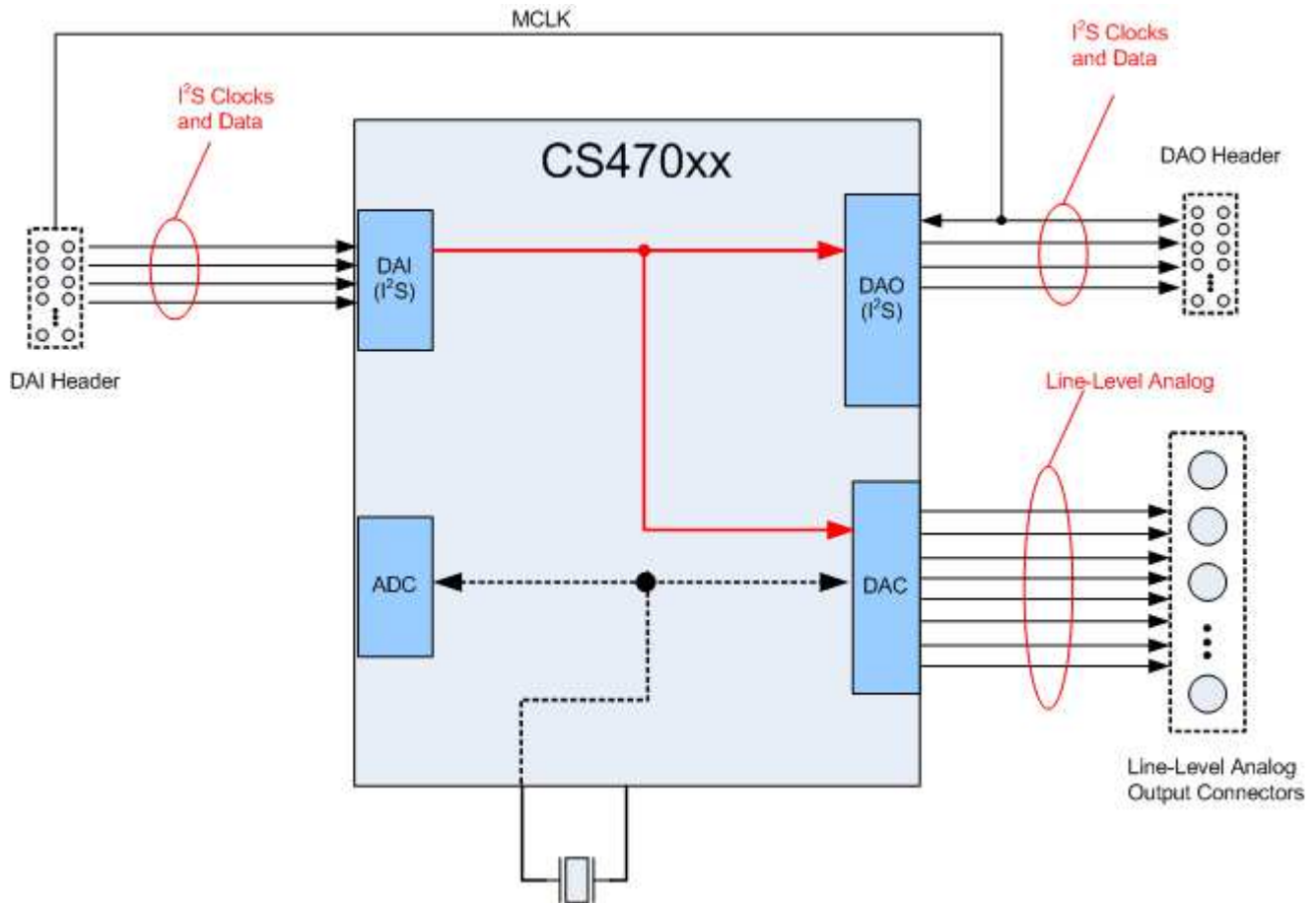


Figure 1-11. DAI Clocking with Fixed Output Fs

The DAI clocking architecture is used when any serial audio data source is connected to the DAI header. [Figure 1-11](#) illustrates this clocking configuration. Note that the incoming DAI data is synchronized to the DAO using a common MCLK.

This is a more traditional clocking architecture for serial audio data, where the DAI Fs and the DAO Fs are synchronous. In this configuration, the SRC is bypassed for the DAO.

1.6 Other Useful Information

1.6.1 Web Sites

- Cirrus Logic main web site: www.cirrus.com

1.6.2 DSP Information

The following information can be obtained from your Cirrus Logic representative.

- *CS470xx Data Sheet*
- *CS470xx Hardware User's Manual*
- AN333, *CS470xx Firmware User's Manual*

1.6.3 Board Information

- The following information can be obtained from your local Cirrus Logic representative.
- Schematics
- BOM
- Artwork and PCB stackup

1.6.4 DSP Software Utility Information

The following information can be obtained from your local Cirrus representative.

- *DSP Composer™ User's Manual*
- *DSP Composer™ Primitive Elements Reference*

The documents listed above are updated periodically and may be more up-to-date than the information in this document. Contact your Cirrus Logic sales representative for the latest updates.