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**CDB48500**  
*High-performance, 32-Bit Audio Decoder DSP Family*

# ***CDB48500-USB***

## **USB Evaluation Kit Guide**

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**Introduction to the CRD48500-USB Evaluation Kit**

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**1.1 CDB48500-USB Kit Contents and Requirements****1.1.1 CDB48500-USB Kit**

Each CDB48500-USB kit comes with the following:

- CDB48500 Development Board (See [Figure 1-2](#))
- Power Supply: +9V, 1.67A, 100V - 240V, with AC Power Cord
- CDB USB MASTER Digital I/O Card (See [Figure 1-2](#))
- USB Cable
- 3 Board Overlays Identifying the Outputs for CS48520, CS48540, and CS48560
- Document Card Explaining How to Get the Latest Board Software

**1.1.2 PC Requirements**

- Microsoft Windows XP® or Windows 7® Operating System
- USB 2.0 Support

**1.1.3 Software Requirements**

- Cirrus Evaluation Software Package (available from your local Cirrus Logic representative)

**1.1.4 Support Hardware Requirements**

- Digital or Analog Audio Source (e.g. DVD player, PC with a digital audio card/device)
- Amplified Speakers for audio playback (e.g. powered PC speakers, AVR/amp + speakers)

**1.1.5 Cabling Requirements**

- Digital Audio Inputs – S/PDIF Optical or Coaxial RCA Cables (Connect to digital audio card, audio analyzer, or DVD player.)
- Digital Audio Output – S/PDIF Optical Cable (Connect to digital audio card, audio analyzer, or AVR.)
- Analog Audio Inputs – RCA Audio Cables (Connect CDB48500 line-level inputs to analog audio source.)
- Analog Audio Outputs – RCA Audio Cables (Connect CDB48500 line-level outputs to powered speakers.)

**1.2 Introducing the CDB48500-USB Customer Development Kit**

The CDB48500-USB kit is composed of the CDB48500 customer development board and the CDB USB MASTER Control board. The CDB48500 provides a practical platform for emulating a typical multi-channel audio system application. The CDB USB MASTER is a USB control board used to interface the host PC to the CDB48500 board, and convert GUI commands into the serial control protocol required for configuring the CS485XX DSP, (2)CS42448 codecs, and CS8416 S/PDIF receiver ICs. [Figure 1-1](#) shows the relationship

between the PC, CS485XX, and the CDB USB MASTER

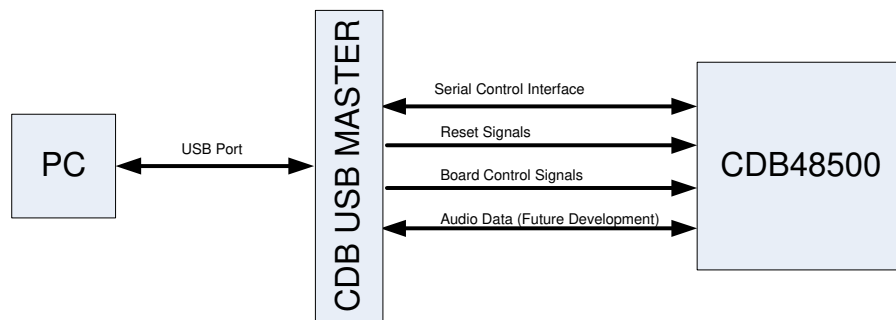


Figure 1-1. CDB48500-USB System Block Diagram

This document will concentrate on the features and basic operation of the CDB48500-USB board. Detailed information regarding the operation and programming of the CS485XX DSP is covered by the CS485XX data sheet, CS485XX Hardware User's Manual, and application note AN298 (see [Section 1.2.2, "Related Documentation"](#) on page 1-4 for more details).

The CDB48500-USB is a convenient and easy-to-operate evaluation platform. It has been designed to demonstrate the majority of the CS485XX functions on a small 6" x 6.5" base board. These features include:

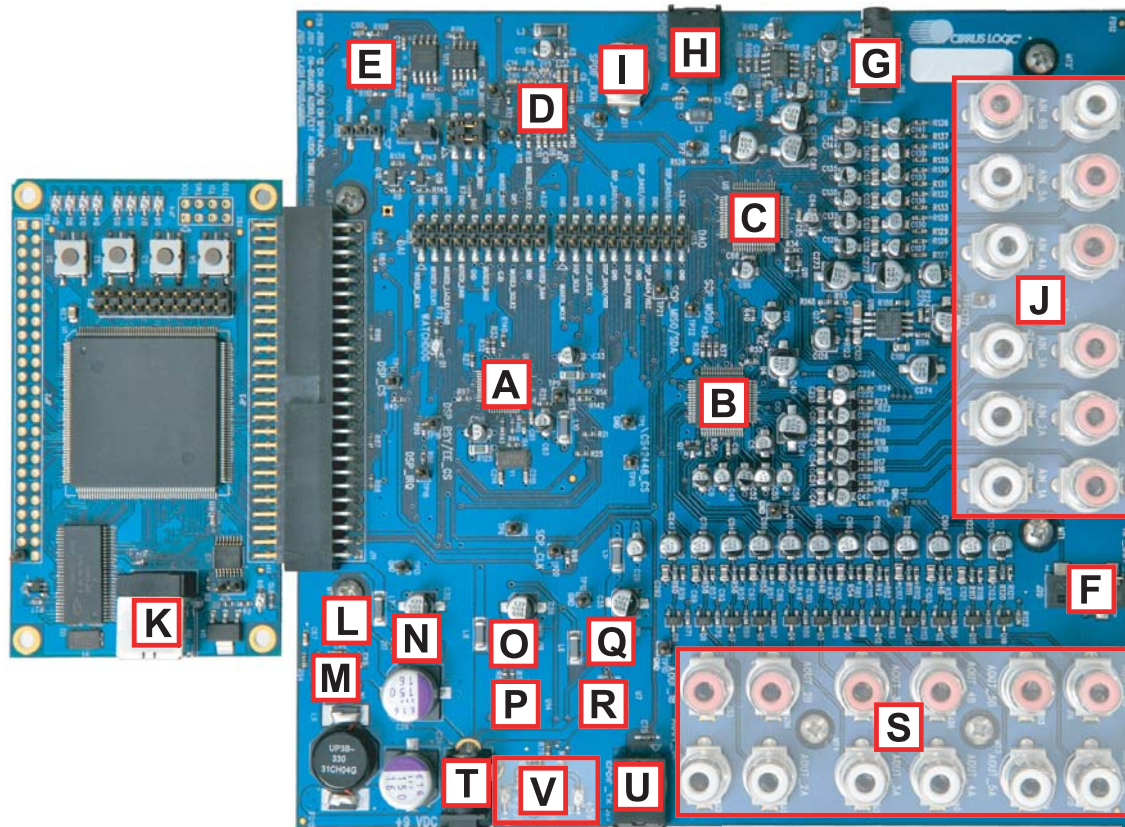
- PC control of the CS485XX using the DSP Composer™ graphical user interface
- Serial control of audio devices on CDB48500 via I<sup>2</sup>C® or SPI™ protocols
- Digital audio input of PCM via optical or coaxial S/PDIF (does not support compressed data input)
- Up to 12-channel analog audio input via the two CS42448 audio codecs
- Up to 12-channel analog output through the two CS42448 audio codecs
- Digital audio output of PCM data via optical S/PDIF
- Headphone output jack
- Multi-channel digital audio input via the CDB USB MASTER card (not yet supported)
- Separate input and output clocking domains to allow 1FS-to-2FS audio processing on the CS485XX
- Fast boot – host-controlled master boot (HCMB) of custom applications from 4 Mbit serial SPI flash device.
- Microphone input with integrated amplifier for Intelligent Room Calibration (IRC) evaluation (future)
- Supports all members of the CS485XX family in the 48-pin LQFP package.

**Note:** Not all features of the CS485xx are exercised on the CDB48500.

## 1.2.1 Identifying CDB48500-USB Components

[Figure 1-2](#) shows the top side of the CDB48500-USB Evaluation Board. The accompanying legend identifies the main components of the board.





### Legend:

A.CS485XX DSP, U6

E.4 Mbit Serial Flash, U11

I. Coaxial S/PDIF Input Jacks (PCM only), J31

M.+3.3V Switching Regulator (1.5A), U8

Q.+5V Selection Header (Regulator/ External), J19

U.Optical S/PDIF Output Jack, J24

B.CS42448 Audio CODEC, U4

F.Headphone jack, J20

J.Analog Inputs, 2 Vrms Max

N.+3.3V Selection Header (Regulator/ External), J17

R.+5V Linear Regulator (1A), U7

V.Power Indicator LEDs

C.CS42448 Audio CODEC, U5

G.1/8" Microphone Input Jack, J5

K.USB Connector on CDB USB Master, P1

O.+1.8V Selection Header (Regulator/ External), J18

S.Analog Audio Outputs

W.On-board/External Digital Audio Mux, U1 & U2 (U1 & U2 are on back of PCB.)

D.CS8416 S/PDIF Receiver, U3

H.Optical S/PDIF Input Jacks (PCM only), J2

L.Alternate +12V Jumper, J3

P.+1.8V Linear Regulator (1A), U14

T.DC Power Input Jack, +9Vdc to +12Vdc, J25

Figure 1-2. CDB48500-USB Top View

## 1.2.2 Related Documentation

The documents described in this section are updated periodically and may be more up-to-date than the information in this document. Check the Cirrus Logic Internet site for the latest updates.

### 1.2.2.1 Additional CDB48500 Evaluation Board Information

The following information about the CDB48500 Evaluation Board can be obtained from your Cirrus Logic representative:

- Schematics
- BOM
- Artwork and PCB stackup

### 1.2.2.2 CS485xx Family DSP Hardware Information

The following documents are installed with the CS485xx System Development Kit (SDK).

- *CS485xx Family Data Sheet*
- *CS485xx Hardware Users Manual*
- CS485xx Errata

### 1.2.2.3 CS485xx Family DSP Software Information

The following document is installed with the CS485xx SDK:

- AN298, *CS485xx Firmware User's Manual*

### 1.2.2.4 DSP Software Utility Information

The following document is installed with the CS485xx SDK:

- *DSP Composer User's Manual*

The documents listed above are updated periodically and may be more up to date than the information in this document. Check the Cirrus Logic Internet site for the latest updates.

### 1.2.2.5 Audio CODEC Information

The following information is located on the [www.cirrus.com](http://www.cirrus.com) Internet site:

- *CS42448 Data Sheet*
- CS42448 Errata

### 1.2.2.6 S/PDIF Receiver Information

The following information is located on the [www.cirrus.com](http://www.cirrus.com) Internet site:

- *CS8416 Data Sheet*
- CS8416 Errata

§§1

## Board Setup and Installing the Evaluation Kit Software

### 2.1 Introduction



It is important to install the Evaluation Software BEFORE connecting the USB cable from the PC to the CDB USB MASTER card. Failure to install the evaluation software before the initial connection can result in an inability to communicate with the CBD485xx.

#### 2.1.1 Installing the Evaluation Kit Software

The DSP evaluation software installation will first install the Cirrus Logic DSP evaluation software followed by the USB drivers required to communicate with the CDB USB MASTER.

1. Run the latest DSP evaluation software installation executable (*CS485xx\_eval\_kit\_rc<revision number>.exe*). This executable is supplied by your Cirrus Logic representative.
2. At the **Welcome** screen, click **Next**.
3. At the **Licensing Agreement** window, select the “**I accept the agreement**” radio button to agree to the terms and then select **Next**.
4. Select the **Destination Location** window, Select the default location “*C:\CirrusDSP*” and click **Next**.
5. Select **Start Menu Folder** window, Select the default location “*C:\CirrusDSP*” and click **Next**.
6. The **Ready to Install** window indicates the selected destination location and the **Start** menu folder for confirmation, select **Install** to begin the install process which should take less than one minute.
7. After the DSP evaluation software is installed, the installer will launch the **Front Panel Driver Setup Wizard** (below). Click *Next* to continue the installation.



Figure 2-1. CDB USB MASTER Driver Setup

8. The **Opal Kelly Licensing Agreement** window will appear next. Click **"I Agree"** to agree to the terms and continue.
9. The next window asks the user to choose components for installation. By default, only one component is available and is pre-selected – **Unified USB Driver**. Click **Next** to continue.
10. The wizard will then ask the user to choose the install location. Select the default location of *"C:\Program Files\Opal Kelly\FrontPanel"* and click **Install**. This should take only a few seconds.
11. Click **Finish** once the wizard has completed installation of the drivers.
12. The Cirrus DSP evaluation software will then prompt the user to click **Finish** to exit the Setup wizard.

## 2.1.2 Setting up the Evaluation Kit Boards

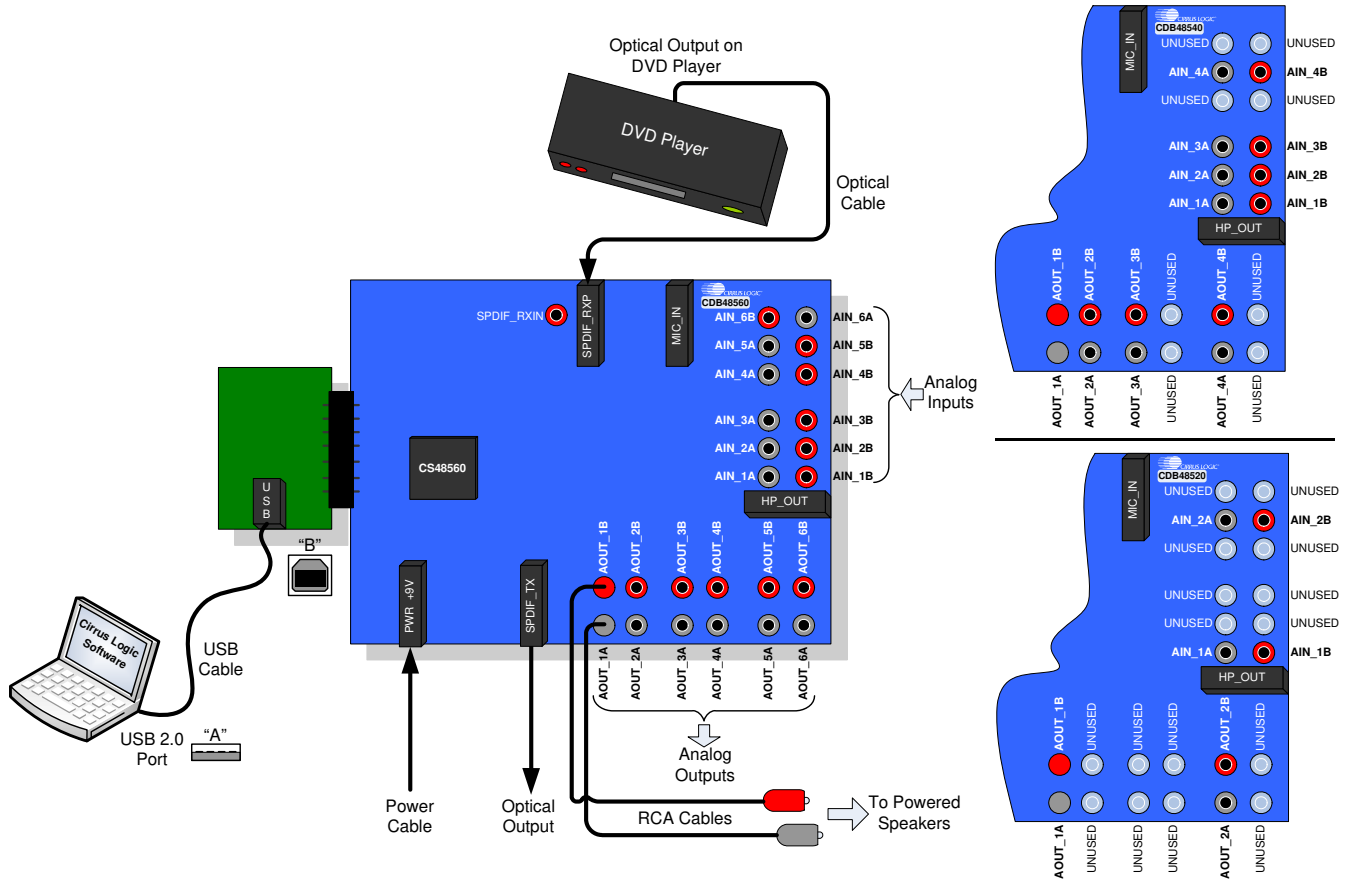


Figure 2-2. Board Setup Diagram

1. Place the CDB48500 and the CDB USB MASTER on a static-free surface.
2. If the boards are not mated, connect them together as shown in [Fig. 2-2](#). Notice that the USB connector on the CDB USB MASTER and the power connector on the CDB48500 are on the same side.
3. Connect the Power Supply as follows:
  - A. Connect the power supply jack to the CDB48500 board at J25 and the adapter to a wall power socket or power strip.
  - B. Check that the D3 (green, 3.3V), D2 (red, 1.8V), and D4 (orange, 5V) power indicator LEDs illuminate on the CDB48500.
4. Setup Audio Input connections to the CDB48500 as follows:
  - A. Connect one end of the digital audio S/PDIF optical cable to SPDIF\_RXP on the CDB48500 board.

- B. Connect the other end of the optical cable to the optical output on the back of a DVD player or other digital audio source.
5. Setup Audio Output connections from CDB48500 as follows:
  - A. The RCA connectors labeled AOUT\_1A and AOUT\_1B are the left and right analog output channels.
  - B. Use the RCA audio cables to connect these line-level analog outputs to powered speakers.

### 2.1.3 Connecting to a PC

Follow these steps to connect to a PC:

1. Connect the “B” end of the USB cable to P1 on the CDB USB MASTER USB Digital I/O Card.
2. Connect the “A” end of the USB Cable to a USB 2.0 port on a notebook or PC running Win XP.
3. Windows® should recognize that a new device has been attached and display a notice saying “**Found New Hardware**”.



Figure 2-3. Found New Hardware Service Window

4. Windows will display the **Found New Hardware Wizard** (below). Select the *No, not at this time* radio button so that Windows does not connect to Windows Update for the drivers. Click *Next*.



Figure 2-4. Found New Hardware Wizard Welcome Window

5. Windows will then ask whether to use automatic installation or manual installation. Allow Windows to install the software automatically and click *Next*.





Figure 2-5. Found New Hardware Wizard Finish Window

6. It is possible that during the installation, Windows might issue a warning that the drivers have not passed “Windows Logo” testing. Select *Continue Anyway*.



Figure 2-6. Microsoft® Windows XP® Message Screen

7. Windows should now locate the correct drivers and complete the installation.

## 2.1.4 Running a Stereo PCM Application on CDB48500-USB

To run a stereo PCM application, follow these steps:

1. Launch DSP composer (**Start** → **Program** → **Cirrus Logic DSP** → **CS485XX** → **DSP Composer**).
2. In DSP Composer, go to **File** → **Open** and open the appropriate project.
3. Press the **GO** button
4. Insert PCM material into the DVD player (e.g., music CD). If a DVD is being used as the audio source, make sure that the DVD Player (or other digital audio source) is configured to output PCM data.
5. Press **Play** on the DVD player (or other digital audio source). You should now hear audio from the speakers.

## 2.1.5 Downloading Other Applications

Separate project files (.cpa) are provided for other applications such as Dolby® Pro Logic® II, DTS Neo6™, Audistry® by Dolby®, SRS® Circle Surround®. In order to evaluate these, please contact your local FAE to ensure the necessary licensing agreements have been completed. Please note that the CDB48500-USB does not support multi-channel decoding such as Dolby Digital® or DTS® because the CS485XX DSP is only a post-processor and does not contain a decoder.

§§

A detailed block diagram of the CDB48500 Customer Development Board is shown in Figure 3-1. The sections that follow provide a detailed description of each block.

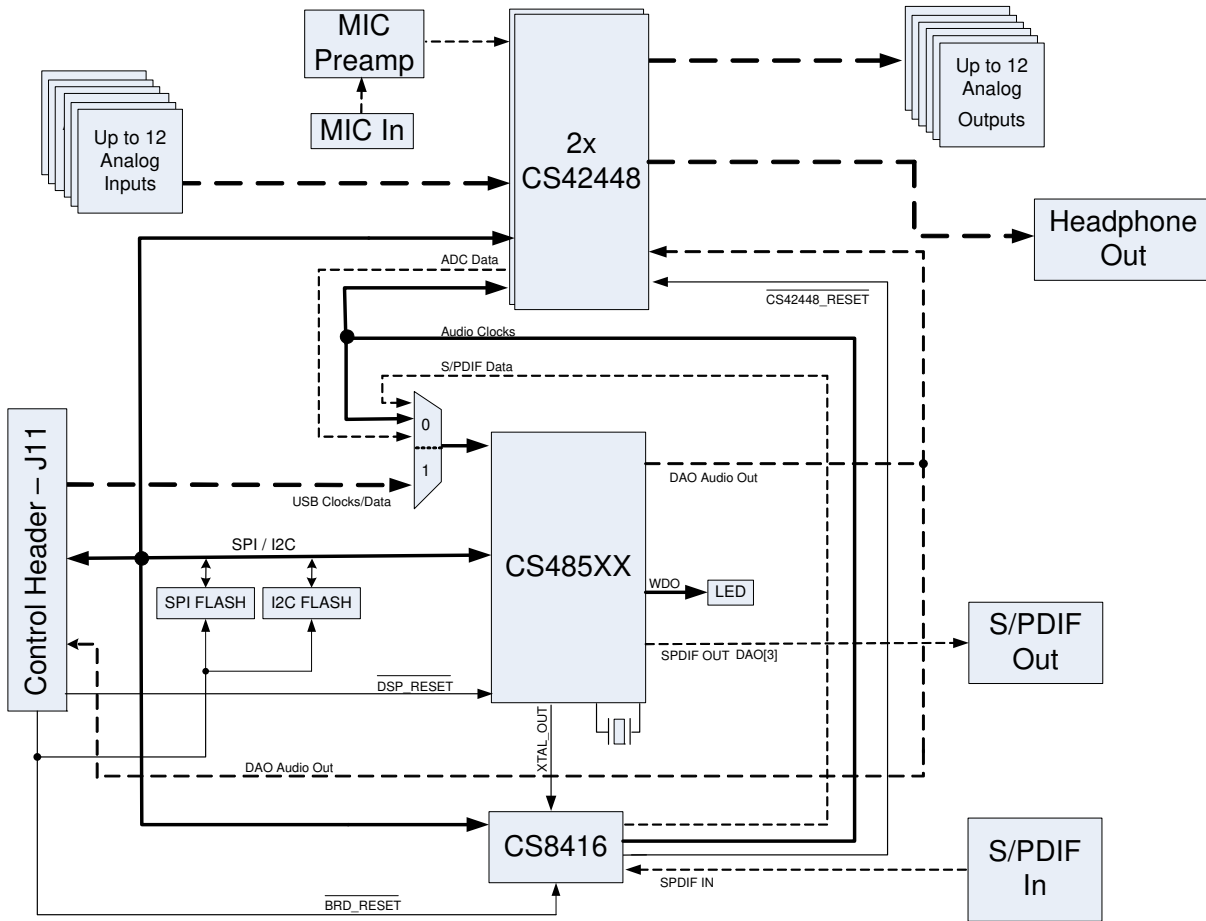


Figure 3-1. CDB48500 Block Diagram

## 3.1 CDB48500 System Block Descriptions

### 3.1.1 Audio Inputs

#### 3.1.1.1 Analog Line-level Inputs

- Connector Type: RCA Female
- Absolute Maximum Signal Level: +6.5V
- Absolute Minimum Signal Level: GND - 0.7V
- Full Scale Amplitude: 2VRMS
- Reference Designators: J4, J6-J10, J12, J26-J30, or AIN1A - AIN6B

#### 3.1.1.2 Digital Optical Input

**Note:** Digital Optical Input is PCM only as there is no multi-channel decoder present on CDB48500-USB.

- Connector Type: Fiber Optic RX for Digital Audio, JIS F05 (JIS C5974-1993 F05)
- Reference Designator: J2, or SPDIF\_RXP

#### 3.1.1.3 Digital Coaxial Input

**Note:** Digital Coaxial Input is PCM only as there is no multi-channel decoder present on CDB48500-USB.

- Connector Type: RCA Female
- Maximum Signal Level: +3.3V
- Minimum Signal Level: GND - 0.7V
- Reference Designator: J31, or SPDIF\_RXN

#### 3.1.1.4 Microphone Input

- Absolute Maximum Signal Level: +5V
- Absolute Minimum Signal Level: GND - 0.7V
- Full Scale Amplitude: 7mVp-p
- Reference Designator: J5

The microphone preamplifier shares the AIN1\_5 ADC with the AIN3\_A RCA jack. Only one analog source can be sampled at any given time. When the microphone input is selected, the AIN3\_A audio jack is ignored. The default configuration enables the AIN3\_A audio jack.

### 3.1.2 Audio Outputs

#### 3.1.2.1 Analog Line-level Outputs

- Connector Type: RCA Female
- Full Scale Amplitude: 1.21VRMS
- Reference Designators: J13-J16, J33-J40, or AOUT\_1A - AOUT\_6B

#### 3.1.2.2 Headphone Output

- Connector Type: 1/8" TRS Female
- Full Scale Amplitude: 3.53 VRMS
- Reference Designator: J20, or HP\_OUT

### 3.1.2.3 Optical Digital Output (PCM)

- Connector Type: Fiber Optic TX for Digital Audio, JIS F05 (JIS C5974-1993 F05)
- Reference Designator: J24, or SPDIF\_TX

The S/PDIF output uses the same data line as AOUT\_4A and AOUT\_4B. When the digital output has been enabled, and you have speakers connected to AOUT\_4A and AOUT\_4B white noise will be heard. This could damage the speakers.

### 3.1.3 DC Power Input

- Voltage Range: +9VDC TO +12VDC
- Minimum Power: 8W supply
- Connector Type: 2mm Female, positive center pin
- Reference Designator: J25

### 3.1.4 Control Header

- Connector Type: 2x25, 0.100 inch Shrouded Male
- Reference Designator: J11

This connector is the interface between the CDB48500 and the CDB USB MASTER. Control signals, clocks, data, and +3.3V power are passed across this connector.

### 3.1.5 On-Board Voltage Selection Headers

- Connector Type: 1x3, 0.100 inch, Stake Header
- Reference Designator: J17 - J19

The CDB48500-USB is designed to operate from a single DC power input. The 9V power supply provided with the kit is connected to the DC power input jack (J25) and is regulated down to the system voltages (5V, 3.3V, 1.8V). The power selection headers should be set to the 'REG' position when using the DC wall supply. This is the default mode of operation and should not need to be changed for most applications.

It is possible to bypass the regulated power supplies for any of the voltages by removing the jumper from the appropriate power selection header, and connecting an external voltage supply to the center pin of that selection header.

The third configuration for the power selection headers is the 'EXT' position. This is a special mode of operation, and cannot be used while connected to the CDB USB MASTER control board. Placing the power selection headers in the 'EXT' position while connected to the CDB USB MASTER will prevent the board from operating.

The unpopulated header, J3, is also designed for a special mode that brings 12V from the control header, but cannot be used when connected to the CDB USB MASTER.



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### 3.1.6 Audio Input Source Multiplexer Selection Headers

The CDB48500-USB includes jumpers to change DSP DAI inputs.

- Source 0: CDB USB MASTER Board, controlled from Software (Refer to [Section 4.2.2, “Changing the Audio Input Source”](#) on page 4-3)
- Source 1: 2 Channels from CS8416 and 8 channels from (2)CS42448, short pins 2 and 3 of J100
- Source 2: 12 Channels from (2)CS42448 codecs, short pins 1 and 2 of J100
- Reference Designators: U1, U2, U9, U18, and J100

These multiplexers are used to select which audio sources feed the CS485XX DAI pins. When the on-board sources (CS8416, U3 and CS42448, U4 and U5) are being used, the CDB USB MASTER data cannot be processed.

The CDB48500 contains a header to connect DAI pins, DAO pins, and clocks to external circuitry. The DAO and clock pins are

- DAI[5,3:0] feed from J102 header, short pins 1 and 3 on J101
- DAI[5,3:0] feed from on board sources, short pins 3 and 5 on J101
- DAI[4] feed from J102 header, short pins 2 and 4 on J101
- DAI[4] feed from on board sources, short pins 4 and 6 on J101
- The DAO pins and clocks are paralleled to both the on board devices and J102, J103 headers

### 3.1.7 Cirrus Logic CS485xx Audio DSP

The CS485xx audio DSP (U6) are a family of 32-bit fixed point processors designed specifically for audio applications. The CDB48500 allows a designer to evaluate the CS485xx DSPs in many different modes of multi-channel input and output. The 48-pin footprint on this board is compatible with any CS485XX chip.

Audio input data to the DSP can come from any of the following sources:

- CS8416 (U3)
- CS42448 (U4 and U5)
- CDB USB MASTER card
- Header for external codecs (not yet supported)

Audio output data from the DSP can be sent to the following destinations:

- Both CS42448's for conversion to Analog Output (AOUT\_1A - AOUT\_6B)
- Optical S/PDIF Out (SPDIF\_TX), this option disables AOUT\_4A and AOUT\_4B
- CDB USB MASTER card

The CS485XX has many applications stored in internal ROM, but a host is still required to configure the application for a particular system. The CDB48500-USB allows the PC to act as a host to boot and configure the DSP through the GUI software.

The CS485XX can also be booted from external serial flash for custom applications that are not stored in the DSP's ROM.

**Note:** The 48-pin footprint on this board is also compatible with the CS485XX family of DSPs. The CDB48500 can support any CS485XX chip if the alternate stuffing options shown on the DSP schematic page have been followed.

### 3.1.8 CS8416 S/PDIF RX

The CS8416 (U3) is a 192 kHz S/PDIF receiver with an integrated input multiplexer. The two S/PDIF input jacks (RXP-RXN) are connected to the CS8416. Only one of the optical or coaxial S/PDIF jacks can be used at a time and is automatically selected by the CS8416. When S/PDIF audio is being processed, the CS8416 must master MCLK for the system (see ["Audio Clocking" on page 1-5](#) for details).

### 3.1.9 CS42448 Audio CODEC

The CS42448 (U4 and U5) is a high-performance, multi-channel audio CODEC capable of supporting sample rates up to 192 kHz on its 6ADCs and 8 DACs. There are two of these devices on the CDB48500 and are used for all analog-to-digital and digital-to-analog conversions.

All analog inputs (AIN\_1A-AIN\_6B) and all analog outputs (AOUT\_1A-AOUT\_6B) are connected to the CS42448s. The microphone input shares the AIN1\_5 ADC with the AIN\_3A RCA jack. When the microphone is in use, the AIN\_3A RCA jack is ignored.

When analog audio is being processed, the 24.576 MHz crystal for the CS485XX must master MCLK for the system (see [Section 3.1.11](#) for details).

### 3.1.10 Memory

The CDB48500 is populated with two 4 Mbit SPI flash devices and one I<sup>2</sup>C EEPROM. Selection from SPI to I<sup>2</sup>C is changed in Software. There are 2 SPI flash footprints (U11, U13) on the board for compatibility with both standard 8-pin serial flash pinouts. The serial control lines are shared by both footprints, and a chip select 0 ohm jumper resistor (R101) is populated to make U13 the active device. To make U11 the active device remove R101 and populate R110 with a 0 ohm resistor.

There is also a jumper (J105) to select Program or Normal (Run) operation of the SPI flash devices. In program mode the CDB USB MASTER card will use the  $\overline{\text{DSP\_CS}}$  line to control the flash while holding the DSP in reset with the  $\overline{\text{DSP\_RST}}$  line. For program mode jumper pins 2 and 3 on J105. In normal the DSP controls the SPI device. In I<sup>2</sup>C mode no jumper change is required for program or normal mode of EEPROM. For normal mode jumper pins 1 and 2. The feature to program flash from the CDB USB MASTER is not yet supported.

### 3.1.11 Audio Clocking

Clocking architecture is one of the most important aspects of a digital audio system. The input and output clock domains of the DSP must be synchronous when delivering audio data in an isochronous fashion (constant bitrate delivery), even if the input/output domains operate at different frequencies (e.g. 48 kHz input/96 kHz output). The CDB48500 can operate in three different clocking modes. Each of these modes is explained in the following sections.

### 3.1.11.1 Clock and Data Flow for up to 8 Channel ADC inputs

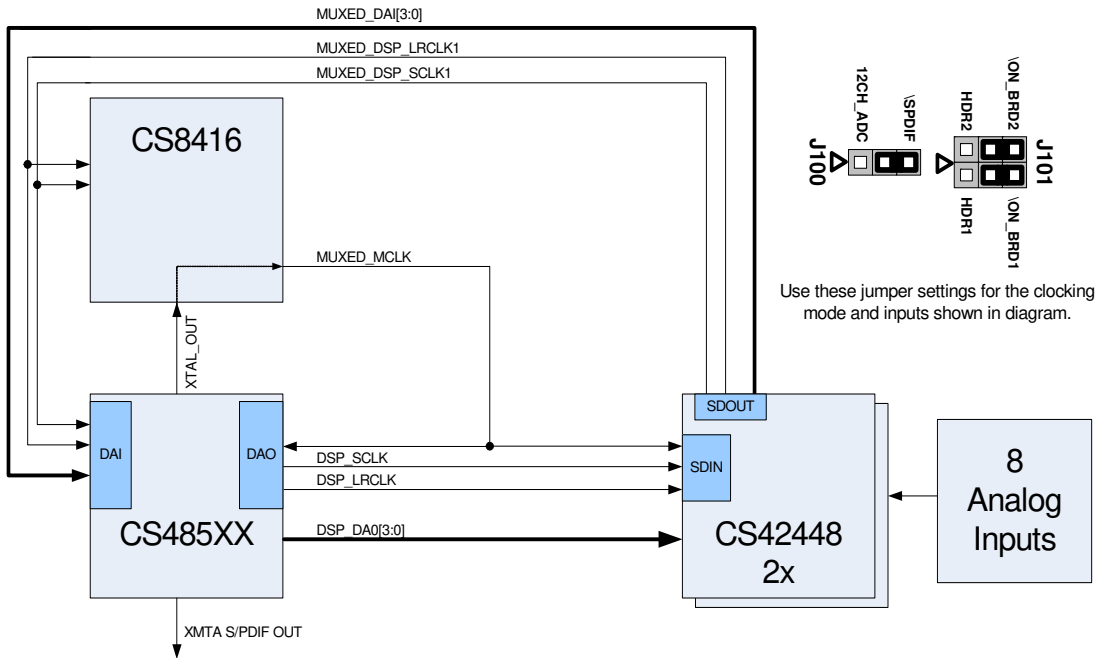


Figure 3-2. Simplified Clock and Data Flow for up to 8 Channel ADC Inputs

The ADC clocking architecture is used when the ADCs are used as the only audio input (i.e. S/PDIF is disabled as described in [Section 4.2.2, “Changing the Audio Input Source” on page 4-3](#)), and the audio input source multiplexer (U1, U2) is used to select on-board audio sources. [Figure 3-2](#) illustrates this clocking configuration. The jumpers must be set as described above.

XTAL\_OUT from the CS485xx is MCLK for the system. The CS8416 slaves to this MCLK and generates SCLK and LRCLK for the ADC side of the CS42448 and the DAI side of the DSP.

On the output side, the CS485xx slaves to MCLK from CS8416 and masters SCLK and LRCLK for the DAC side of the CS42448.

An example of this clocking scheme can be found in pcm\_mc\_1fs.cpa.

### 3.1.11.2 Clock and Data Flow for S/PDIF Input

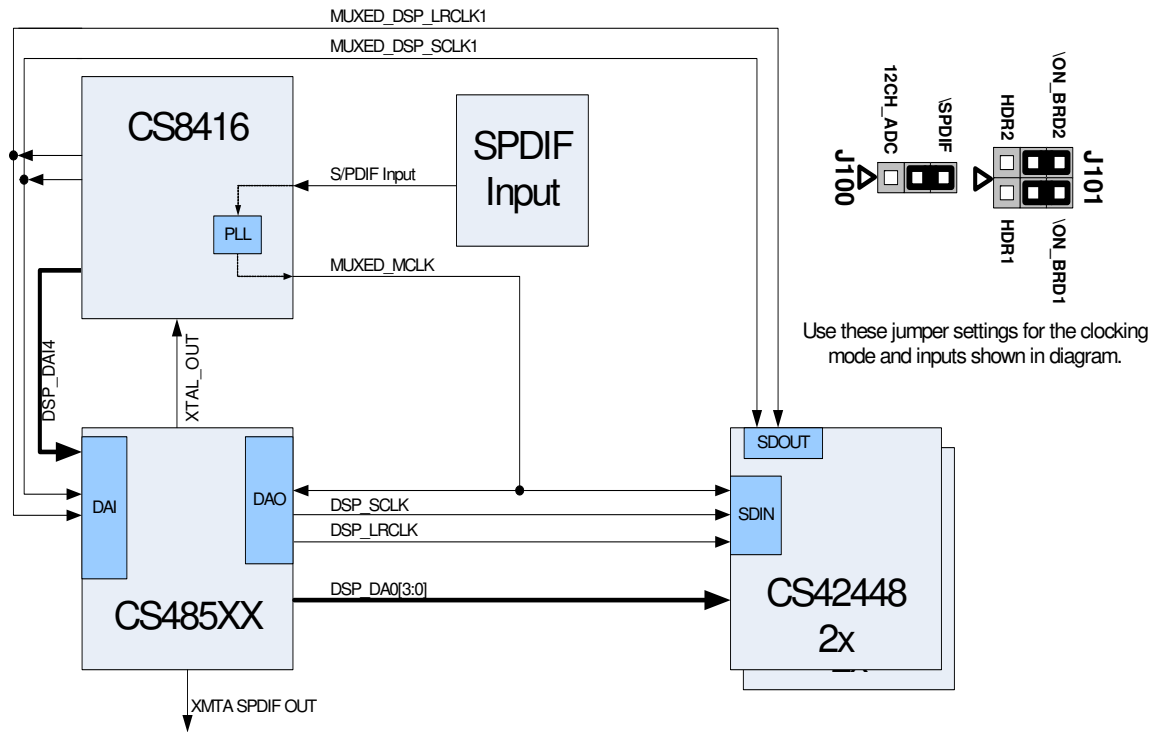


Figure 3-3. Simplified Clock and Data Flow for S/PDIF Input

Figure 3-3 illustrates the S/PDIF clocking architecture used when any S/PDIF RX is used as an audio source, as described in Section 4.2.2, “Changing the Audio Input Source” on page 4-3). MCLK recovered from the incoming S/PDIF stream is the MCLK for the system. The CS8416 also generates SCLK and LRCLK for the DAI side of the DSP from the recovered MCLK.

On the output side, the CS485XX slaves to MCLK from CS8416 and masters SCLK and LRCLK for the DAC side of the CS42448.

An example of this clocking scheme can be found in pcm.cpa.

### 3.1.11.3 Clock and Data Flow for CDB USB Master Card Source

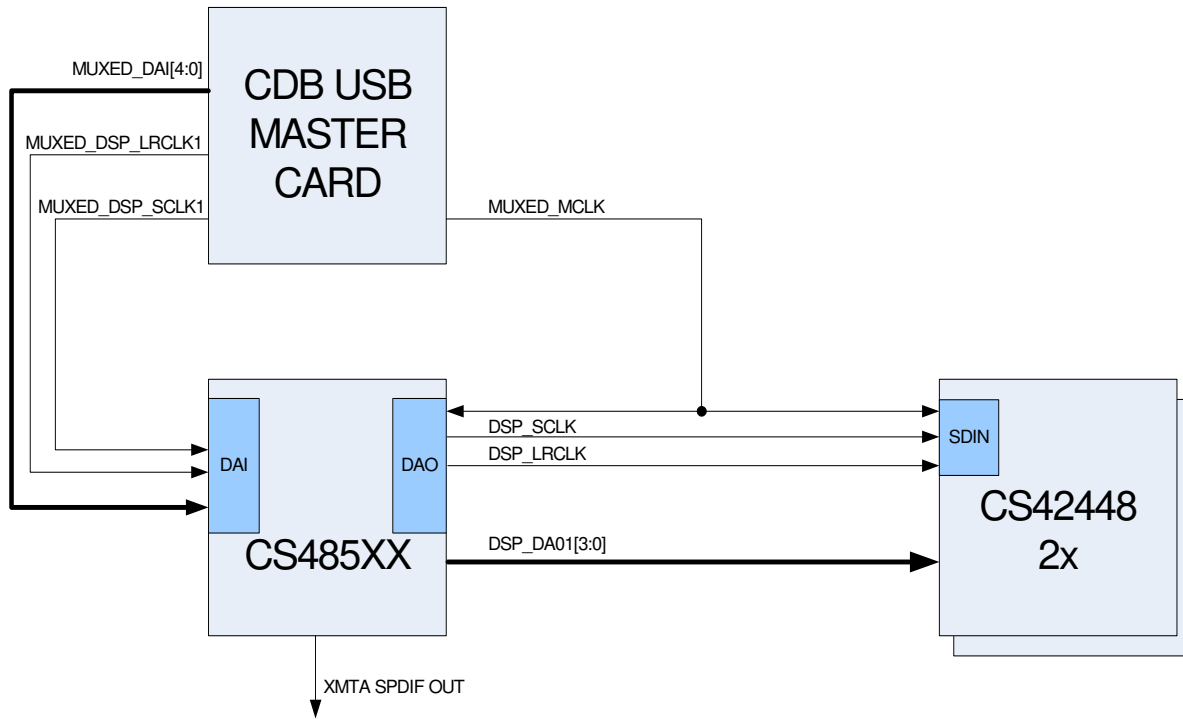


Figure 3-4. CDB USB Master Card Clocking and Data Flow

Figure 3-4 illustrates the clocking architecture used when IIS(USB) is used as an audio source, as described in Section 4.2.2, “Changing the Audio Input Source” on page 4-3). MCLK is generated by the PLL on the USB Master card. The PLD on the USB Master Card generates SCLK and LRCLK for the DAI side of the DSP from the MCLK.

On the output side, the CS485xx slaves to MCLK from the USB Master Card and masters SCLK and LRCLK for the DAC side of the CS42448. The CS485XX always masters its output clocks (DSP\_SCLK/DSP\_LRCLK).

§§



## 4.1 Introduction

The DSP Composer™ software is a graphical user interface (GUI) that is used to program the CS485XX DSP, and to configure the CDB48500. With the exception of the power selection and DAI input jumpers, the CDB48500 is configured exclusively through software. This section provides basic instruction for using the GUI to control the CDB48500, but detailed information can be found in the DSP Composer™ User's Manual. Both the DSP Composer™ software, and the User's Manual for the software package will be provided by your local Cirrus Logic representative.

## 4.2 Basic Application Download and System Configuration for PCM Pass-through

Follow the instructions in [Chapter 1, "Board Setup and Installing the Evaluation Kit Software"](#) in order to install the USB drivers on your PC and launch DSP Composer (the GUI used to control the CDB48500).

After following the instructions in [Section 2.1.4, "Running a Stereo PCM Application on CDB48500-USB"](#) on [page 1-5](#), the DSP Composer main window will appear as shown in [Fig. 4-1](#).

[Fig. 4-1](#) shows the DSP Composer™ main window for a PCM pass-through application on the CDB48500. The blocks shown in the main window of DSP Composer™ can be selected from the folders in the left-hand window pane, and then connected together by "wires" to indicate the processing path as shown.

The "Audio In" and "Audio Out" blocks represent the hardware ports that need to be configured. The "Audio In" block is used to select the S/PDIF Input, Analog input or USB input that is to be processed. It configures the digital audio format for the CS8416, ADC side of CS42448 and the DAI port of the CS485XX. The "Audio Out" block is used to configure the digital audio format for the DAC side of the CS42448, the DAO port of the CS485XX and enables or disables the S/PDIF TX output port of the CS485XX.

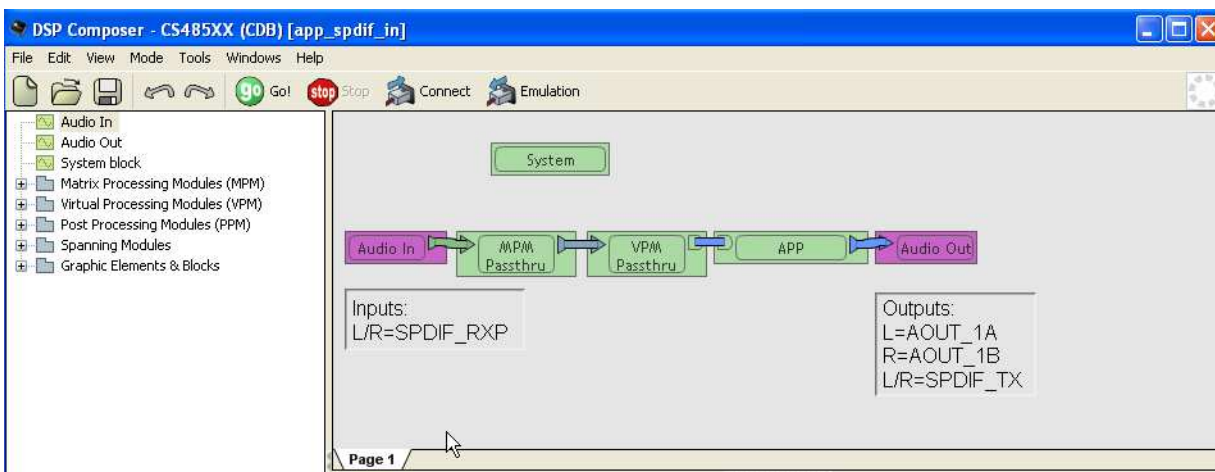


Figure 4-1. PCM Pass-through Example Application

## 4.2.1 System Block

The CDB48500 board is populated with a CS48560. However it is possible to evaluate the CS48520, CS48540, CS48560, CS485AU2B, and CS485DV2B on this board. When you drag the system block on to the work space, a popup menu is displayed as shown in [Fig. 4-2](#). This menu lets you choose the target chip that you need to evaluate. When you select the target chip, place the template of the target chip on the analog connectors. The template is a guide that shows which input/output channels are valid for the selected chip.

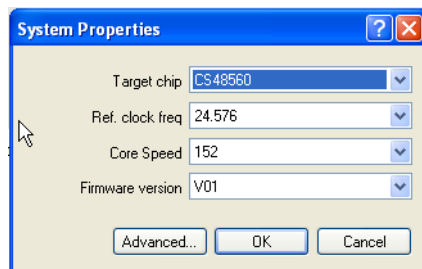


Figure 4-2. System Configuration

## 4.2.2 Changing the Audio Input Source

The audio input to the DSP is selected through the “Audio In” block in DSP Composer. The Audio can be delivered to the DSP via the following:

- S/PDIF (J100 on S/PDIF)
- Analog (J100 on 12CH\_ADC)
- Analog (J100 on 8CH\_ADC)
- Analog (J100 on 2CH\_ADC)
- USB (IIS)
- Echo Audio

### 4.2.2.1 Audio In via S/PDIF

To deliver data to the DSP via S/PDIF, drag the Audio In block to the work space and select “SPDIF” as the Input Source. Double click the Audio In block to see the signal flow. Right Click on SPDIF Rx. The device properties of the S/PDIF IN element lets you select if the SPDIF input is on SPDIF\_RXP (Optical In) or on SPDIF\_RXN (Coaxial). The Input FS depends on input stream and must not be changed. The Master/Slave property must always be set to Master to indicate that the S/PDIF transmitter masters MCLK, SCLK and LRCLK as described in [Section 3.1.11.2, “Clock and Data Flow for S/PDIF Input” on page 1-7](#). The Audio In module with S/PDIF In as the input source is shown in [Fig. 4-3](#).

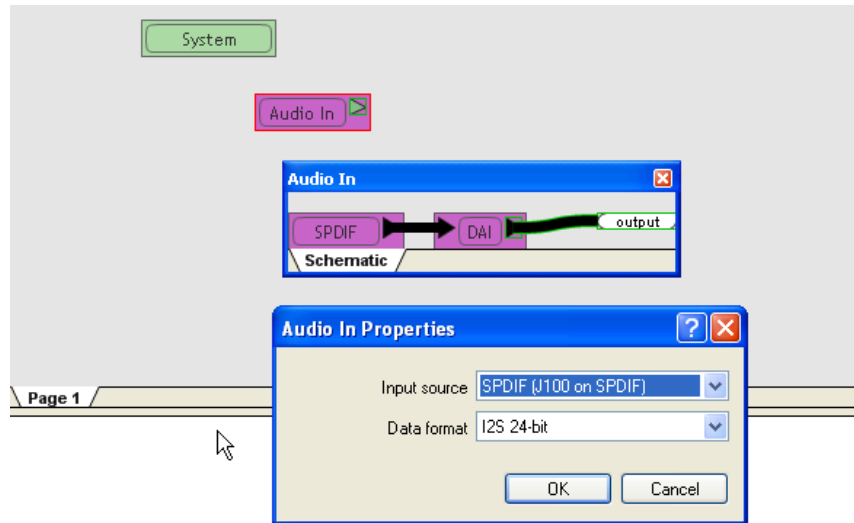


Figure 4-3. Audio In via S/PDIF In

#### 4.2.2.2 Audio In via 8-channel ADC

To deliver data to the DSP via 8ch ADC, drag the Audio In block to the work space and select “Analog (8 ch)” as the Input Source. Double click the Audio In block to see the signal flow. The device properties of the Analog (8 ch) element lets you select if the sampling frequency of the ADC on the CS42448 CODEC. The Master/Slave property must always be set to Master to indicate that the ADC will master SCLK and LRCLK as described in [Section 3.1.11.1, “Clock and Data Flow for up to 8 Channel ADC inputs” on page 1-6](#). The Audio In module with Analog (8-channel) as the input source is shown in [Fig. 4-4](#).

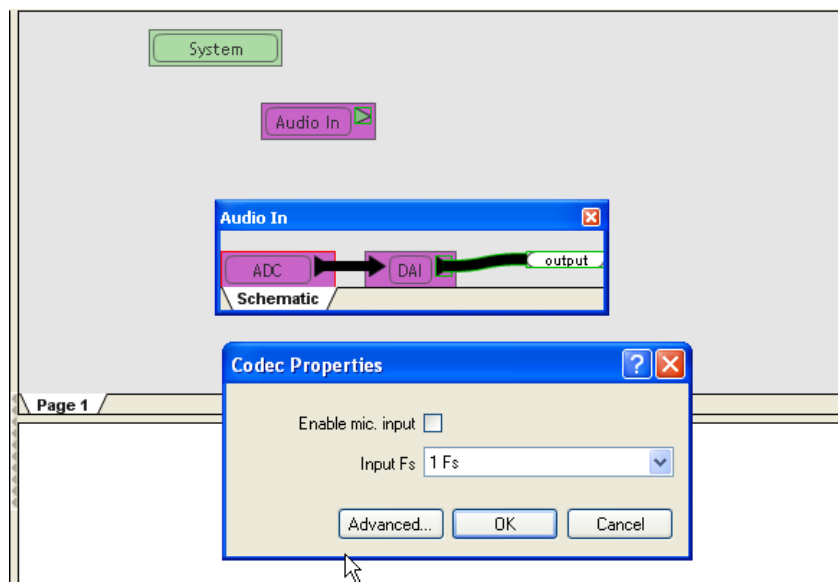


Figure 4-4. Audio In via 8 Channel ADC

#### 4.2.2.3 Audio In via USB

This feature is currently not supported.