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CDB5340

Evaluation Board for CS5340

Features

- Demonstrates recommended layout and grounding arrangements
- CS8406 generates S/PDIF, and EIAJ-340 compatible digital audio
- Requires only an analog signal source and power supplies for a complete Analog-to-Digital-Converter system

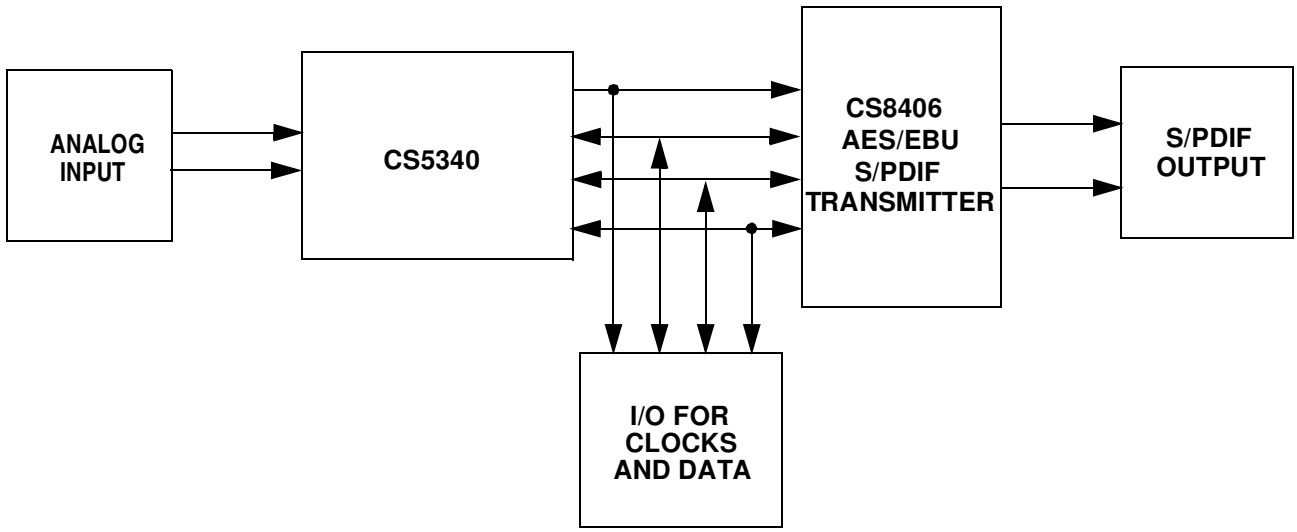
Description

The CDB5340 evaluation board is an excellent means for quickly evaluating the CS5340 24-bit, stereo A/D converter. Evaluation requires a digital signal analyzer, an analog signal source, and a power supply.

Also included is a CS8406 digital audio interface transmitter which generates S/PDIF, and EIAJ-340 compatible audio data. The digital audio data is available via RCA phono and optical connectors.

ORDERING INFORMATION

CDB5340 Evaluation Board



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Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **www.cirrus.com**

1. CDB5340 SYSTEM OVERVIEW

The CDB5340 evaluation board is an excellent means of quickly evaluating the CS5340. The CS8406 digital audio interface transmitter provides an easy interface to digital audio signal analyzers including the majority of digital audio test equipment.

The CDB5340 schematic has been partitioned into 5 schematics shown in Figure 2 through Figure 6. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

2. CS8406 DIGITAL AUDIO TRANSMITTER

The system generates and encodes standard S/PDIF data using a CS8406 Digital Audio Transmitter (see Figure 5). The outputs of the CS8406 are RS422 compatible differential line drivers. The CS8406 supports both Left Justified and I^2S data formats, as determined by the DIP switch, S2. A description of the CS8406 is included in the CS8406 datasheet.

3. INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the 10-pin header, J11. The schematic for the clock/data input/output is shown in Figure 4.

The CDB5340 allows some flexibility as to the generation of the clocks. When the CS5340 and CS8406 are in slave mode, the SCLK and LRCK must be provided via the header, J11. MCLK can be generated from the on-board oscillator, Y1 or provided via the header, J11 as determined by the DIP switch, S2. The on-board oscillator is socketed to allow other frequency oscillators to be used. Please note that the on-board oscillator must be removed if an external MCLK is provided through header J11.

4. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by four binding posts (VA/VD, VL, GND, +5V), see Figure 6. The VA/VD input supplies the VA and VD pins of the CS5340. VL supplies power to the VL pin of the CS5340 and to the level shifter circuits. The +5V input supplies power to the digital circuitry and the input amplifiers.

5. GROUNDING AND POWER SUPPLY DECOUPLING

The CS5340 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 3 details the power distribution used on this board. The decoupling capacitors are located as close to the CS5340 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

6. ANALOG INPUT FILTER

The CDB5340 implements a single-ended analog input buffer, as shown in Figure 2. Note that there is no attenuation or gain associated with the input buffer.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
VA/VD	Input	+3.3V to +5V power for the CS5340
VL	Input	+2.5V to +5V power for the CS5340
GND	Input	Ground connection from power supply
+5V	Input	+ 5 Volt power
AINL	Input	Analog input left channel
AINR	Input	Analog input right channel
Optical Output	Output	Digital audio output
Coax Output	Output	Digital audio output

Table 1. System Connections

JUMPER/SWITCH	PURPOSE	POSITION		FUNCTION SELECTED
J5	VA/VD Power Source	ADJ *+3.3V +5V		Power from the Binding Post (J1) Power from the +3.3V Regulator Power from the +5V Supply
J6	VL Power Source	ADJ *+3.3V +5V		Power from the Binding Post (J2) Power from the +3.3V Regulator Power from the +5V Supply
J11	Input/Output for clocks/data	-		-
S1	Reset for the CDB5340	-		-
S2	CDB5340 Configuration	M1/M0	Open *Closed	Hi Low
		SCLK/LRCK	Open *Closed	Header J11 is an input for clocks. Header J11 is an output for clocks.
		MCLK	Open *Closed	Header J11 is an input for MCLK. Header J11 is an output for MCLK.
		8406	Open *Closed	CS8406 in Master mode CS8406 in Slave mode
		DIF	Open *Closed	Digital interface format set to I^2S Digital interface format set to Left Justified

Table 2. CDB5340 Jumper and Switch Settings

* denotes default factory settings

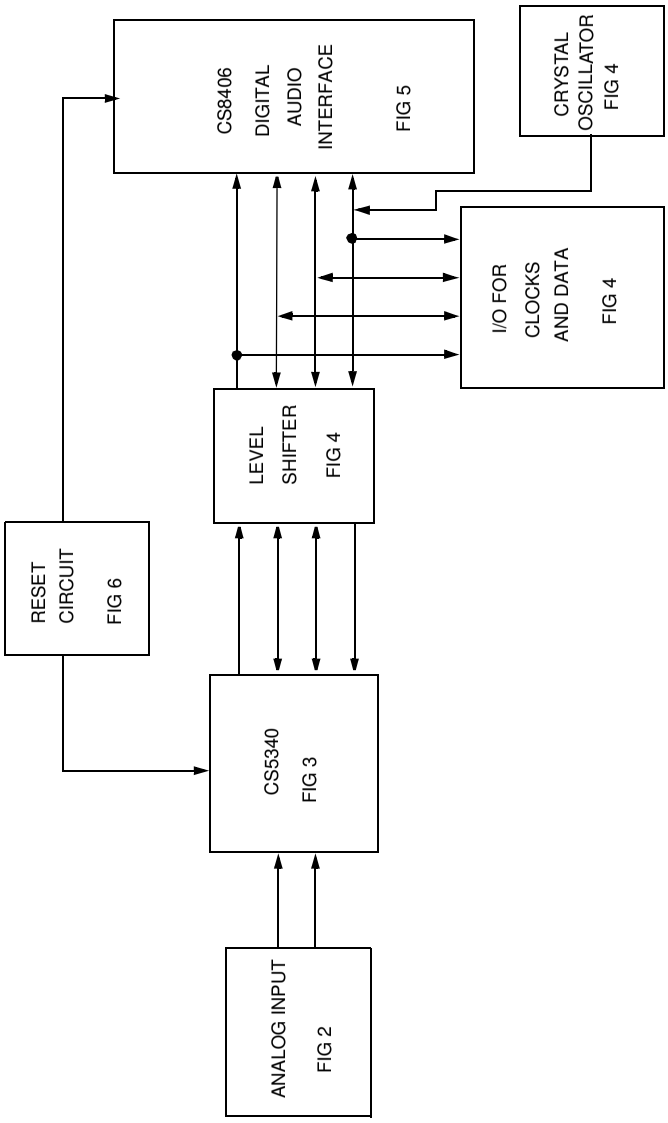


Figure 1. System Block Diagram and Signal Flow

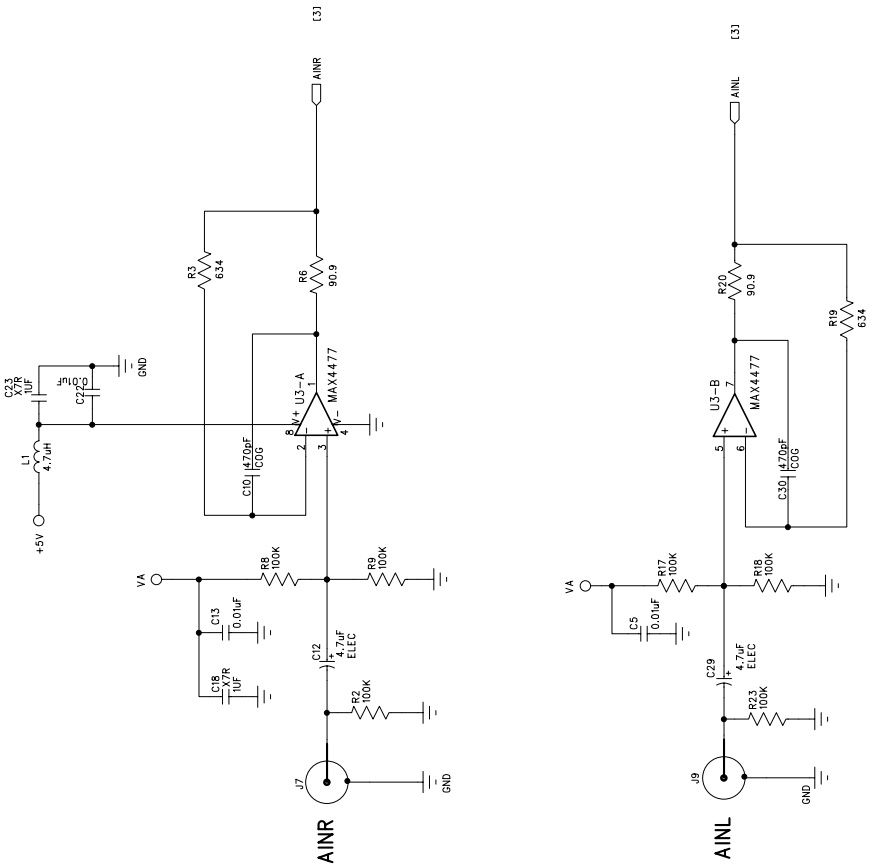
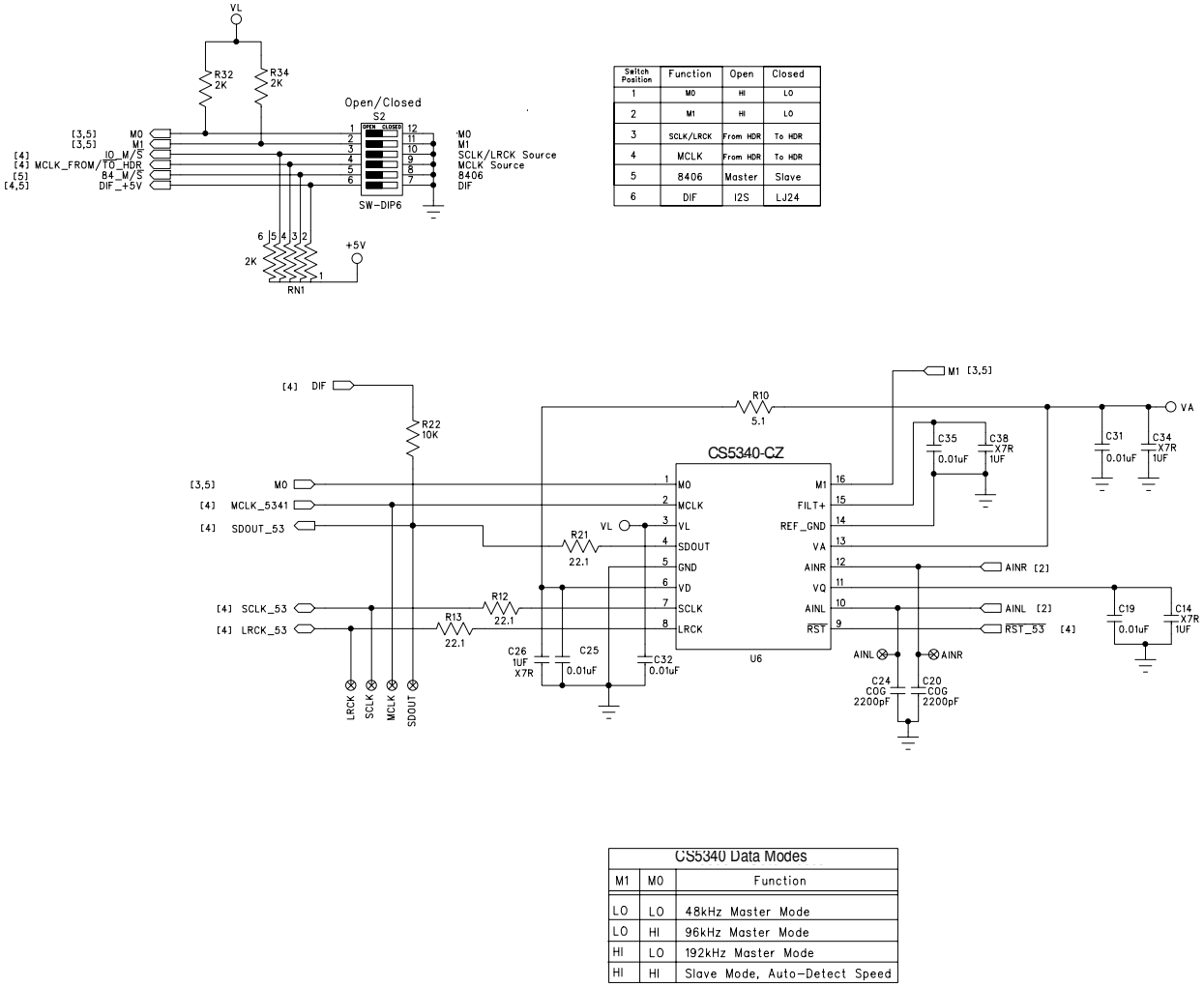


Figure 2. Analog Audio Input



Switch Position	Function	Open	Closed
1	M0	HI	LO
2	M1	HI	LO
3	SCLK/LRCK	From HDR	To HDR
4	MCLK	From HDR	To HDR
5	8406	Master	Slave
6	DIF	I2S	LJ24

CS5340 Data Modes		
M1	M0	Function
LO	LO	48kHz Master Mode
LO	HI	96kHz Master Mode
HI	LO	192kHz Master Mode
HI	HI	Slave Mode, Auto-Detect Speed

Figure 3. CS5340

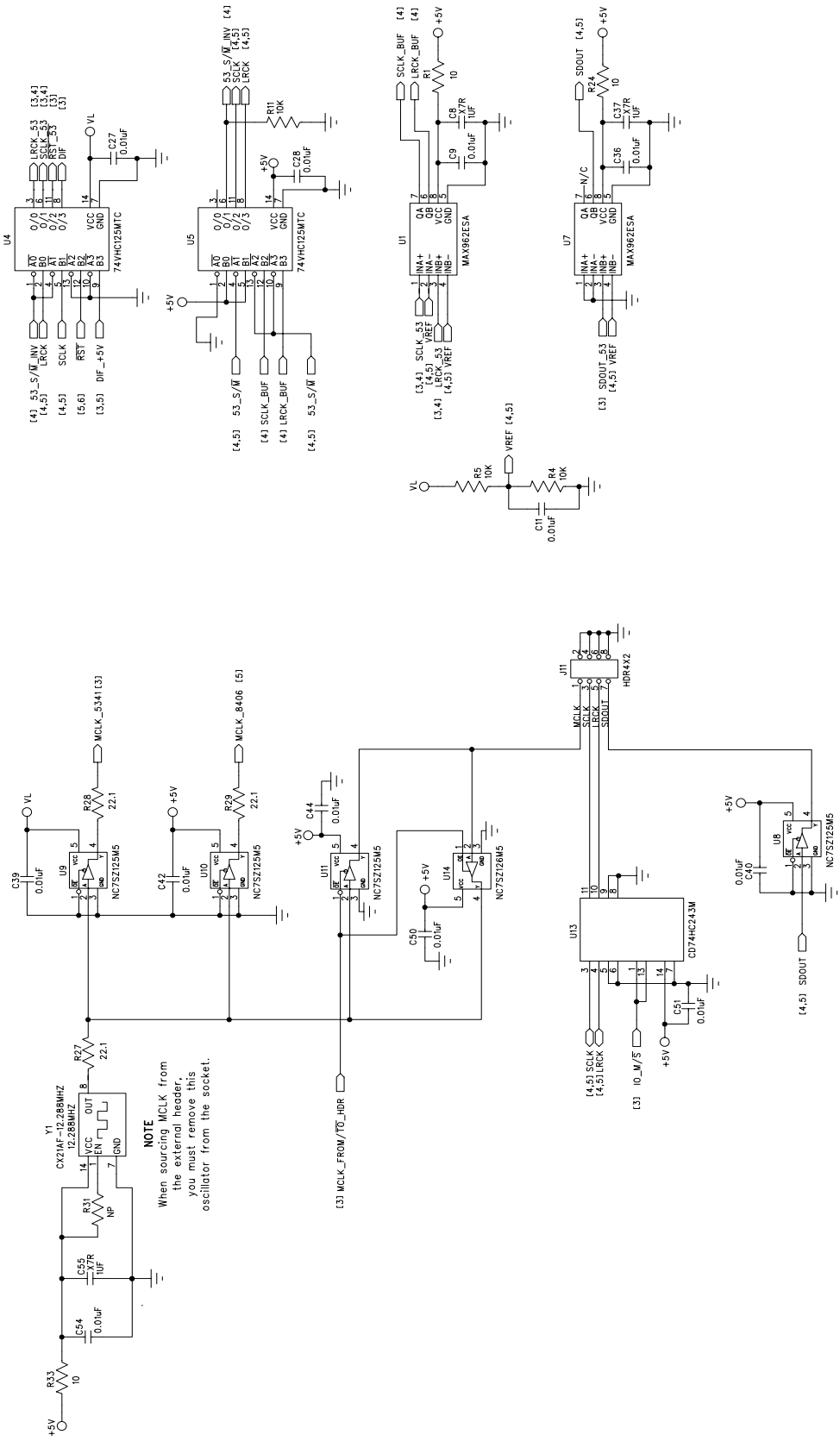


Figure 4. Level Shifters

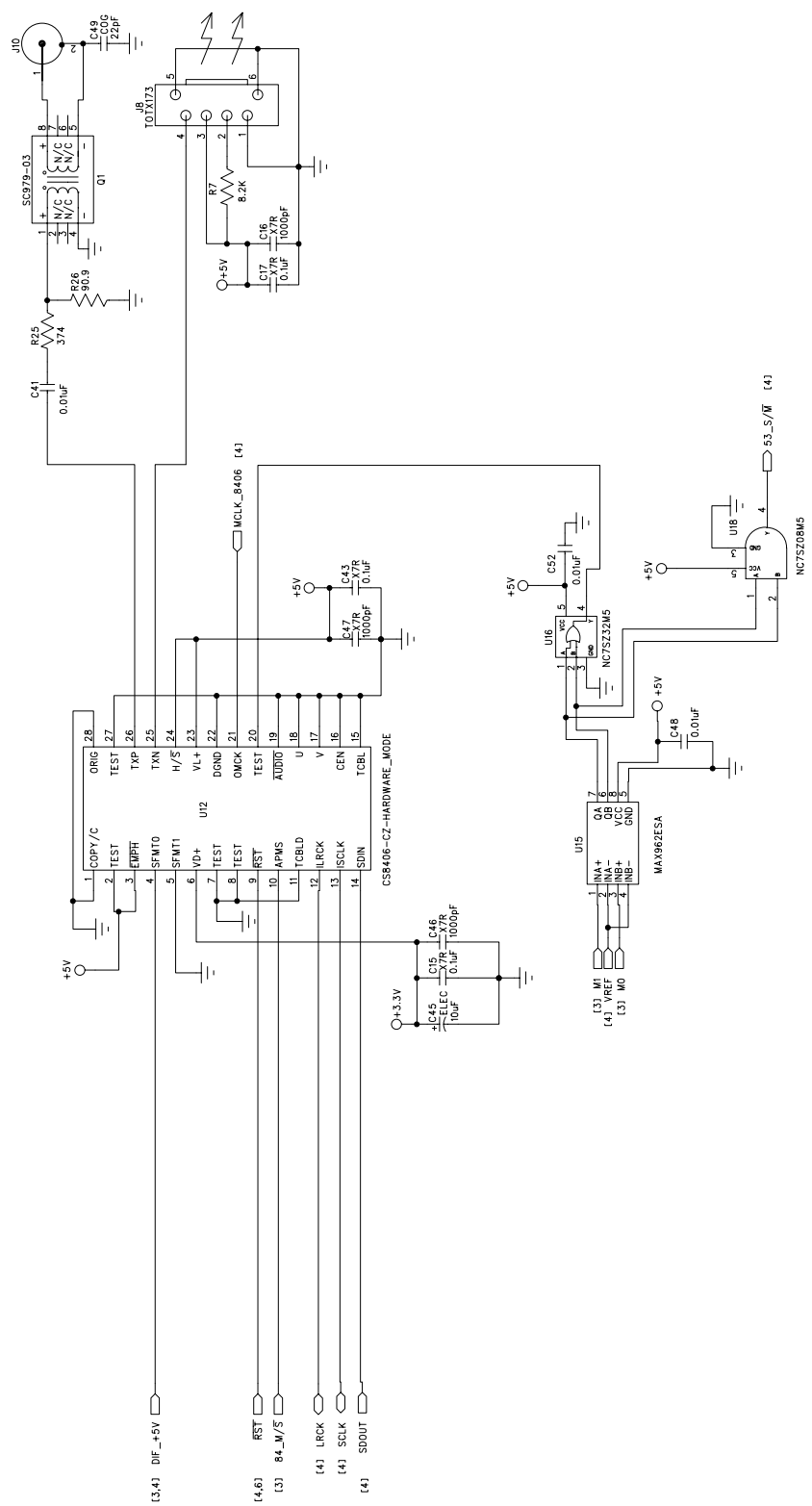


Figure 5. CS8406 Digital Audio Interface

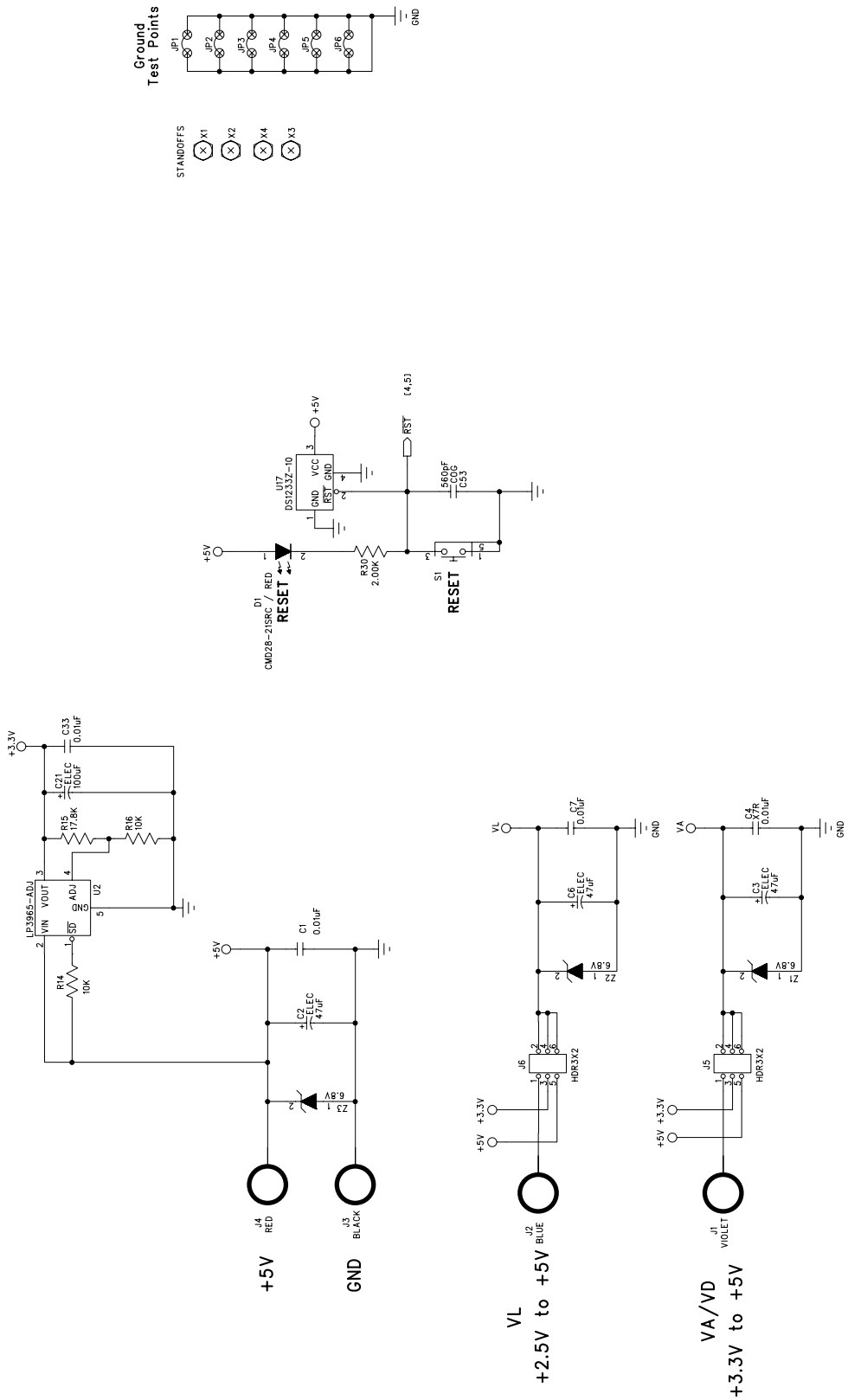
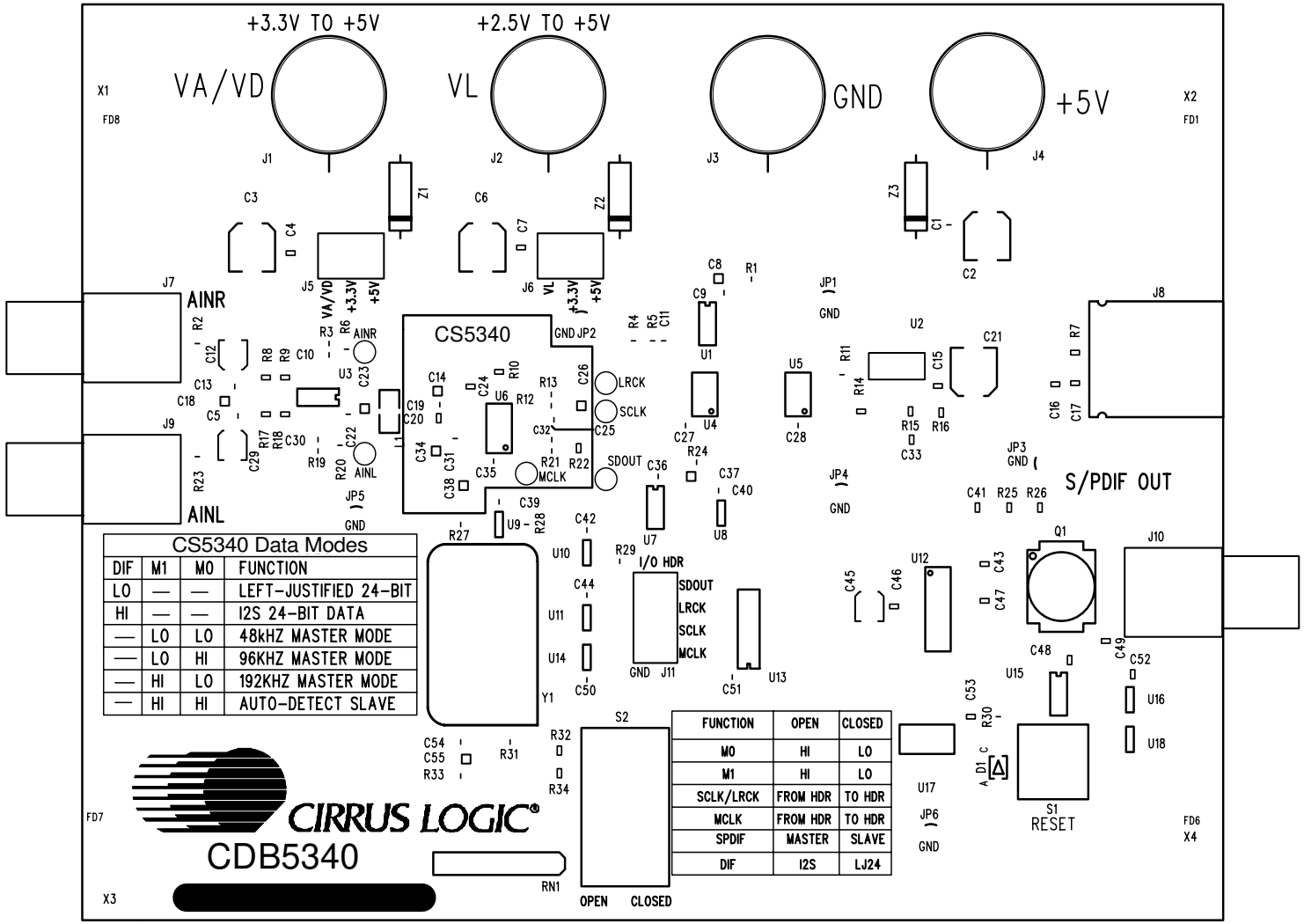


Figure 6. Power Circuit



SILKSCREEN TOP

Figure 7. Top Layer Silkscreen

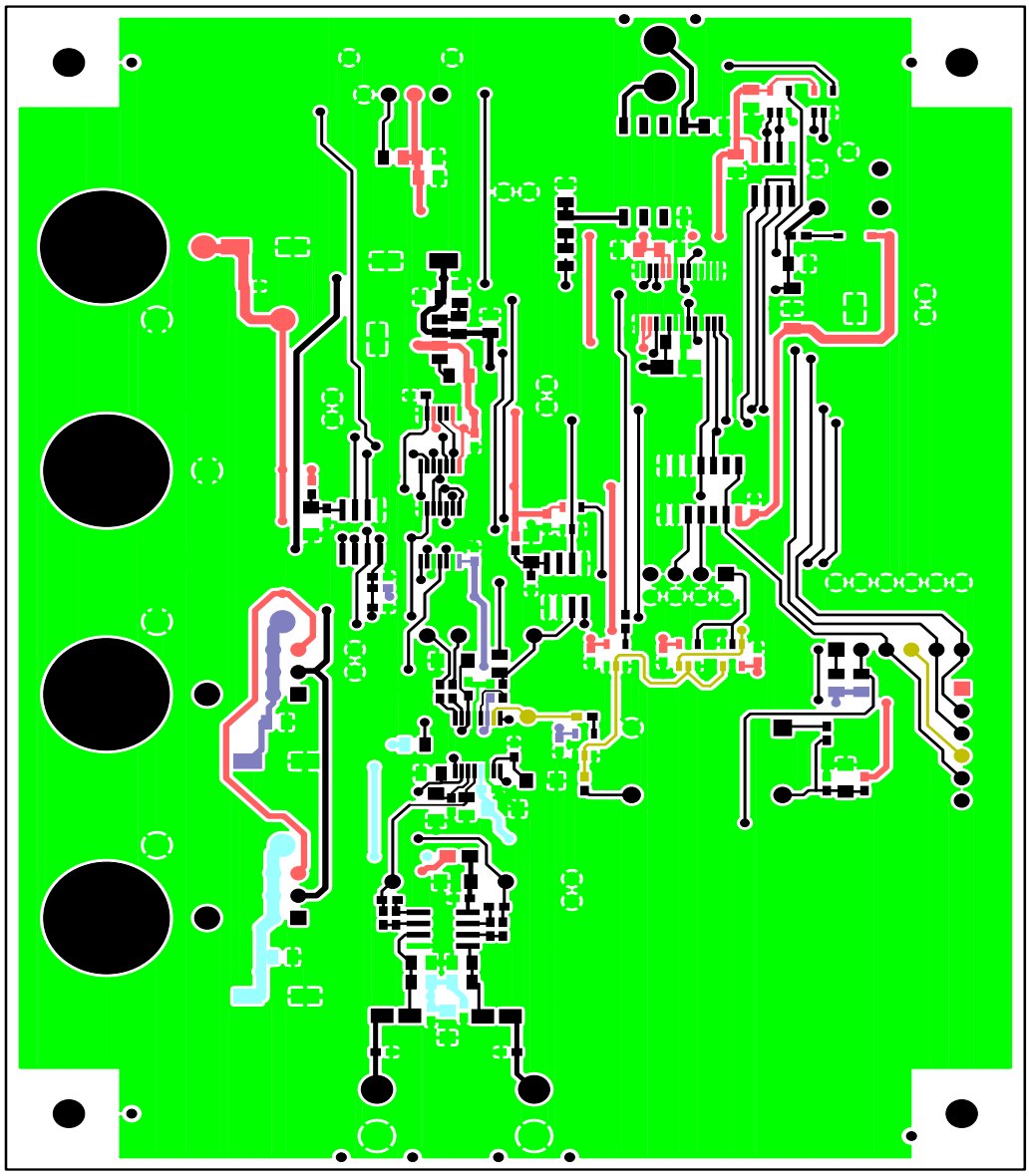


Figure 8. Top Layer

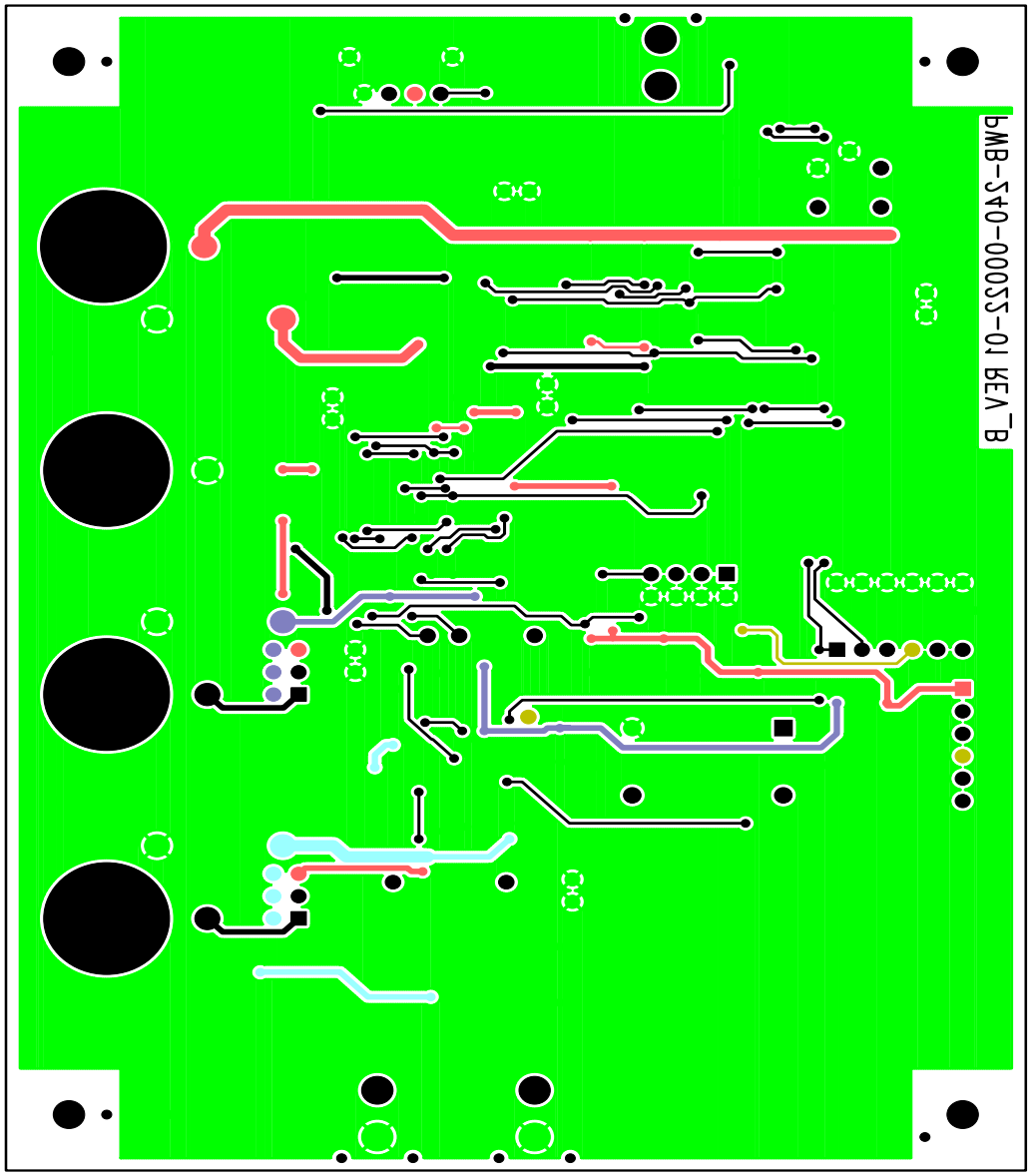


Figure 9. Bottom Layer