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CDB5345

Evaluation Board for CS5345

Features

- Single-ended Analog Inputs
- Single-ended Analog Outputs
- CS8406 S/PDIF Digital Audio Transmitter
- Header for Optional External Software Configuration of CS5345
- Header for External PCM Serial Audio I/O
- 3.3 V Logic Interface
- Pre-defined Software Scripts
- Demonstrates Recommended Layout and Grounding Arrangements
- Windows® Compatible Software Interface to Configure CS5345 and Inter-board Connections

ORDERING INFORMATION

CDB5345 Evaluation Board

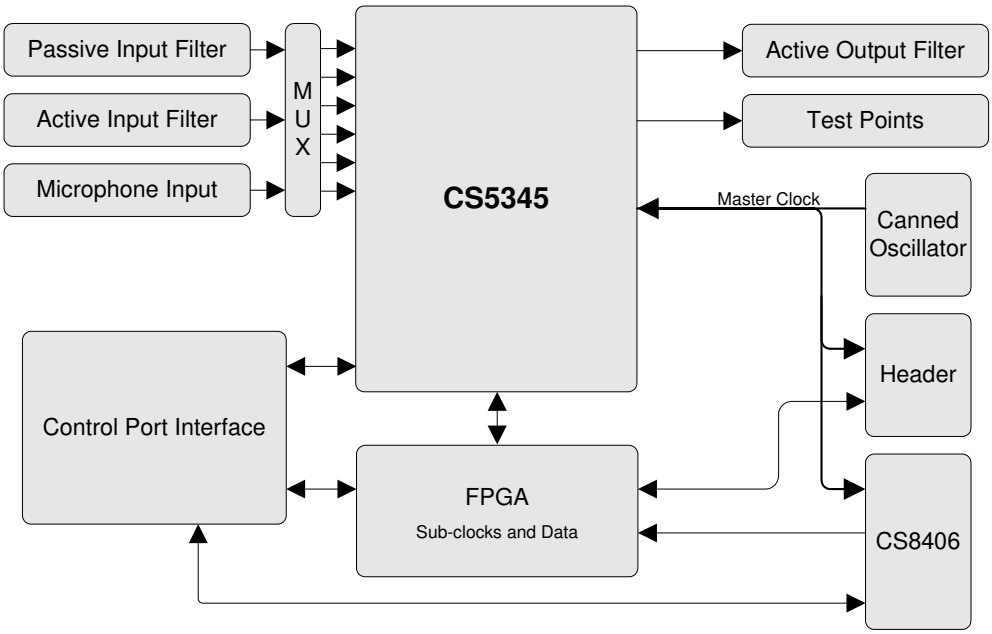
Description

The CDB5345 evaluation board is an excellent means for evaluating the CS5345 ADC. Evaluation requires an analog signal source and analog/digital analyzer, and power supplies. A Windows® PC compatible computer must be used to evaluate the CS5345.

System timing for the I²S, Left-Justified and Right-Justified interface formats can be provided by the CS5345, the CS8406, or by a PCM I/O stake header with an external source connected.

RCA phono jacks are provided for the CS5345 analog inputs and outputs. Digital data input is available via RCA phono or optical connectors to the CS8406.

The Windows® software provides a GUI to make configuration of the CDB5345 easy. The software communicates through the PC's serial port to configure the control port registers so that all features of the CS5345 can be evaluated. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.



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1. SYSTEM OVERVIEW

The CDB5345 evaluation board is an excellent means for evaluating the CS5345 ADC. Analog and digital audio signal interfaces are provided, an on-board FPGA is used for easily configuring the evaluation platform, and a 9-pin serial cable is included for use with the supplied Windows® configuration software.

The CDB5345 schematic set is shown in Figures 4 through 11. The CDB5345 is assembled on the printed wire board designed for the CDB4245, with a number of components un-populated. These un-populated components have been removed from the included schematic set for clarity. For a complete schematic set, see the CDB4245 data sheet.

1.1 Power

Power must be supplied to the evaluation board through the red +5.0 V binding post. On-board regulators provide 3.3 V, 2.5 V, and 1.8 V supplies. Appropriate supply levels for powering VA, VD, VLS, and VLC are set by a series of jumpers (see Table 5 on page 14). All voltage inputs must be referenced to the single black binding post ground connector (see Table 4 on page 13).

WARNING: Please refer to the CS5345 data sheet for allowable voltage levels.

1.2 Grounding and Power Supply Decoupling

The CS5345 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 3 on page 15 provides an overview of the connections to the CS5345. Figure 12 on page 24 shows the component placement. Figure 13 on page 25 shows the top layout. Figure 14 on page 26 shows the bottom layout. The decoupling capacitors are located as close to the CS5345 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

1.3 CS5345 Audio ADC

A complete description of the CS5345 is included in the CS5345 product data sheet.

The required configuration settings of the CS5345 are made in its control port registers, accessible through the CS5345 tab of the Cirrus Logic FlexGUI software.

Clock and data source selections are made through the control port of the FPGA. Basic routing selections can be made using the CS5345 Controls tab in the GUI software application. Advanced options are accessible through the Board Configuration sub-tab on the Register Maps tab of the Cirrus Logic FlexGUI software. Refer to the FPGA register descriptions sections beginning on page 11.

1.4 CS8406 Digital Audio Transmitter

A complete description of the CS8406 transmitter (Figure 7 on page 19) and a discussion of the digital audio interface are included in the CS8406 data sheet.

The CS8406 converts the PCM data generated by the CS5345 to the standard S/PDIF data stream. The CS8406 can operate in either master or slave mode, accepts 128 Fs, 256 Fs, 384 Fs, and 512 Fs master clocks on the OMCK input pin, and can operate in the Left-Justified, I²S, Right-Justified 16-bit, and Right-Justified 24-bit interface formats.

The most common operations of the CS8406 may be controlled via the CDB5345 Controls tab in the GUI software application. Advanced options are accessible through the CS8406 sub-tab on the Register Maps tab of the Cirrus Logic FlexGUI software.

1.5 FPGA

The FPGA handles both clock and data routing on the CDB5345. Clock and data routing selections made via the CDB5345 Controls tab in the GUI will be handled by the FPGA with no user intervention required. For advanced information regarding the internal registers and operation of the FPGA, see sections 4 and 5 beginning on page 10.

1.6 Canned Oscillator

A canned oscillator, Y1, is available to provide a master clock source to the CDB5345.

The oscillator is mounted in pin sockets, allowing easy removal or replacement. The board is shipped with a 12.2880 MHz crystal oscillator populated.

1.7 External Control Headers

The evaluation board has been designed to allow interfacing with external systems via the headers J10, and J17.

The 8-pin, 2 row header, J10, provides access to the serial audio signals required to interface to the serial audio port of the CS5345 with a DSP (see Figure 10 on page 22).

The direction of the signals on header J10 can be configured using the controls located within the Board Controls group box on the CDB5345 Controls tab in the provided GUI software.

The 15-pin, 3 row header, J17, allows the user bidirectional access to the SPI/I^2C control signals by simply removing all the shunt jumpers from the “PC” position. The user may then choose to connect a ribbon cable to the “EXTERNAL CONTROL” position. A single “GND” row for the ribbon cable’s ground connection is provided to maintain signal integrity. Two unpopulated pull-up resistors are also available should the user choose to use the CDB for the I^2C power rail.

1.8 Analog Inputs

RCA connectors supply the CS5345 analog inputs through single-ended, unity gain, active or passive circuits. Refer to the CS5345 data sheet for the ADC full-scale level.

A 4-pin CD-ROM type header is provided for easily connecting the analog outputs from a CD-ROM drive to the analog inputs of the CS5345.

1.9 Analog Outputs

The CS5345 PGA analog outputs are routed through a two-pole active filter. The output of the filter is connected to RCA jacks for easy evaluation.

1.10 Serial Control Port

A graphical user interface is included with the CDB5345 to allow easy manipulation of the registers in the CS5345, CS8406, and FPGA. See the device-specific data sheets for the CS5345 and CD8406 internal register descriptions. The internal register map for the FPGA is located in section 4 on page 10.

Connecting a cable to the RS-232 connector (J42) and launching the Cirrus Logic FlexGUI software (FlexLoader.exe) will enable the CDB5345.

Refer to “PC Software Control” on page 7 for a description of the Graphical User Interface (GUI).

1.11 USB Control Port

The USB control port connector (J37) is currently unavailable.

2. SYSTEM CLOCKS AND DATA

The CDB5345 implements comprehensive clock routing capabilities. Configuration of the clock routing can be easily achieved using the controls within the Board Controls group box on the CDB5345 Controls tab in the GUI software application.

2.1 Clock Routing

The master clock signal (MCLK) may be sourced from the canned oscillator (Y1) or the PCM1 I/O header (J10)

The sub-clock signals (SCLK and LRCK) may be sourced from the CS5345 in master mode, the CS8406 in master mode, or the PCM1 I/O header.

Clock routing configuration is achieved using the MCLK Source and Subclock Source controls within the Board Controls group box on the CDB5345 Controls tab in the GUI software application.

2.2 Data Routing

The serial data output of the CS5345 is routed to both the CS8406 S/PDIF transmitter and the PCM1 I/O header. No user configuration of the serial data routing is required.

3. PC SOFTWARE CONTROL

The CDB5345 is shipped with a Microsoft Windows® based graphical user interface which allows control over the CS5345, CS8406, and FPGA. The board control software communicates with the CDB5345 over the RS-232 interface using the PC's COM1 port.

To use the board control software, the contents of the included CD-ROM should first be copied to a directory on the PC's local disk. If applied, the Read Only attribute should be removed from all files. Once the appropriate cable has been connected between the CDB5345 and the host PC, load FlexLoader.exe from the Software directory. When the software loads, all devices will be reset to their default reset state.

The GUI's File menu provides the ability to save and load script files containing all of the register settings. Pre-configured script files are provided for basic functionality. Refer to "Pre-Configured Script Files" on page 8 for details.

3.1 CDB5345 Controls Tab

The CDB5345 Controls tab provides a high-level intuitive interface to many of the configuration options of the CS5345 and CDB5345. The controls within the ADC/PGA Controls group box control the internal registers of the CS5345. The controls within the Board Controls group box control the board level clock and data routing on the CDB5345.

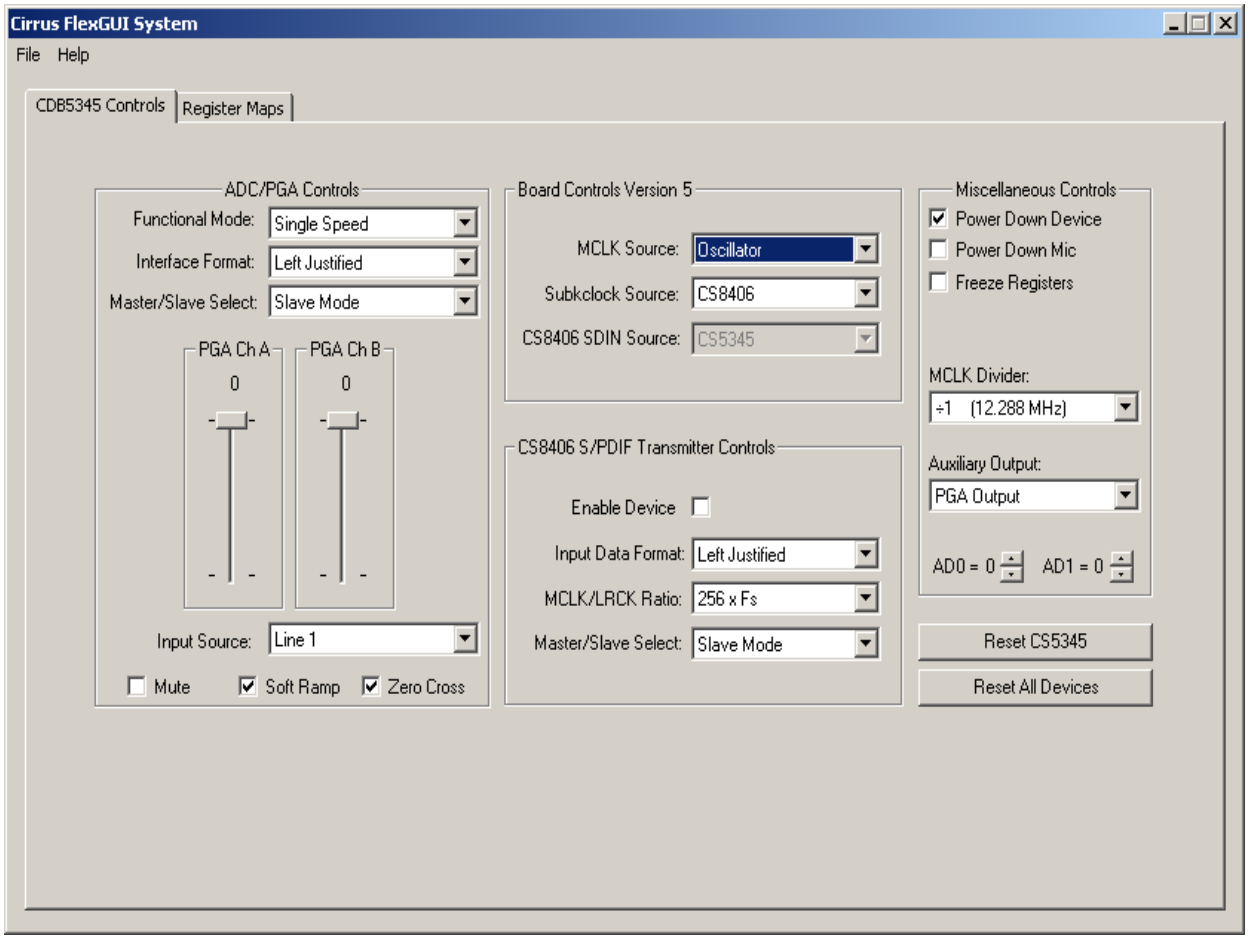

Figure 1. CDB5345 Controls Tab

3.2 Register Maps Tab

The Register Maps tab provides low level control over the register level settings of the CS5345, CS8406, and FPGA. Each device is displayed on a separate tab. Register values can be modified bit-wise or byte-wise. For bit-wise, click the appropriate push button for the desired bit. For byte-wise, the desired hex value can be typed directly in the register address box in the register map.

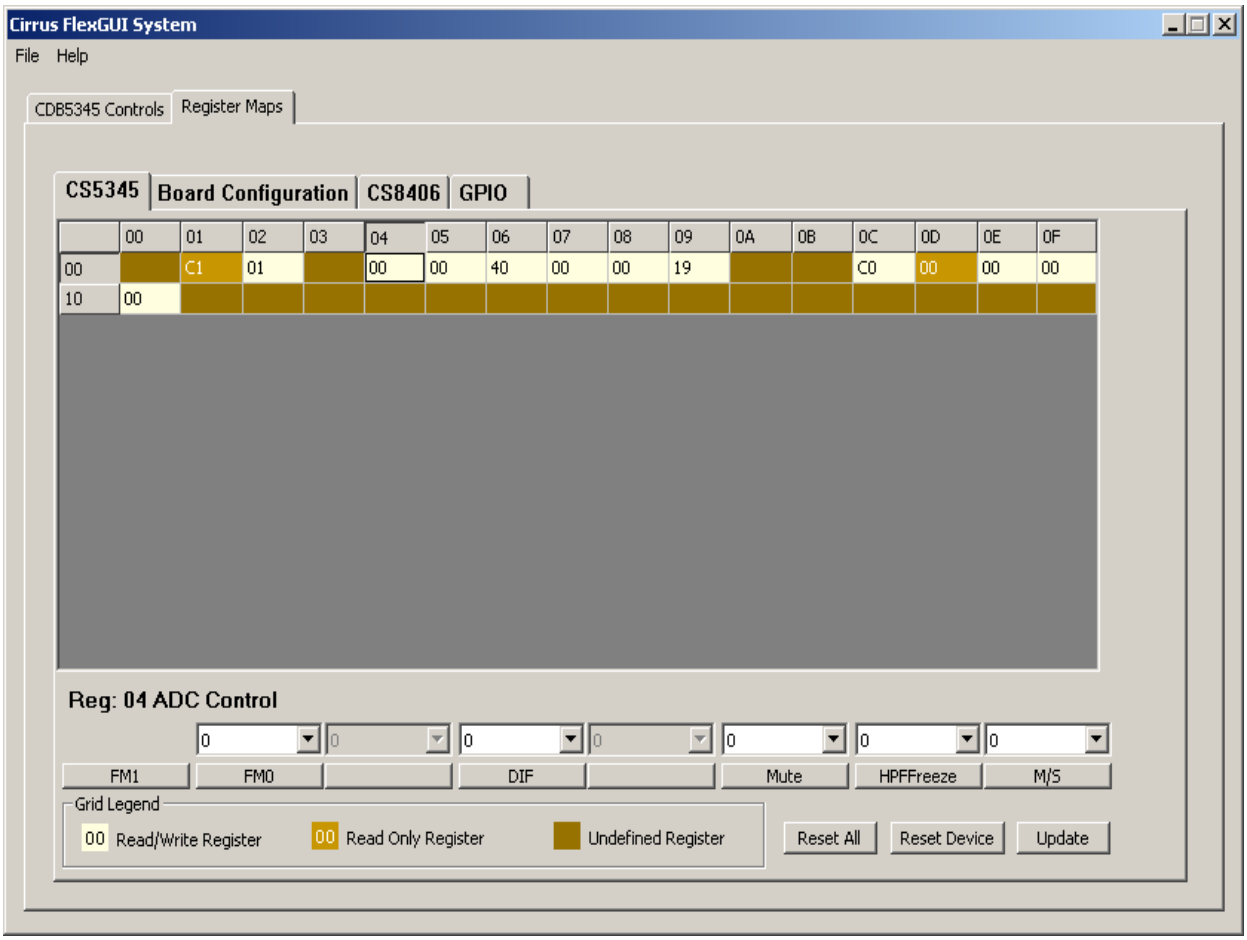

Figure 2. Register Maps Tab

3.3 Pre-Configured Script Files

Pre-configured script files are provided with the CDB5345 to allow easy initial board bring-up. The board configurations stored within these files are described in sections 3.3.1 - 3.3.2.

3.3.1 Oscillator Clock - ADC Ch 1 In to In to SPDIF & PGA Out

Using the pre-configured script file named “Oscillator Clock - ADC Ch 1 In to SPDIF & PGA Out.txt”, an analog input signal applied to channel 1 of the CS5345 input multiplexer will be digitized by the ADC, transmitted in S/PDIF format by the CS8406, and will be output through the active output filter and RCA jacks.

The canned oscillator is the source of MCLK. The CS5345 is the sub-clock master to the CS8406 and the PCM1I/O header.

3.3.2 Oscillator Clock - ADC Ch 2 In to In to SPDIF Out

Using the pre-configured script file named “Oscillator Clock - ADC Ch 2 In to SPDIF Out.txt”, an analog input signal applied to channel 2 of the CS5345 input multiplexer will be digitized by the ADC and transmitted in S/PDIF format by the CS8406. No signal will be output through the active output filter and RCA jacks.

The canned oscillator is the source of MCLK. The CS5345 is the sub-clock master to the CS8406 and the PCM1I/O header.

4. FPGA REGISTER QUICK REFERENCE

This table shows the register names and their associated default values.

Addr	Function	7	6	5	4	3	2	1	0
01h	Code Rev. ID	Rev7	Rev6	Rev5	Rev4	Rev3	Rev2	Rev1	Rev0
		x	x	x	x	x	x	x	x
02h	MCLK Source	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCLK
		0	0	1	0	0	0	0	0
03h	Subclock Source	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SUBCLK1	SUBCLK0
		0	0	0	1	0	0	0	1
04h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		0	0	0	0	0	0	0	0
05h	Transmitter SDIN Source	Reserved	Reserved	Reserved	CS8406	Reserved	Reserved	Reserved	Reserved
		0	0	0	1	0	0	0	1

5. FPGA REGISTER DESCRIPTION

5.1 CODE REVISION ID - ADDRESS 01H

7	6	5	4	3	2	1	0
Rev7	Rev6	Rev5	Rev4	Rev3	Rev2	Rev1	Rev0

Function:

Identifies the revision of the FPGA code. This register is Read-Only.

5.2 MCLK SOURCE CONTROL - ADDRESS 02H

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCLK

5.2.1 MCLK SOURCE (BIT 0)

Default = 0

Function:

This bit selects the source of the CS5345 MCLK signal. Table 1 shows the available settings.

Table 1. MCLK Source

MCLK	MCLK Source
0	Canned Oscillator
1	M1 position on PCM1 I/O Header

5.3 SUBCLOCK SOURCE CONTROL - ADDRESS 03H

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SUBCLK1	SUBCLK0

5.3.1 SUBCLOCK SOURCE (BITS 1:0)

Default = 01

Function:

This bit selects the source of the CS5345 SCLK and LRCK signals. Table 2 shows the available settings.

Table 2. Subclock Source

SUBCLOCK1	SUBCLOCK	Subclock Source
0	0	- CS5345 is Master - CS8406 is Slave to CS5345 - PCM I/O Header Subclocks are Output from CS5345
0	1	- CS5345 is Slave to CS8406 - CS8406 is Master - PCM I/O Header Subclocks are Output from CS8406
1	0	- CS5345 is Slave to Header - CS8406 is Slave to Header - PCM I/O Header Subclocks are an Input
1	1	Reserved

5.4 TRANSMITTER SDIN SOURCE CONTROL - ADDRESS 05H

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	CS8406	Reserved	Reserved	Reserved	Reserved

5.4.1 CS8406 SDIN SOURCE (BIT 4)

Default = 0

Function:

These bit selects the source of the CS8406 SDIN signal. Table 3 shows the available settings.

Table 3. CS8406 SDIN Source

CS8406	CS8406 SDIN Source
0	Reserved
1	CS5345 SDOUT

6. CDB CONNECTORS, JUMPERS, AND SWITCHES

CONNECTOR	Reference Designator	INPUT/OUTPUT	SIGNAL PRESENT
+5V	J1	Input	+5.0 V Power Supply
GND	J2	Input	Ground Reference
S/PDIF TX	J15	Output	CS8406 digital audio output via coaxial cable
S/PDIF TX	OPT2	Output	CS8406 digital audio output via optical cable
RS232 I/O	J42	Input/Output	Serial connection to PC for SPI / I^2C control port signals
USB I/O	J37	Input/Output	USB connection to PC for SPI / I^2C control port signals. **Not Available.**
PCM1 I/O	J10	Input/Output	I/O for Serial Audio Clocks & Data
CONTROL	J17	Input/Output	I/O for external SPI / I^2C control port signals.
MICRO JTAG	J36	Input/Output	I/O for programming the micro controller (U46).
FPGA-JTAG	J18	Input/Output	I/O for programming the FPGA (U35).
MICRO RESET	S2	Input	Reset for the micro controller (U46).
PROGRAM FPGA	S1	Input	Reset for the FPGA (U35).
PINA PINB	J38 J39	Input	RCA phono jacks for analog input signal to CS5345. Passive input filter.
AINA AINB	J40 J41	Input	RCA phono jacks for analog input signal to CS5345. Active input buffer.
MICIN1 MICIN2	J21 J34	Input	1/8“ TRS jacks for microphone input.
AOUTA AOUTB	J14 J16	Output	RCA phono jacks for PGA analog outputs. Active output buffer.

Table 4. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
J3	Selects the source of voltage for the VLC supply.	+1.8 V +2.5 V +3.3 V +5 V*	Voltage source is +1.8 V regulator. Voltage source is +2.5 V regulator. Voltage source is +3.3 V regulator. Voltage source is +5 V regulator.
J4	Selects the source of voltage for the VD supply	+3.3 V +5 V*	Voltage source is +3.3 V regulator. Voltage source is +5 V regulator.
J5	Selects the source of voltage for the VLS supply.	+1.8 V +2.5 V +3.3 V +5 V*	Voltage source is +1.8 V regulator. Voltage source is +2.5 V regulator. Voltage source is +3.3 V regulator. Voltage source is +5 V regulator.
J6	Selects the source of voltage for the VA supply	+3.3 V +5 V*	Voltage source is +3.3 V regulator. Voltage source is +5 V regulator.
J19 J20	Select the input type for channel 4 of the CS5345 ADC input multiplexer.	Line Input* Mic Input	Select RCA input multiplexer as source. Select TRS inputs as source.
J22 - J33	Maps the passive and active input circuits to the CS5345 input multiplexer channels.	Passive Filter* Active Filter	Passive filter mapped to input MUX channel. Active filter mapped to input MUX channel.

*Default factory settings

Table 5. System Jumper Settings

7. CDB BLOCK DIAGRAM

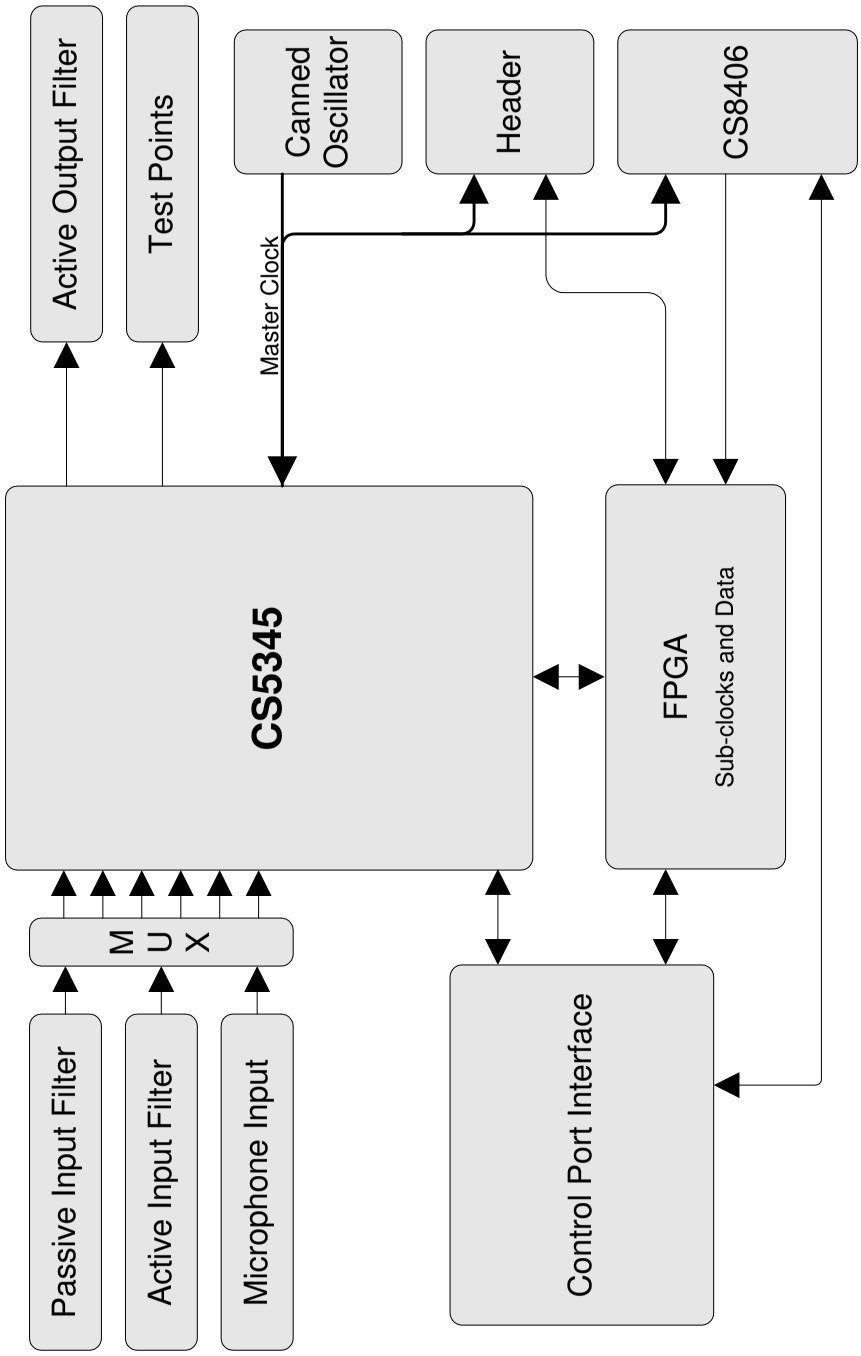

Figure 3. Block Diagram

8. CDB SCHEMATICS

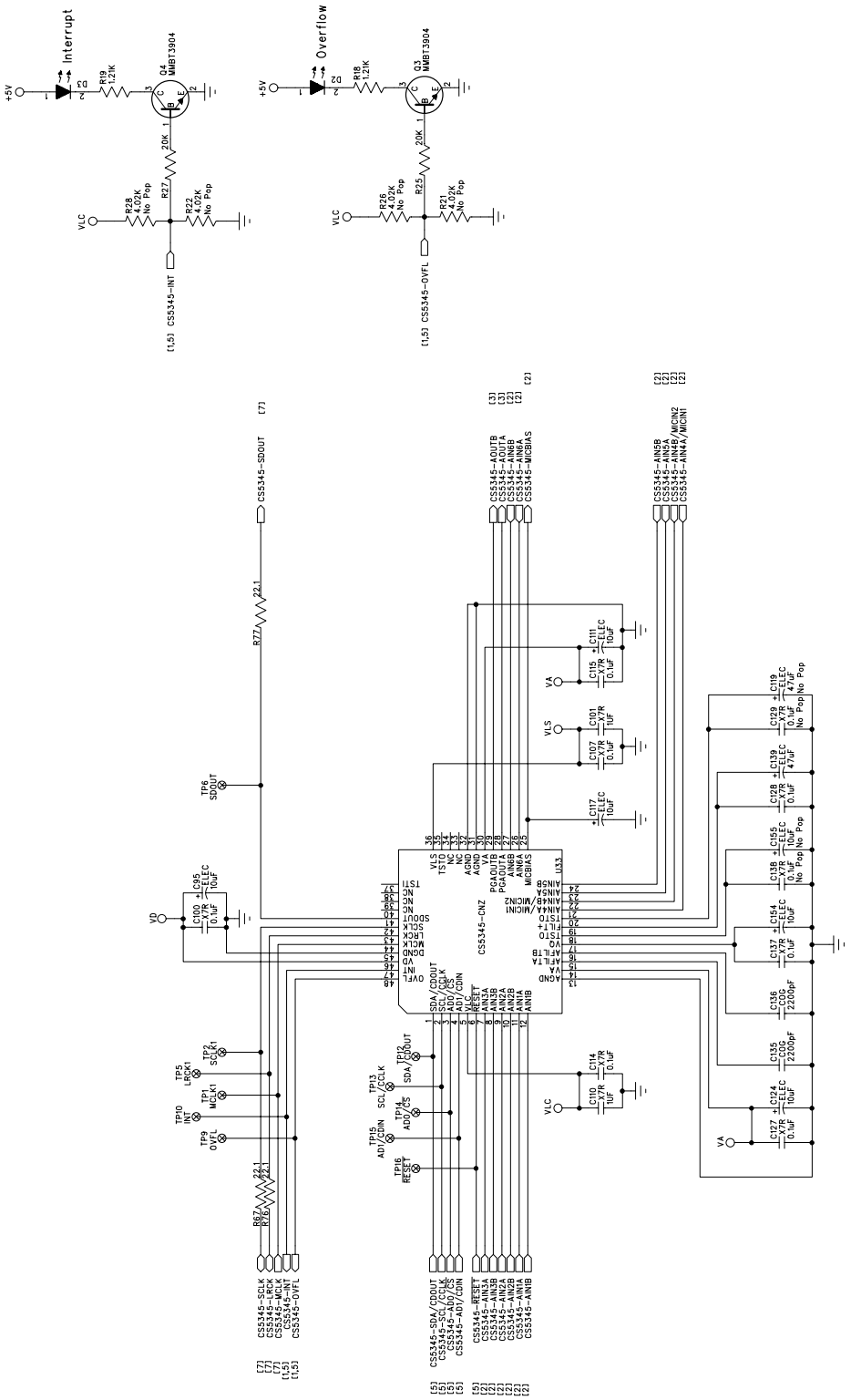

Figure 4. CS5345

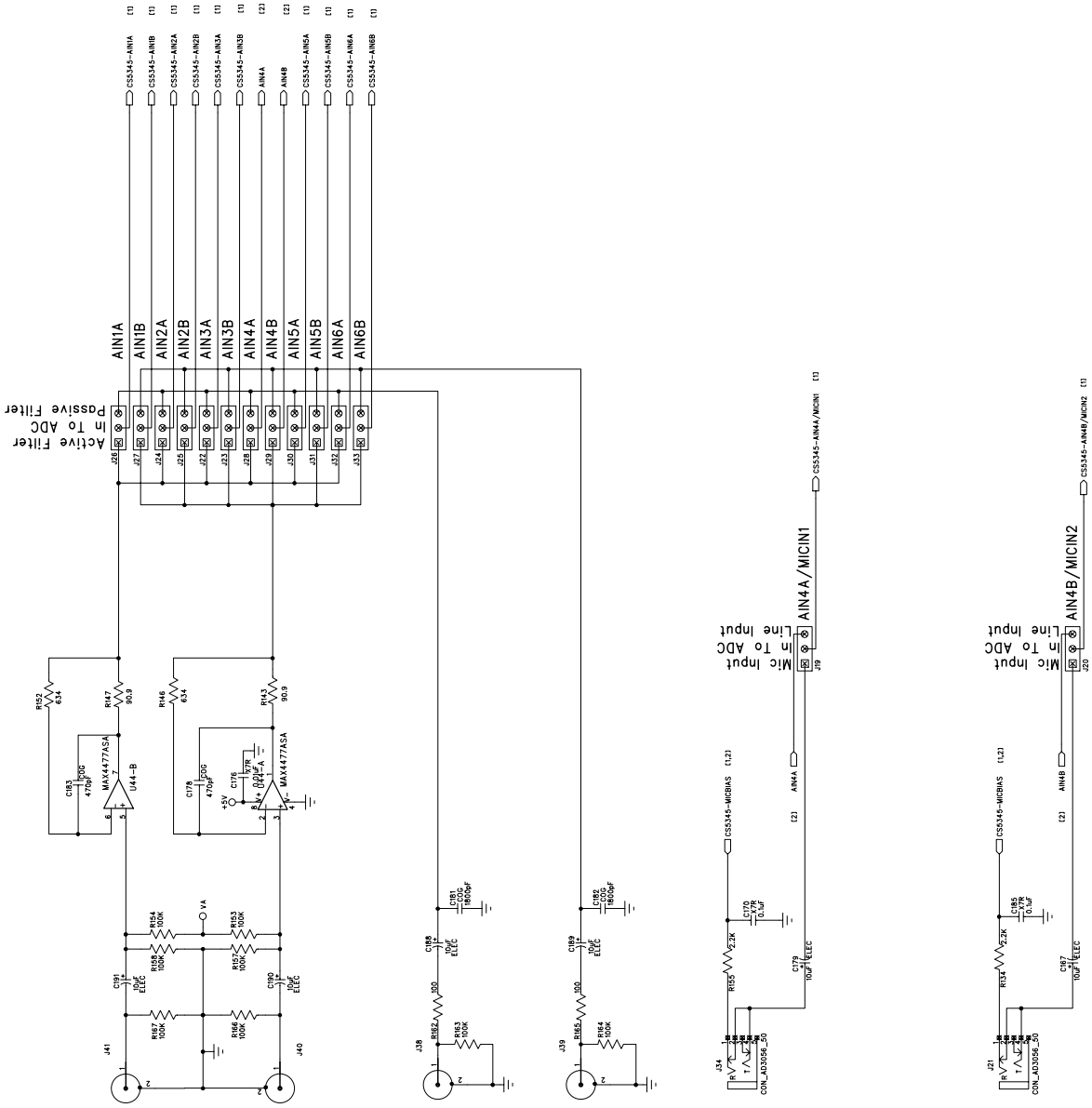

Figure 5. Analog Inputs

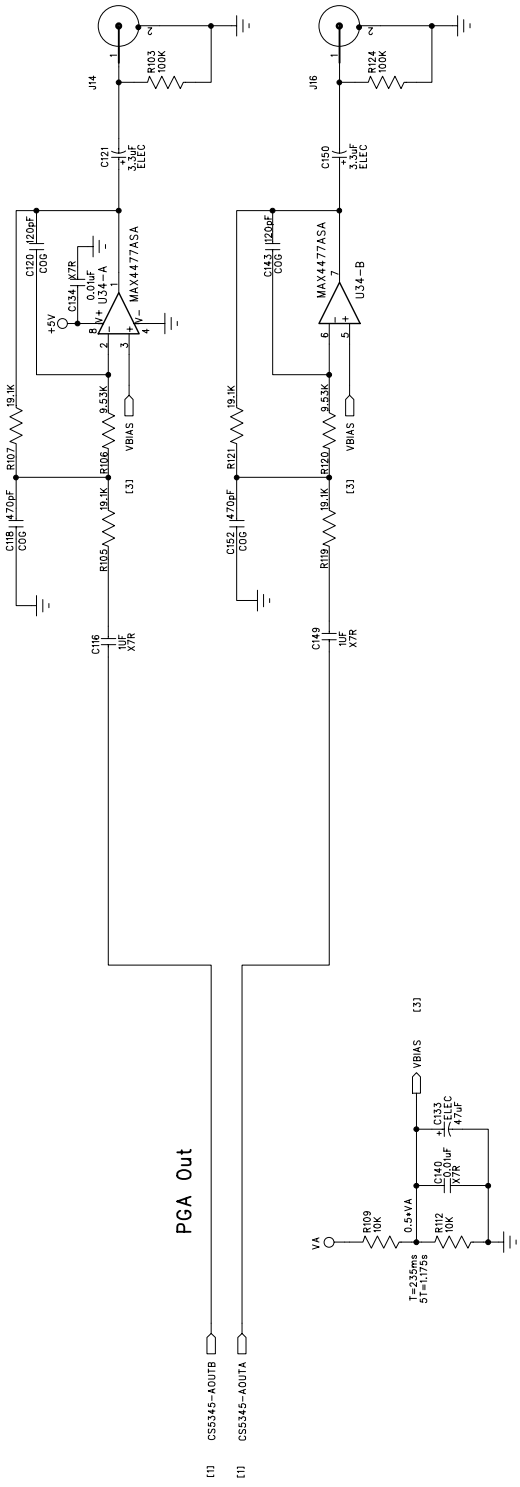

Figure 6. Analog Outputs

CS8406 – S/PDIF Transmitter

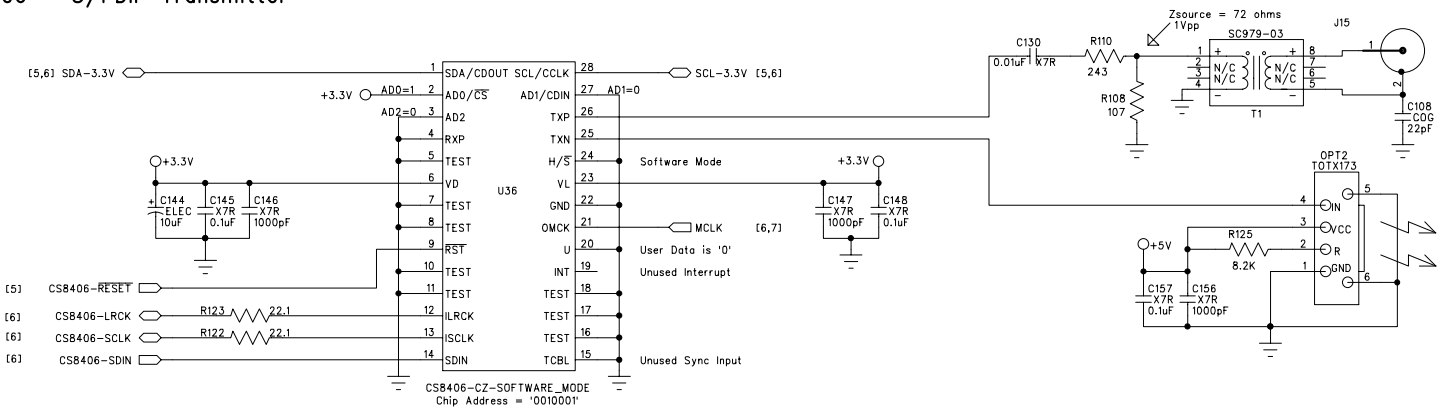

Figure 7. S/PDIF Output

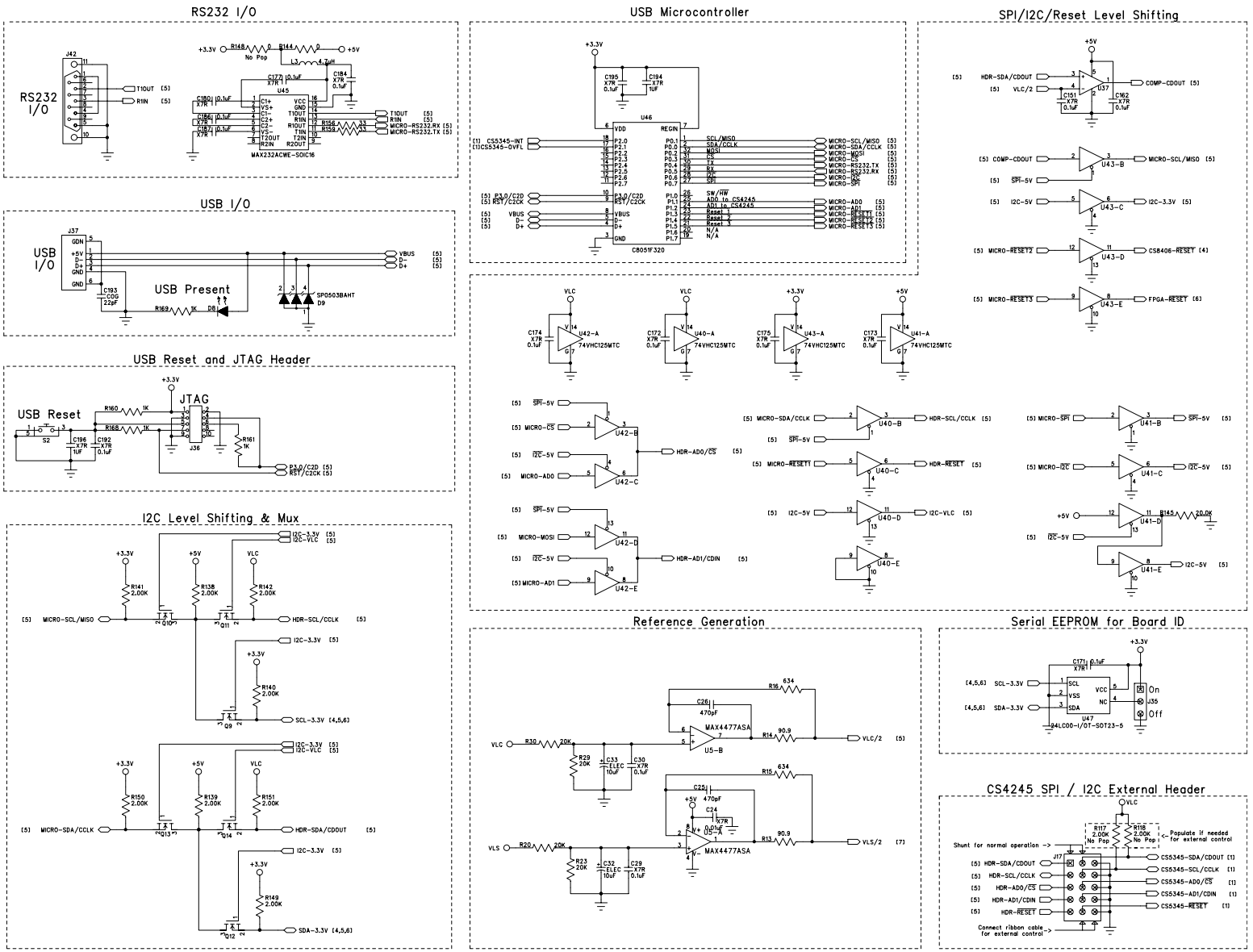

Figure 8. Control Port

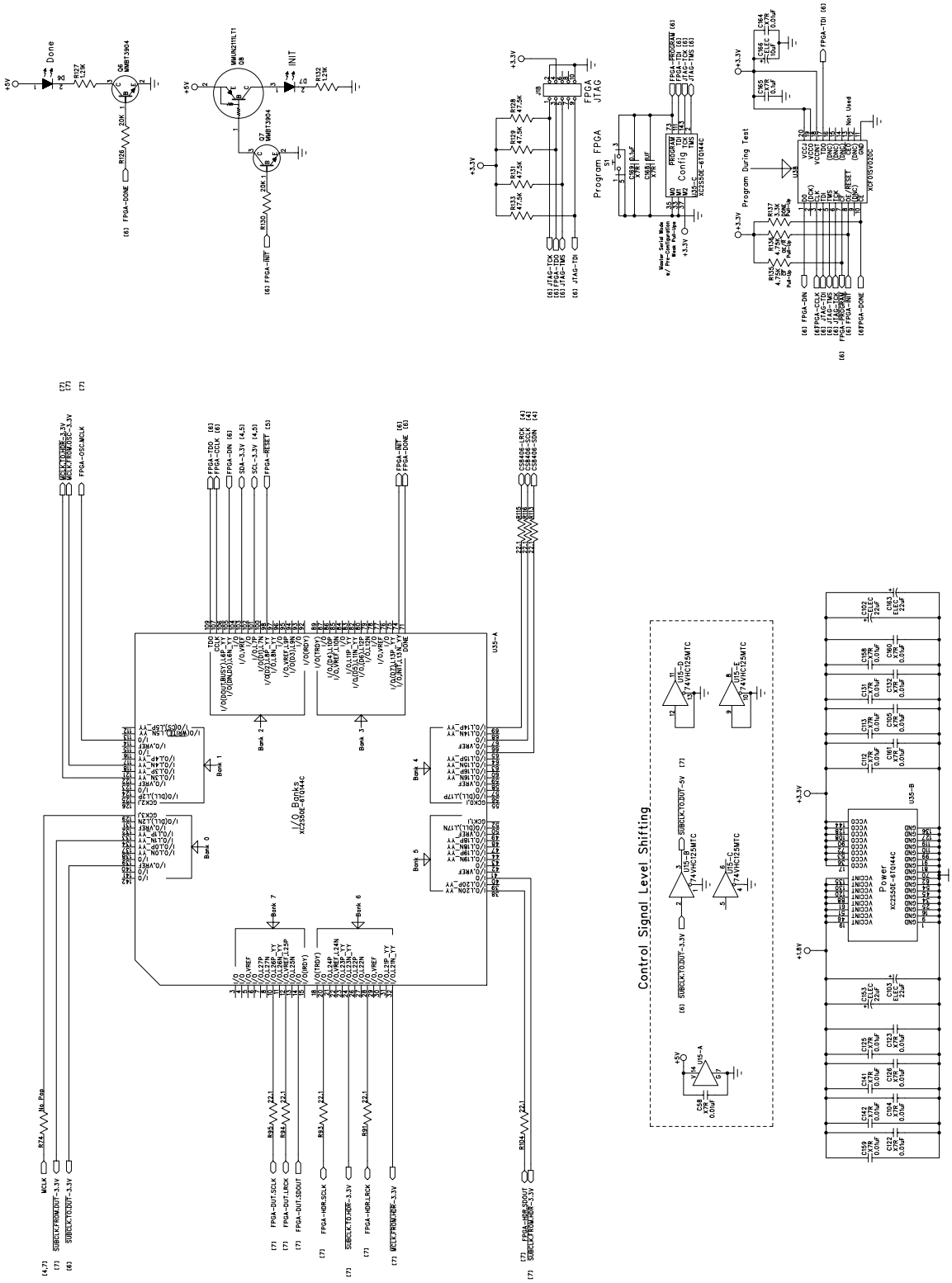

Figure 9. FPGA

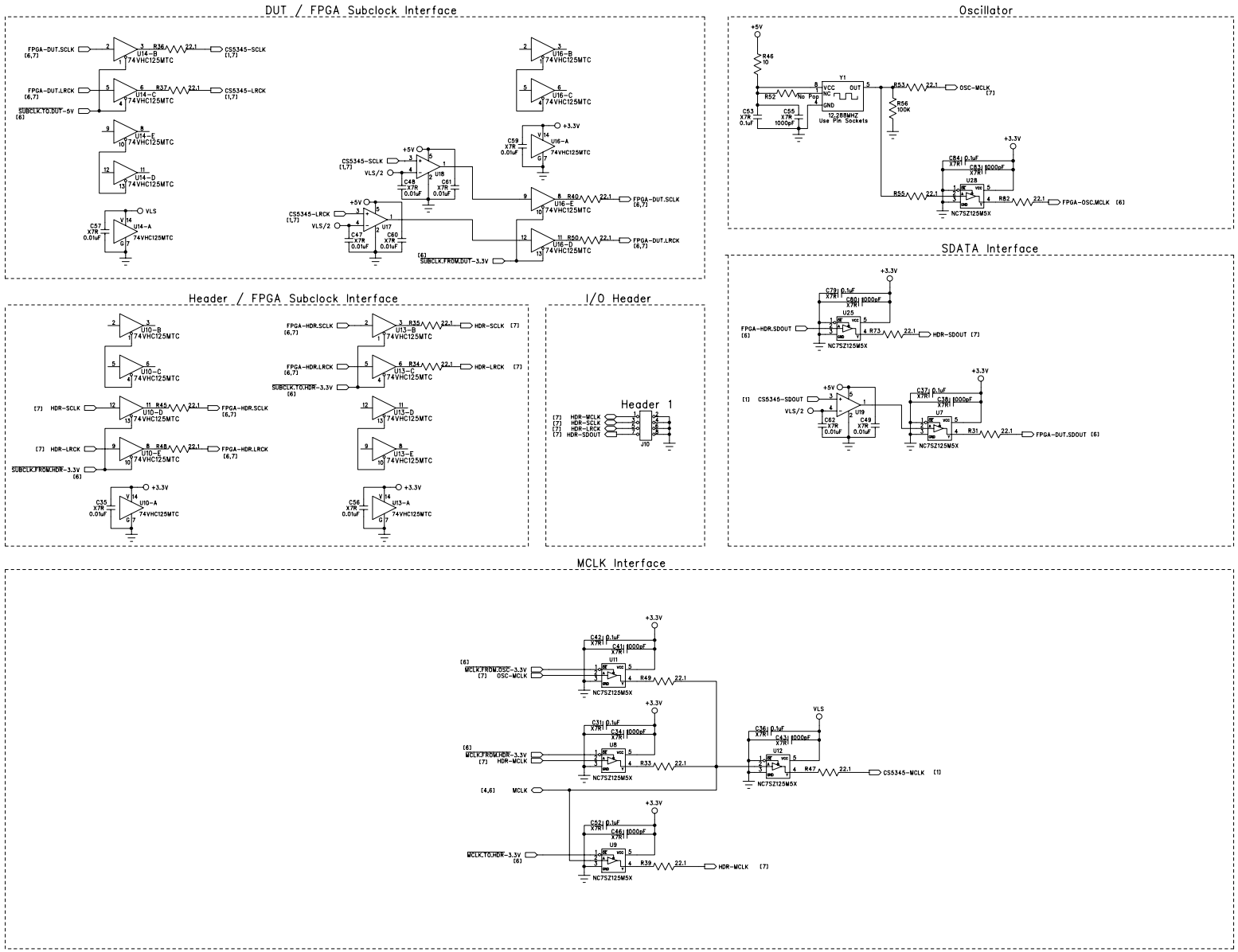

Figure 10. Discrete Clock Routing and Level Shifting

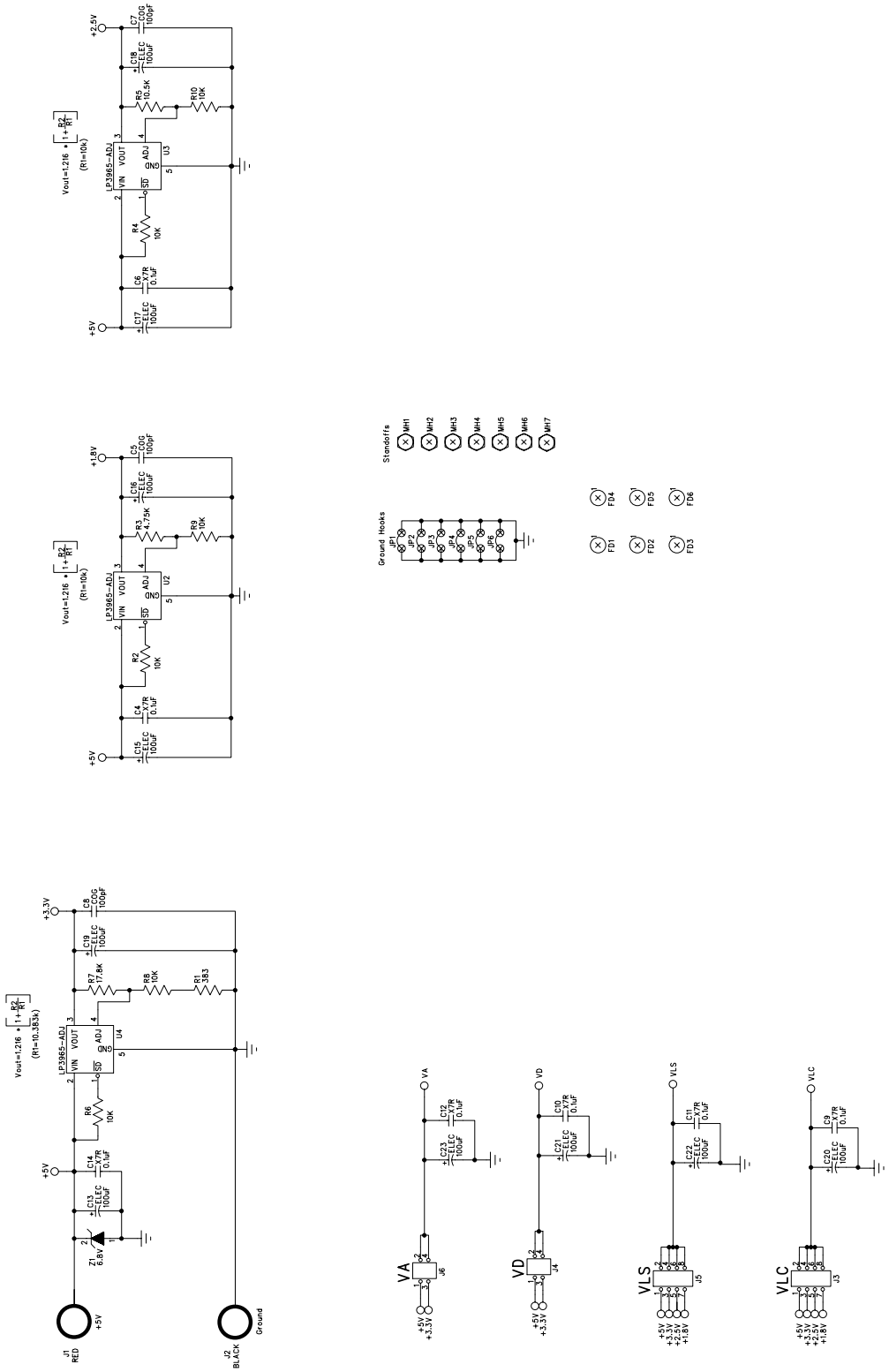

Figure 11. Power

9. CDB LAYOUT

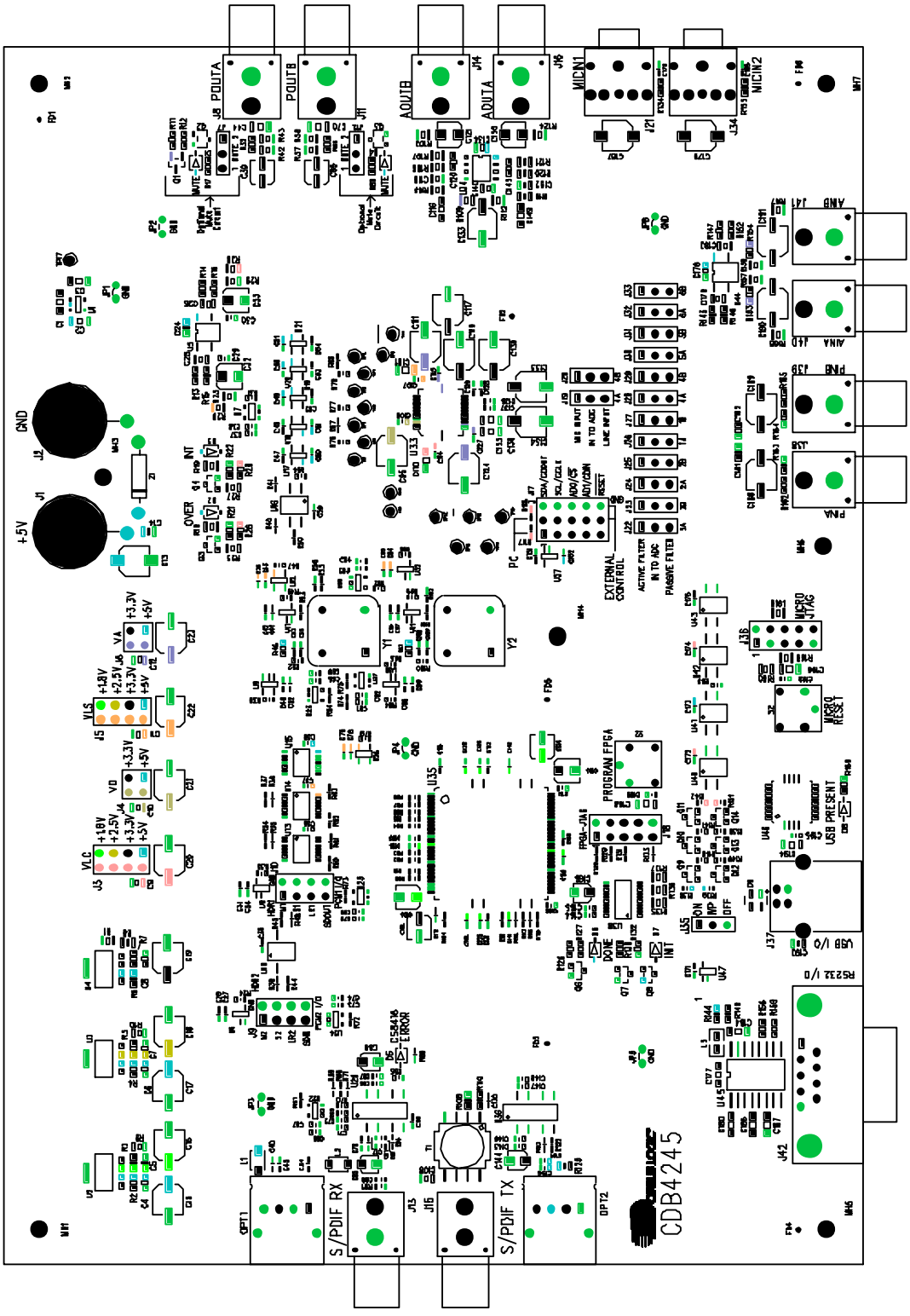

Figure 12. Silk Screen

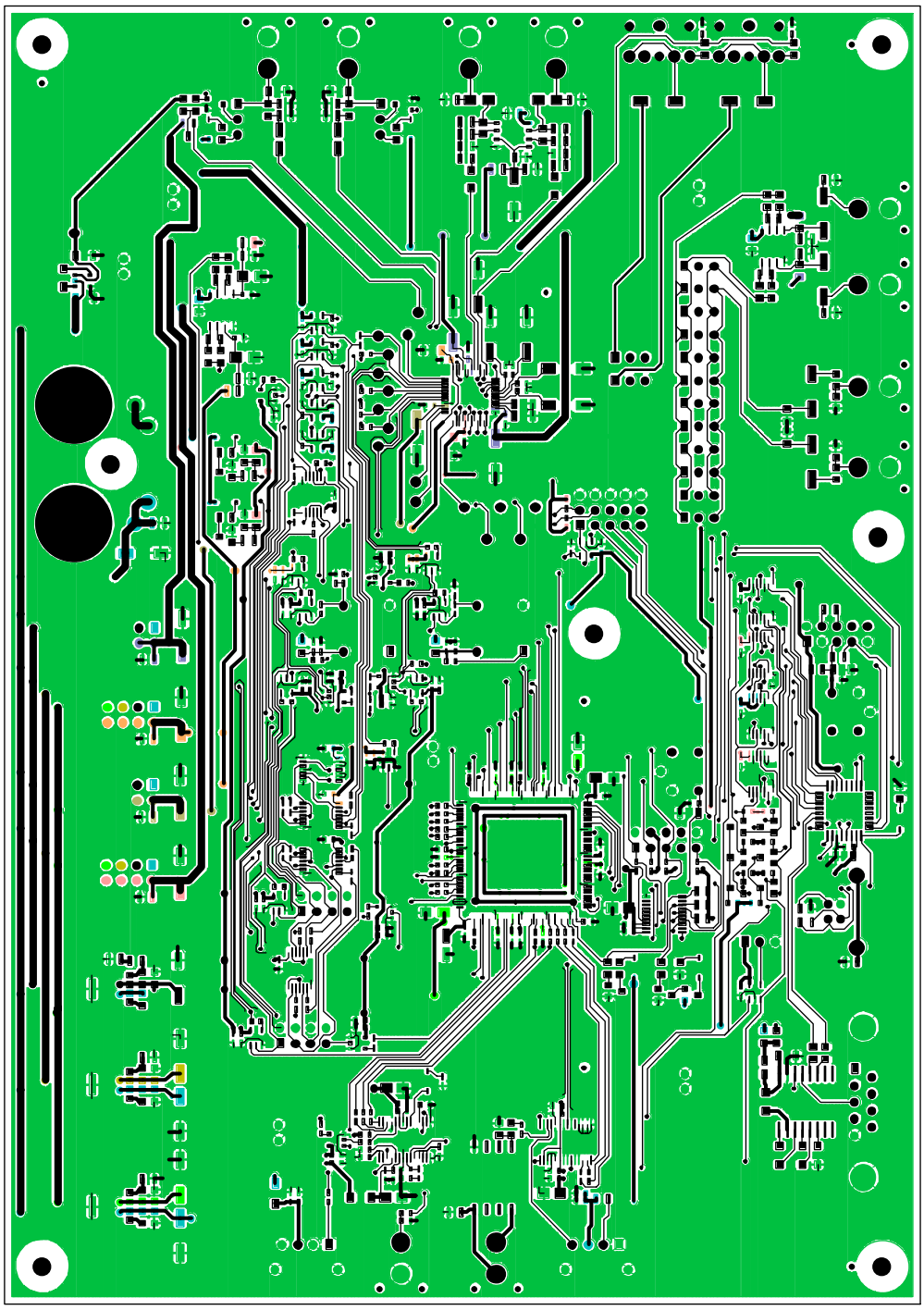

Figure 13. Topside Layer