Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

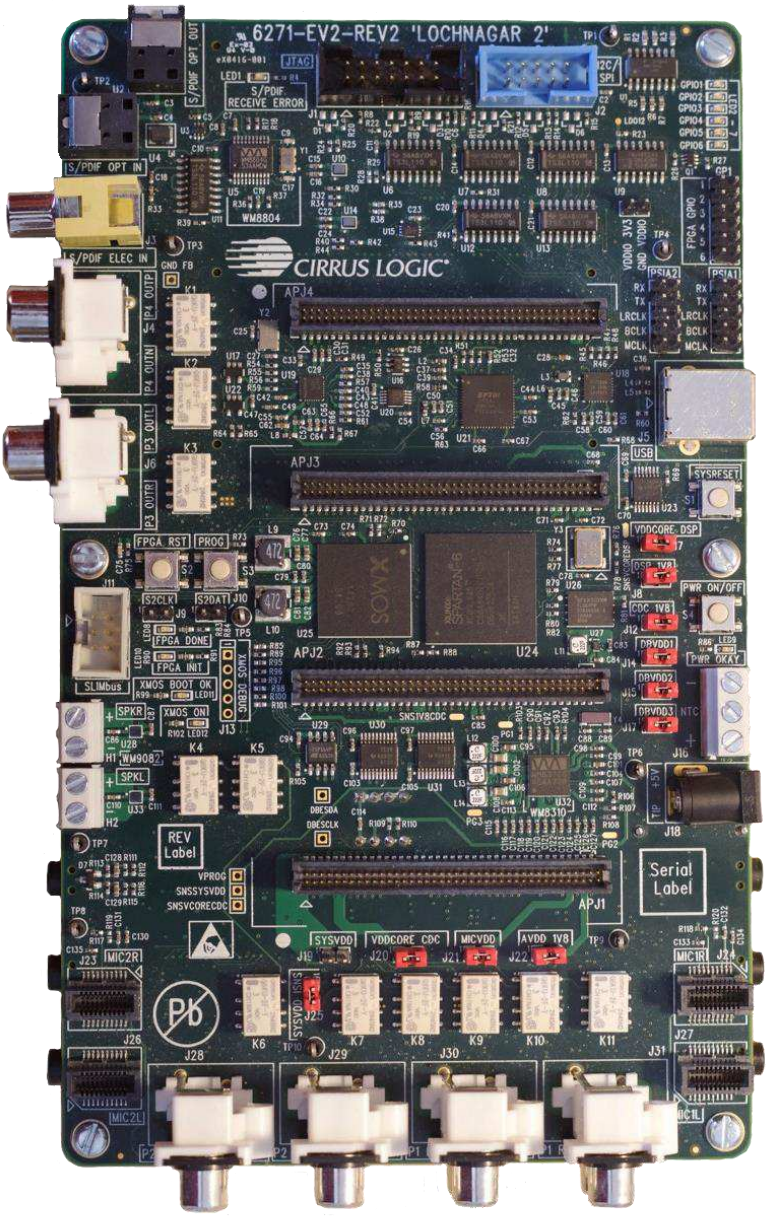
We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Lochnagar 2 User Guide

For firmware version: 1.0.0



Contents

1 Introduction 6

2 Hardware Connections 7

2.1 USB connection to PC 7

2.2 Power options 7

2.2.1 USB Power 8

2.2.2 Wall socket Supply 8

2.2.3 Battery / Bench Supply 9

2.3 Minicard Types 9

2.3.1 DSP Minicard 10

2.3.2 Codec Minicard 10

2.3.3 Microphone Minicards 10

2.4 Expansion Headers 10

2.5 Buttons / Switches 11

2.6 LED indicators 11

2.7 Other Headers 12

2.7.1 I2C/SPI (Aardvark) 12

2.7.2 JTAG 12

2.7.3 SLIMbus 12

2.8 Jumper Links 13

3 Driver Installation and WISCE Support 15

3.1 WISCE™ Device Pack 15

3.2 Minimum WISCE™ Version 15

3.3 Controlling Lochnagar 2 16

3.4 Lochnagar 2 Firmware Update 16

3.4.1 Hardware setup during update 16

3.4.2 Optional Update 17

3.4.3 Forced Update 17

3.4.4 Updating the Firmware 18

4 Clocking 19

4.1 Configuring Clock Routing 19

4.2 Clock Setup Guide 19

4.2.1 Example Configuration 20

4.3 Descriptions of clock sinks and sources 20
4.3.1 List of Clock Sinks 20
4.3.2 List of Clock Sources 21
5 Digital Audio 22
5.1 Digital Audio Connection Diagrams 22
5.2 Configuring Digital Audio Routing 23
5.2.1 BCLK / LRCLK Routing Operation 23
5.2.2 High Frequency Mode 24
5.2.3 Example Configuration 24
5.2.4 Advanced Clocking Configurations 24
5.3 AIF interfaces on codec minicard 25
5.4 AIF interfaces on the expansion headers 25
5.5 PSIA Headers 25
5.6 S/PDIF and ADAT 26
5.6.1 Standard use cases 26
5.6.2 Advanced use cases 27
5.7 Sound Card 28
5.7.1 Sound Card Audio Format 28
5.7.2 Enabling the Sound Card 29
5.8 Descriptions of AIF sinks and sources 30
5.8.1 List of AIF Sinks 30
5.8.2 List of AIF Sources 31
6 USB Audio Streaming 32
6.1 CLUSBAudio Control Panel 32
6.2 Using Lochnagar 2 with Windows DirectSound 34
6.3 Using Lochnagar 2 with WASAPI 35
6.4 Using Lochnagar 2 with ASIO 36
6.4.1 Adobe Audition Setup 36
6.4.2 Foobar Setup 37
6.5 I2S Format on Lochnagar 2 39
7 I2S TDM 40
7.1 I2S TDM Mux/Demux Operation 40
7.2 Configuring the I2S TDM Peripheral 41
7.2.1 Example Configuration 41

7.2.2 Description of I2S TDM sinks and sources 42
7.3 Clocking Restrictions 42
8 Analogue Audio 43
8.1 Analogue Port Connection Diagrams 43
8.2 Configuring Analogue Audio Routing 44
8.2.1 Save Settings to Profile 44
8.3 RCA Phono Input Ports 44
8.3.1 P1 phono inputs 44
8.3.2 P2 phono inputs 45
8.3.3 Input BIAS 46
8.4 Analogue/Digital Microphones 46
8.4.1 MICBIAS 46
8.4.2 Analogue Mics 47
8.4.3 Digital Mics 47
8.5 RCA Phono Output Ports 48
8.5.1 P3 phono outputs 48
8.5.2 P4 phono output 48
8.6 Speaker Outputs 49
8.7 Analogue I/O on the minicard 49
9 GPIOs 50
9.1 Setting up GPIO routing 50
9.2 GPIO level 51
9.3 Lochnagar 2 on-board GPIOs/LEDs 51
9.4 GPIOs on Codec Minicards 52
9.5 Descriptions of GPIO sinks and sources 53
9.5.1 GPIO Sink List 53
9.5.2 GPIO Source List 54
10 JTAG 55
10.1 Required Chess toolchain update 55
10.2 JTAG configuration 55
10.2.1 Example configuration 56
11 SLIMbus 58
11.1 SLIMbus Header 59
11.2 SLIMbus through Expansion Headers 59

12 Power 60
12.1 Configuring Power Options 60
12.2 MICVDD Options 60
12.2.1 Example Configuration 61
13 Current Monitor 62
13.1 Lochnagar 2 Power Rails 62
13.1.1 Monitored Voltage Rails 62
13.1.2 Unmonitored Voltage Rails 63
13.2 Current Monitor Plugin 63
13.2.1 Voltage / Current Rail Selection 64
13.2.2 Power Measurement 64
13.2.3 Measurement Modes 64
13.2.4 Samples/Reading 64
13.2.5 Export Measurements 65
13.2.6 Save/Load/Restore Settings 65
13.2.7 Board Temperature 65
14 Example Setup Scripts 66
14.1 WISCE™ Profile Scripts 66
14.2 Lochnagar 1 and Lochnagar 2 Register Compatibility 66
14.3 Details of Scripts Provided 67
14.3.1 Configuration Template Script 67
14.3.2 Lochnagar Setup Scripts 68
15 Troubleshooting 69
15.1 Lochnagar 2 Drivers in Device Manager 69
15.2 Common issues with Lochnagar 2 69
15.2.1 Audio Driver Issue: Drivers reinstalled while audio playing 69
15.2.2 COM Port Issue: Run out of COM port numbers 70
15.2.3 Lochnagar 2 does not appear in WISCE 70
16 Contacting Cirrus Logic Support 71

1 Introduction

Lochnagar 2 (6271-EV2) is the next generation evaluation and development board for Cirrus Logic Smart Codec and Amps devices. It is designed to provide a variety of audio inputs and outputs to the Cirrus devices and to allow for configuration and programming them in a variety of possible use cases.

Lochnagar 2 is the same form factor as the original Lochnagar board and is compatible with the same Smart Codec and Amp minicards. It provides all the same functionality as the previous generation, and in addition adds many new features and capabilities. This includes the ability to stream up to 16 channels of USB audio, and built-in current monitor feature that allows the power consumption of the Cirrus devices to be measured without any external equipment.

This document describes the features and usage of Lochnagar 2 in detail. The first two sections deal with the initial steps of hardware configuration and driver installation. The sections after this detail each of the features of the board and how to set it up in any potential use case. The final sections detail how to use the setup scripts provided with the Lochnagar 2 Device Pack and a guide on troubleshooting the board if any problems occur.

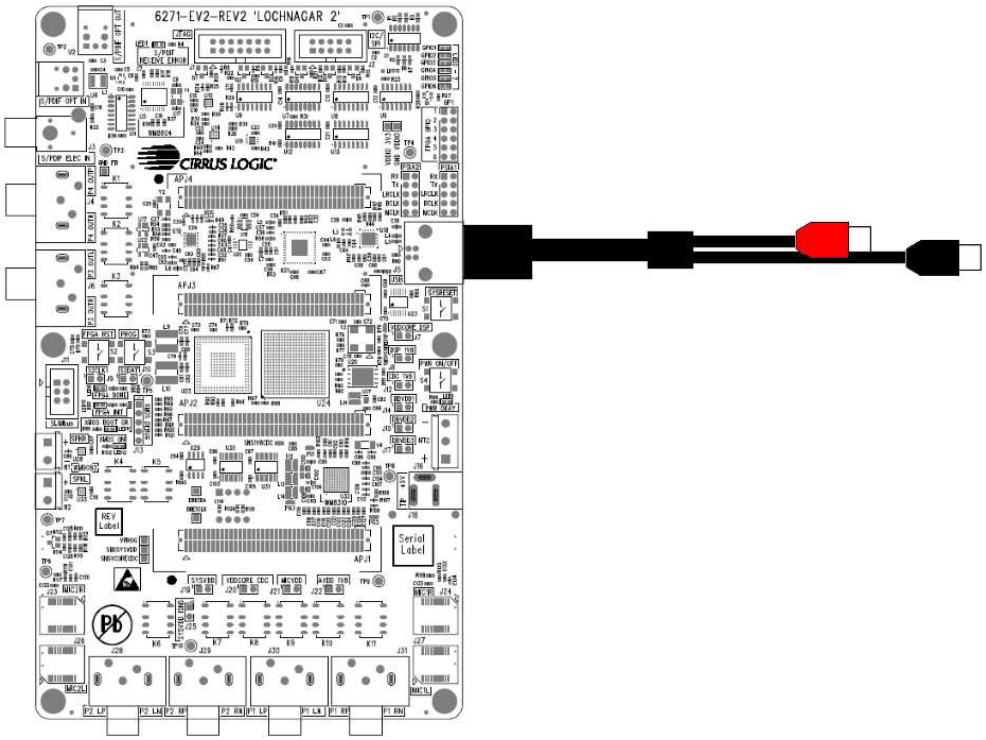
2 Hardware Connections

2.1 USB connection to PC

Lochnagar 2 is powered and controlled via a single USB connection. This provides:

- Power
- I2C/SPI communications to control device and board
- JTAG communications for DSP debug
- Multichannel USB streaming audio (USB class 2)
- USB serial port to communicate with Cirrus devices with UART interfaces

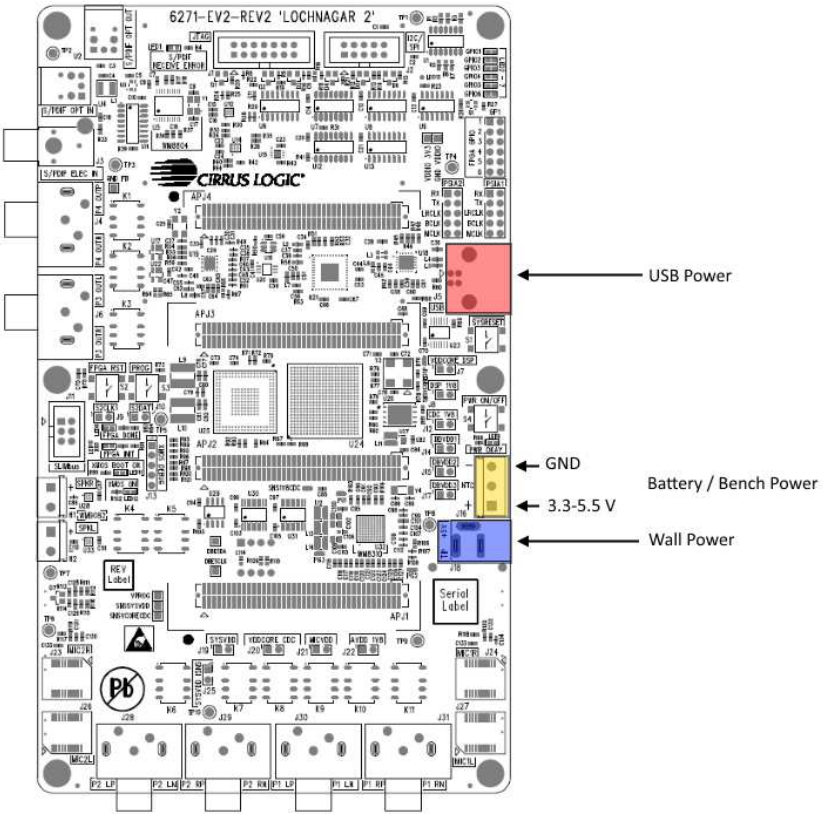
The board is provided with a Y-shaped USB cable, connecting a single USB B socket on Lochnagar 2 to two USB A ports on the computer (Black plug for power + communications, Red for power only). Both USB connectors must be plugged in to allow for the power consumption of the board.



A Total Phase Aardvark connector is **NOT** required for Lochnagar 2 to operate, and neither does it require a separate power supply. All power and communications is provided to the board via this single USB link.

2.2 Power options

For most use cases, the provided USB cable is enough to power the entire board. In some scenarios, especially those using speakers, it may be necessary to plug a second power source into the Lochnagar 2 board. The onboard WM8310 PMIC will select the highest voltage from each of the three potential power supply inputs and use this to power the board's main SYSVDD bus. This is nominally 5V, but may be lower if a battery is used to supply the board.



2.2.1 USB Power

As described in the USB Connection to PC section, this is the normal mode of operation for the Lochnagar 2 board. For most use cases, USB power alone is adequate and there is no need to connect any additional power supplies to the board.

To be certain of getting the full 900 mA maximum input current supported by Lochnagar 2 USB connection, it is vital to ensure that a Y-shaped dual-USB cable is used and that both ends are plugged in at the PC end. If a USB hub is used, then it is also important to use a self-powered USB hub with a wall power connection, as otherwise it may not be able to supply enough current.

2.2.2 Wall socket Supply

Lochnagar 2 provides a socket to accept 5V input from a dedicated wall supply.
It may be necessary to plug in the Wall supply as well as the USB connector for more power-hungry use-case scenarios such as those involving speakers.

The wall power connector J30 is positive tip (Tip = +5V), in contrast to the original Lochnagar board which used negative tip.

Protection diodes are fitted to prevent damage if a negative tip supply is inserted.

2.2.3 Battery / Bench Supply

Lochnagar 2 has three screw terminals which allow either a battery or a bench-top power supply unit to be plugged into the board.
It may be necessary to plug in a bench supply as well as the USB connector for more power-hungry use-case scenarios such as those involving speakers.

This input is nominally expected to be a 4.2 V battery, but the terminals can accept anything from 3.3 - 5.5 V. The terminals are marked with + and - symbols on the silkscreen to denote power and ground respectively.

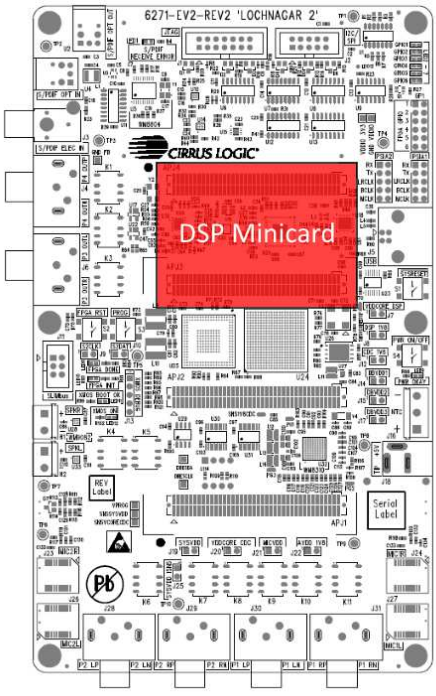
Note that when the battery / bench supply is used as the sole power source for the board, the PWR ON/OFF button (S4) must be held down in order to power the board. This is in contrast to the other supply options, where the board will automatically power on as soon as the Wall or USB connector are plugged in.

2.3 Minicard Types

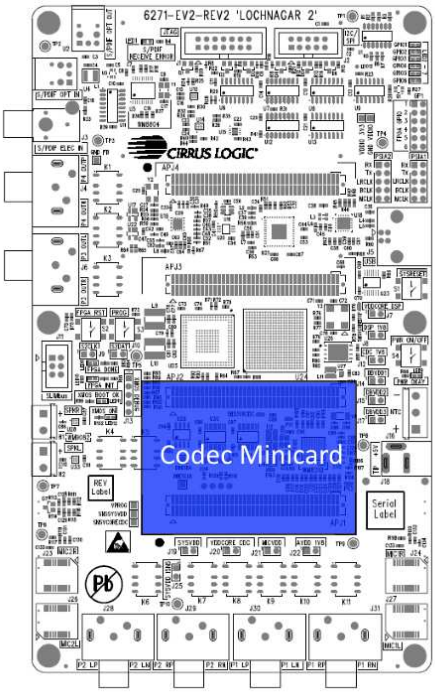
Lochnagar 2 works with interchangable minicards to allow for a variety of Smart Codec devices. The minicard connectors are fully backwards compatible with the original Lochnagar board.

Minicards should not be inserted or removed while the Lochnagar 2 board is powered. If using the Wall Socket or Battery / Bench Screw Terminals for board power, then it is recommended to fully disconnect or power down the external supply before changing minicards.

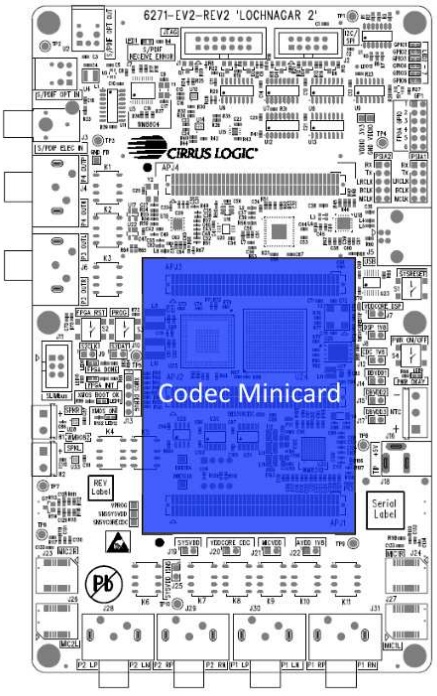
There are three main categories of minicard that can connect to Lochnagar 2.



DSP minicard



Codec minicard (2-header)



Codec minicard (3-header)

2.3.1 DSP Minicard

This type of minicard was designed for an older range of sidecar DSPs that sit alongside a Codec minicard.

DSP minicards connect to the top two headers on the Lochnagar 2 board.
There are no current product lines that use the DSP minicard slot.

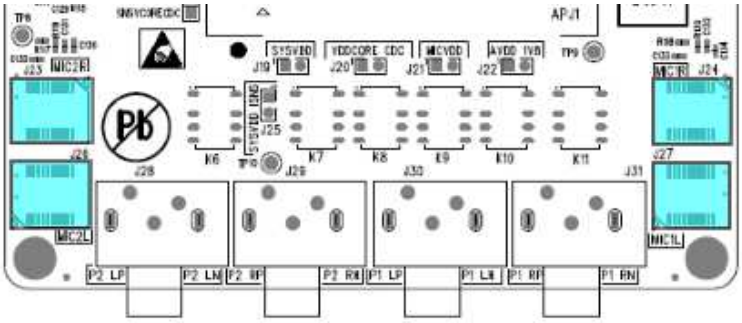
2.3.2 Codec Minicard

Codec minicards house Cirrus Codec and Smart Codec type devices. Smart Codecs include a built-in DSP, but are not classed as "DSP" minicards.

Traditionally Codec minicards connect to the lower two headers on the Lochnagar 2 board.
However, some of the larger Smart Codec devices extend onto the third header in order to make use of the extra I/O.
These cards cannot be used alongside a DSP minicard.

2.3.3 Microphone Minicards

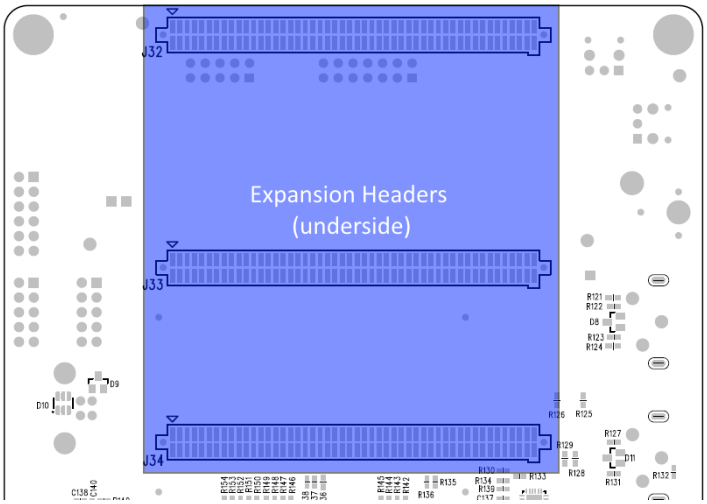
There are four microphone slots on the bottom of the Lochnagar 2 board.



These are designed to accept Cirrus Digital and Analogue microphone minicards.

2.4 Expansion Headers

There are three Expansion Headers on the underside of Lochnagar 2.
These are designed to connect the board to other test hardware. They are commonly used to connect Lochnagar 2 to a Linux Application Processor system.



2.5 Buttons / Switches

There are four push buttons on the Lochnagar 2 board connected with power and reset functionality.

Part Number	Name	Description
S1	SYSRESET	Resets all power rails on the board, returning all components to default state inc. Codec and FPGA
S2	FPGA RST	Resets all FPGA registers
S3	PROG	Resets FPGA operation, forcing a reprogram from EEPROM This will also reset all FPGA registers and re-initialise other components on the board
S4	PWR ON/OFF	Press when powered off: Power on the board Hold down for 2 seconds: Power off the board

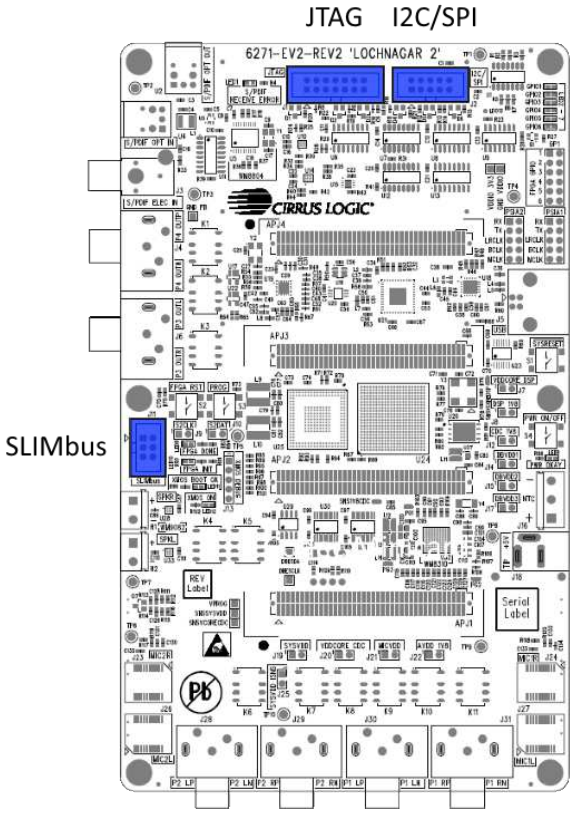
2.6 LED indicators

There are six status LEDs on Lochnagar that indicate the board's current state of operation

Part Number	Colour	Name	Normally lit?	Description
LED1	Red	S/PDIF RECEIVE ERROR	No	Set to red when there is an error receiving S/PDIF signals
LED2-7	Green	GPIO1 - GPIO6	No	Tied to FPGA GPIOs 1 to 6.
LED8	Green	FPGA DONE	Yes	Indicates that the FPGA booted successfully
LED9	Green	PWR OK	Yes	Indicates the Lochnagar 2 board has power applied
LED10	Red	FPGA INIT	No	Indicates that the FPGA is currently initialising. Should flicker once upon board startup/power applied.
LED11	Green	XMOS BOOT OK	Yes	Indicates that the XMOS USB transceiver chip booted correctly
LED12	Green	XMOS ON	Yes	Indicates that the XMOS USB transceiver chip is powered

2.7 Other Headers

There are several other headers on the Lochnagar 2 board that allow for connections to other systems.



2.7.1 I2C/SPI (Aardvark)

Header J2 (I2C/SPI) is designed to connect to Total Phase Aardvark systems for legacy compatibility with the original Lochnagar board.

All I2C/SPI communications for most use cases is now expected to go through the standard USB/XMOS link that also powers the board and provides USB Audio streaming capability. However, the Aardvark can still be used for legacy applications or as a slave to test SPI master peripherals on the minicard.

2.7.2 JTAG

Header J1 (JTAG) is designed to connect to Macraigor usbWiggler JTAG systems for legacy compatibility with the original Lochnagar board.

As with the I2C/SPI communications, JTAG functionality is now possible using the standard USB link that also powers the board and provides USB Audio streaming. It is still possible to use the Macraigor through this header if required. USB is the default option within the register map.

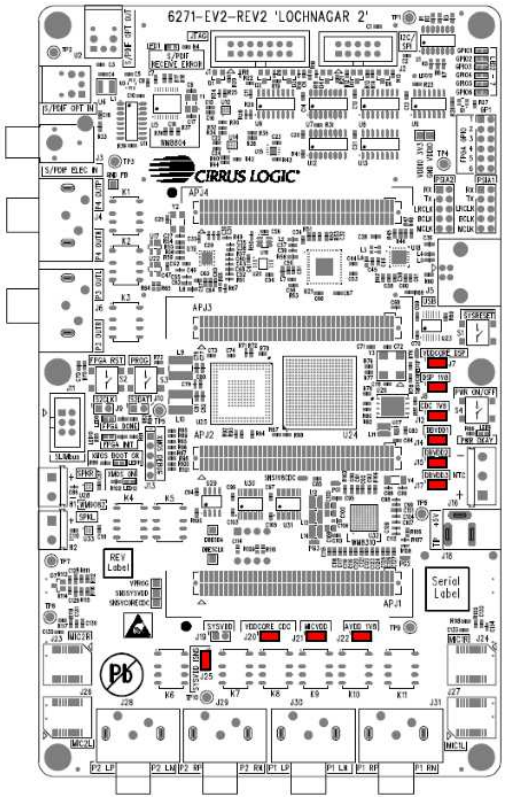
2.7.3 SLIMbus

A 2x3 box header is provided to connect Lochnagar 2 to LnK SLIMbus test systems.

2.8 Jumper Links

Lochnagar 2 has removed most of the jumpers from the original Lochnagar board, and replaced them with relay switches. All analogue audio routing is now controlled via the FPGA register map.

There are 11 jumpers on the Lochnagar 2 board. These are all related to power supply rails.



These jumpers allow you to either isolate certain supply rails from the minicard, or insert a series ammeter between the two pins in order to measure current consumption on individual rails.

No jumper should be fitted over J19 (SYSVDD), as this will prevent the built-in current monitor circuitry from working correctly.

Header	Power Rail	Default Voltage	Jumper default
J7	VDDCORE DSP	1.2 V	On (fitted)
J8	DSP 1V8	1.8 V	On (fitted)
J12	CDC 1V8	1.8 V	On (fitted)
J14	DBVDD1	1.8 V	On (fitted)
J15	DBVDD2	1.8 V	On (fitted)
J17	DBVDD3	1.8 V	On (fitted)
J19	SYSVDD	Alternative SYSVDD jumper connection bypassing the current sense circuitry. Should only be used if the current sense circuitry is causing issues.	Off (not fitted)

Header	Power Rail	Default Voltage	Jumper default
J20	VDDCORE CDC	1.2 V	On (fitted)
J21	MICVDD	1.8 V	On (fitted)
J22	AVDD 1V8	1.8 V	On (fitted)
J25	SYSVDD ISNS	Highest of Wall, USB and battery supplies Normally 5V	On (fitted)

Note that these power rail names refer to the rails on the Lochnagar 2 board and may not directly correspond to the rails on the device/minicard. This depends entirely upon the schematic designer of the codec minicard, and how they have decided is the best method to connect the DUT to the Lochnagar system. Always refer to the board schematics if there is any doubt.

(For example, recent codec minicards such as Moon CDB47L91-M-1 do not use the DBVDD1, DBVDD2, DBVDD3, AVDD_1V8 rails, but instead derive all 1.8V rails from the single 1V8_CDC supply rail on Lochnagar and split the rails on the minicard).

3 Driver Installation and WISCE Support

3.1 WISCE™ Device Pack

In order to communicate with the Lochnagar 2 board, WISCE™ needs the Lochnagar 2 Device Pack to be installed.

This automatically installs:

- Latest version of Lochnagar 2 board firmware
  - Use WISCE plugin to start the update
- Lochnagar 2 configuration plugin for WISCE™
- Current Monitor plugin for WISCE™ to monitor current on selected supply rails
- Lochnagar 2 ASIO drivers for USB audio
- Lochnagar 2 SPI/I2C communications driver
- Register map description for WISCE™
- Sample WISCE™ configuration scripts for the board

If upgrading...

Close all audio streaming applications (eg. Adobe Audition or Foobar) before upgrading your Lochnagar 2 drivers to the latest version.

If an application is streaming audio (or has an open connection to the driver) during the installation process, the driver installation will not be successful. The system will present itself as a "USB Composite Device" and attempts to automatically install the drivers will generate the error "This device cannot start. (Code 10)."

If this happens, the solution is to close all applications and re-install the Device Pack again from scratch.

3.2 Minimum WISCE™ Version

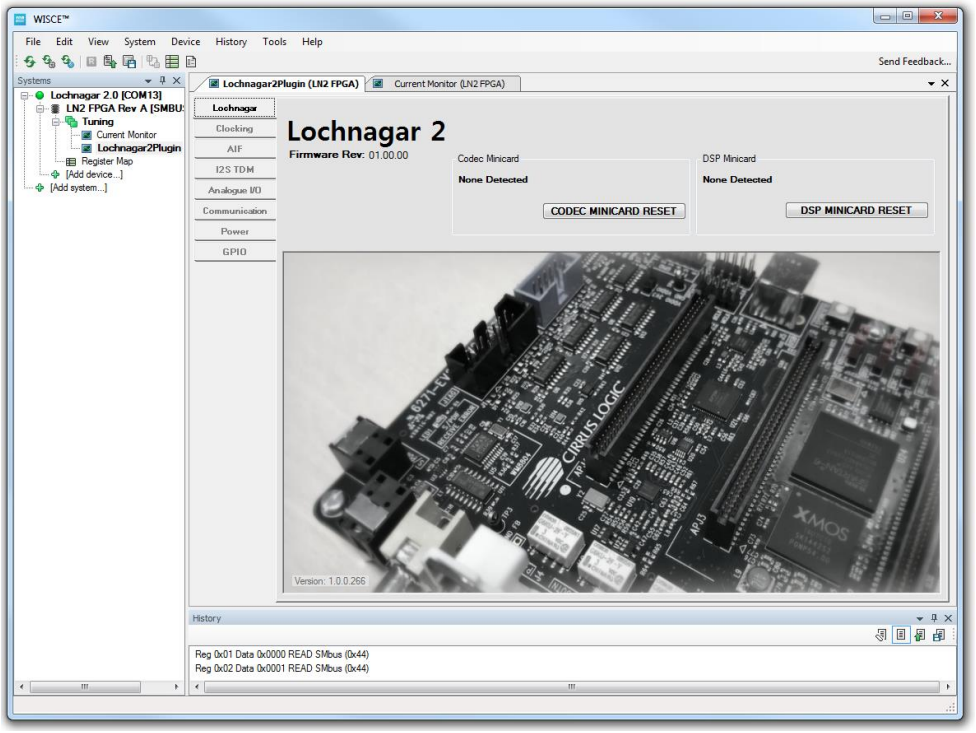
The WISCE™ 3.4.0.3 provides a minimum level of support for Lochnagar 2, but does not provide the full feature set. It is strongly recommended to use version **3.5.0.21** or above.

- The current stable release of WISCE is available from the public Cirrus website
  - http://www.cirrus.com/en/support/software/evaluationsoftware.html

3.3 Controlling Lochnagar 2

Upon opening WISCE™, the Lochnagar 2 board should be automatically detected.

It will appear as a device called "**LN2 FPGA**" at I2C address 0x44. The **LN2 FPGA** device should have a "Tuning" folder that contains both the **Lochnagar2Plugin** and **Current Monitor** plugin. These allow for full configuration of the Lochnagar 2 board.



3.4 Lochnagar 2 Firmware Update

After installing the latest WISCE Device Pack, restart WISCE and open the Lochnagar 2 Plugin.

3.4.1 Hardware setup during update

Firmware updates will generally work with most hardware minicards attached.

It is recommended to unplug any minicards, interposers or connectors that have their own separate power supplies during the Lochnagar 2 firmware upgrade process, as they may interfere with the process.

This includes:

- FPGA Emulation Interposers
- Zynq systems
- Amplifier minicards with separate power connections

3.4.2 Optional Update

If the Lochnagar 2 firmware is not up-to-date, a yellow box prompting the user to update the board firmware will be displayed on the main page of the plugin:

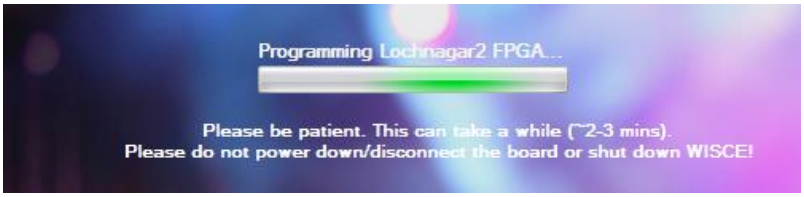
3.4.3 Forced Update

If the version of firmware on the board is so old that the plugin / register map will not function at all, the plugin will remove the element of choice and will force the user to do an update before it can operate:

Firmware numbers in the screenshots are for illustration purposes only and may not reflect the behaviour of actual firmware releases.

3.4.4 Updating the Firmware

After clicking the "Update" button in the plugin, it will display a prompt to reset the board and confirm that the user intends to do a board update.
After confirming, it will take 2-3 minutes for the firmware update to complete.



It is important not to shut down WISCE™ or power down or disconnect the Lochnagar 2 board during the firmware update process, as this may result in the Lochnagar 2 hardware becoming unusable.

4 Clocking

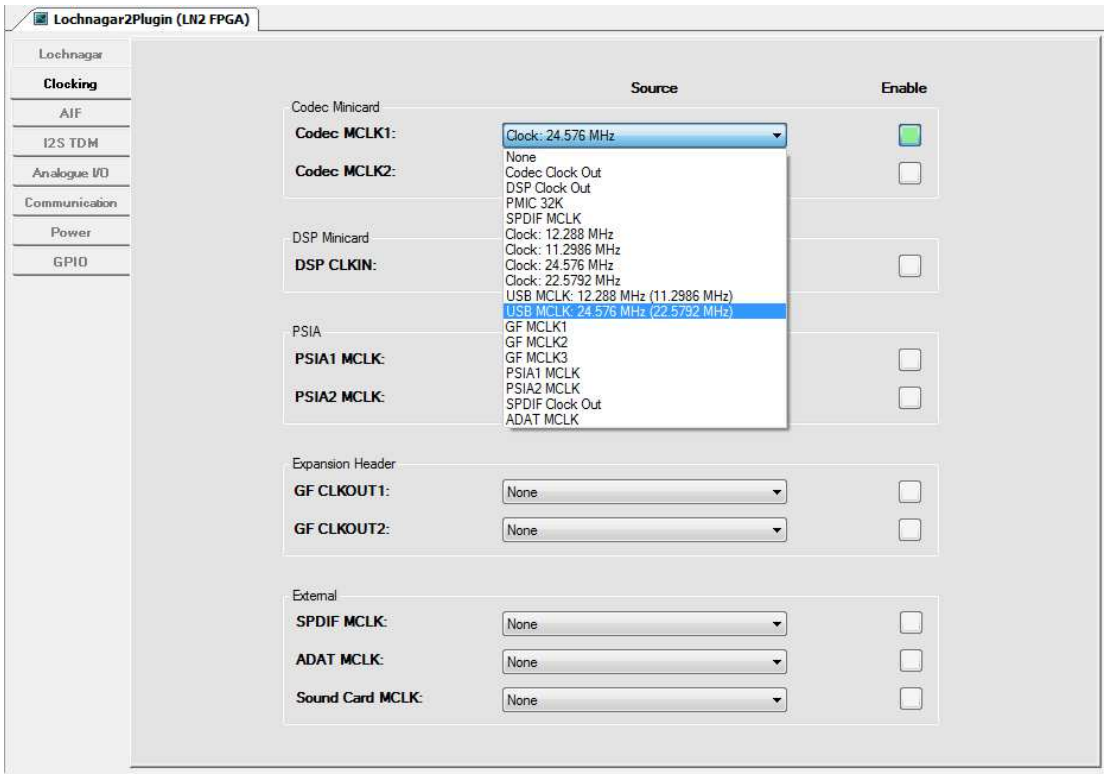
The Lochnagar 2 FPGA controls the clock routing on the board.

If no clock input is provided to the Cirrus device on the minicard, then it may not operate correctly. It is vital to configure the clocks on the Lochnagar 2 board before attempting to use the device.

4.1 Configuring Clock Routing

Digital clock signals on Lochnagar 2 are routed through the central FPGA and can connect the clock signals on the board to a number of input sources.

Routing is controlled via the **Clocking** panel of the Lochnagar 2 plugin.



4.2 Clock Setup Guide

The Lochnagar 2 FPGA manages the clocking setup of various clocks on the board.

Clock signals are separated into clock sources (available clock frequencies from a variety of sources) and clock sinks (signals that require an input clock). The Lochnagar 2 allows the user to connect any clock source to any of the available clock sinks. There are some clocks that can be either source or sink, depending on the configuration. For example, if a PSIA header is used to connect the Lochnagar 2 to an Audio Precision test system, the Audio Precision can act as either

MCLK master or slave, depending on the setup. Accordingly, Lochnagar 2 allows this clock signal to be used as either a Sink or a Source.

Lochnagar 2 has an on-board clock generator that generates the following frequencies: 11.2986 MHz, 12.288 MHz, 22.5792 MHz and 24.576 MHz. In addition, clocks can be provided from the USB streaming peripheral, PSIA headers, GF Expansion Headers, PMIC chip, clock output pins from the codec or DSP minicards, the S/PDIF transceiver or ADAT source.

When using digital audio with Cirrus Smart Codec devices, the MCLK signal provided to the chip should be synchronous with any digital audio interfaces used on the chip. For example, if using the audio from the USB audio streaming, the MCLK provided to the slave device needs to be synchronous with the audio data coming from the USB audio streamer. For this reason, a USB, PSIA, S/PDIF and ADAT MCLK signals are provided as available clock sources in the Clocking tab.

4.2.1 Example Configuration

To connect the USB MCLK signal to the Sound Card clock:

1. Open the Clocking tab of the plugin
2. Find the row associated with the Sound Card MCLK clock sink
3. Select USB MCLK: 24.576 MHZ (12.288 MHz) Clock Source from the drop-down menu on the Sound Card MCLK row.
4. Click the enable button on the same row

This will provide the 24/22 MHz USB MCLK signal into the Sound Card peripheral.

4.3 Descriptions of clock sinks and sources

4.3.1 List of Clock Sinks

This lists all the potential destinations that clock signals can be routed to on Lochnagar 2. The register map addresses for the control registers associated with these clock sinks are provided for advanced users.

Clock Sink	Control Register	Description
Codec MCLK1	R1Eh	Master clock input on the codec minicard
Codec MCLK2	R1Fh	Master clock input on the codec minicard
DSP CLKIN	R20h	Clock input on the DSP minicard
PSIA1 MCLK	R21h	Master clock input or output signal on the PSIA1 pin headers
PSIA2 MCLK	R22h	Master clock input or output signal on the PSIA2 pin headers
GF CLKOUT1	R24h	Clock output to the GF expansion headers
GF CLKOUT2	R25h	Clock output to the GF expansion headers
SPDIF MCLK	R23h	Master clock input or output signal for the S/PDIF interface
ADAT MCLK	R26h	Master clock input or output signal for the ADAT interface
Sound Card MCLK	R27h	Clock input signal to the Sound Card hardware on underside of Lochnagar 2

4.3.2 List of Clock Sources

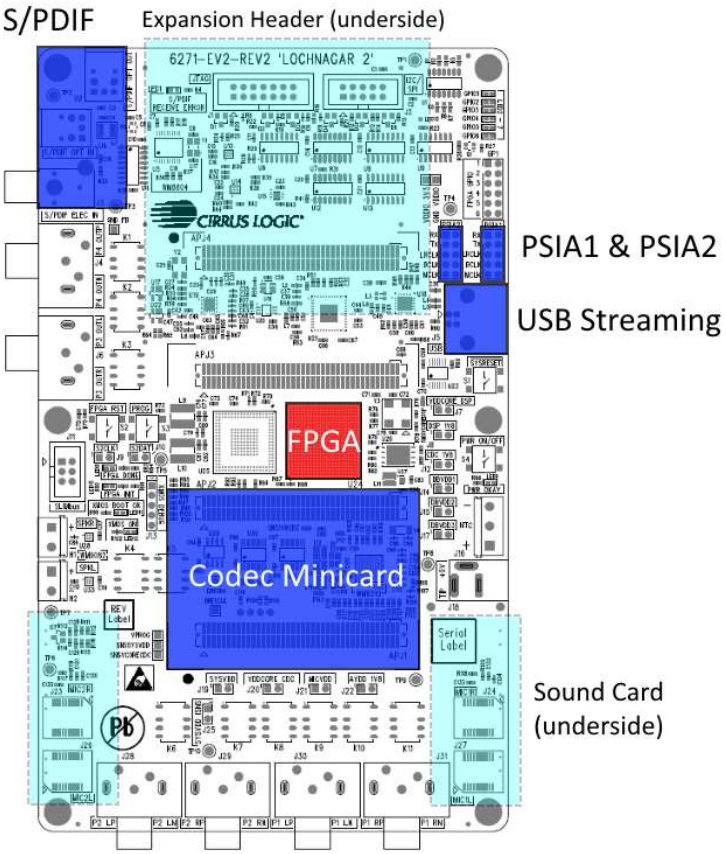
This lists all the potential sources of clock signals that can be routed to the clock sinks listed in the table above. The binary values for these sources are provided for advanced users.

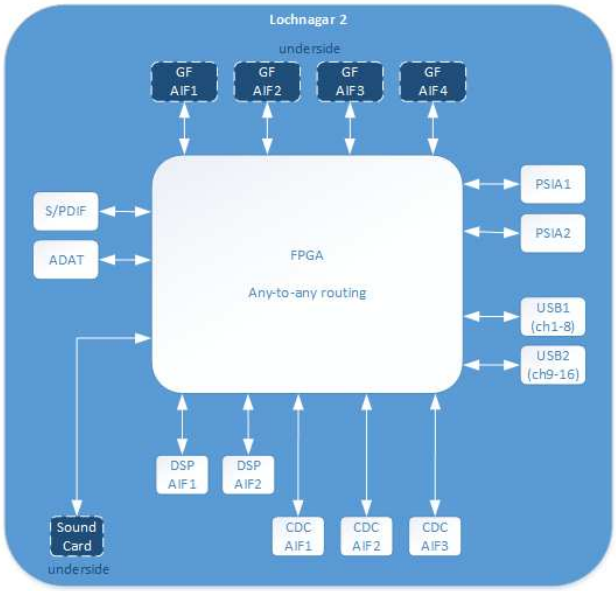
Clock Source	Binary Value	Description
None	0x00	No clock source selected
Codec Clock Out	0x01	Clock output signal generated by the codec
DSP Clock Out	0x02	Clock output signal generated on the DSP minicard
PMIC 32K	0x03	32.578 kHz clock generated by the onboard power management IC
SPDIF MCLK	0x04	Use this clock input for S/PDIF audio use cases Clock output from the S/PDIF receiver chip. Frequency will depend upon sampling rate of SP/DIF audio. With no S/PDIF signal applied, the chip generates a default of 12.0 MHz
Clock: 12.288 MHz	0x05	Fixed 12.288 MHz (48k multiple) clock from onboard clock generator chip.
Clock: 11.2986 MHz	0x06	Fixed 11.2986 MHz (44.1k multiple) clock from onboard clock generator chip.
Clock: 24.576 MHz	0x07	Fixed 24.576 MHz (48k multiple) clock from onboard clock generator chip.
Clock: 22.5792 MHz	0x08	Fixed 22.5792 MHz (44.1k multiple) clock from onboard clock generator chip.
USB MCLK: 12.288 MHz (11.2986 MHz)	0x0A	Use this clock input for USB streaming use cases Half rate clock that is synchronous to USB audio data. Frequency will depend on the sampling rate of audio being transferred over USB This will be either 12.288 MHz or 11.2986 MHz
USB MCLK: 24.576 MHz (22.5792 MHz)	0x12	Use this clock input for USB streaming use cases Full rate clock that is synchronous to USB audio data. Frequency will depend on the sampling rate of audio being transferred over USB This will be either 24.576 MHz or 22.5792 MHz
GF MCLK1	0x0B	Clock signal from the expansion headers on underside. Usually used when connected to Linux Application Processor systems
GF MCLK2	0x0D	Clock signal from the expansion headers on underside. Usually used when connected to Linux Application Processor systems
GF MCLK3	0x0C	Clock signal from the expansion headers on underside. Usually used when connected to Linux Application Processor systems
PSIA1 MCLK	0x0E	Clock signal applied to PSIA1 headers (3.3V I2S pin headers)
PSIA2 MCLK	0x0F	Clock signal applied to PSIA2 headers (3.3V I2S pin headers)
SPDIF Clockout	0x10	Seconary clock output signal from the S/PDIF receiver chip. For advanced use cases only.
ADAT MCLK	0x11	Clock signal from the ADAT receiver when used in ADAT mode.

5 Digital Audio

This section details the digital audio inputs and outputs on the Lochnagar 2 board, and how to configure the routing. Any digital audio interface (AIF) on the Lochnagar 2 system can be connected to any other via the flexible routing of the FPGA.

5.1 Digital Audio Connection Diagrams

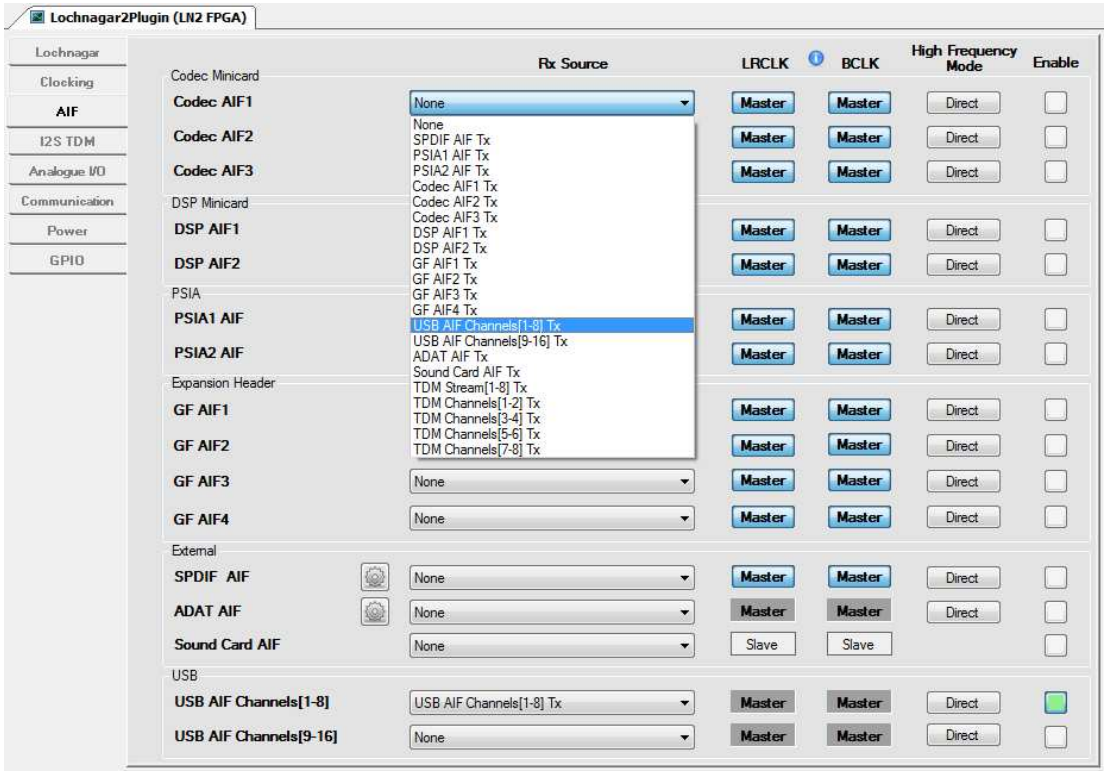




5.2 Configuring Digital Audio Routing

Digital audio signals on Lochnagar 2 are routed through the central FPGA and can connect any AIF port to any other AIF port on the board.

Routing is controlled via the **AIF** panel of the Lochnagar 2 plugin.



5.2.1 BCLK / LRCLK Routing Operation

The **Rx Source** drop-down menu selects where the audio data comes from for the AIF sink on that row.

If **BCLK/LRCLK** are set to **Slave**, the Lochnagar 2 Board will supply the clocks from audio interface selected in the **Rx Source** selection.
If **BCLK/LRCLK** are set to **Master**, the Lochnagar 2 will not provide any clocks outputs to the AIF sink. The pins will be put into high-Z mode and used as inputs.

Clocks in Slave Mode

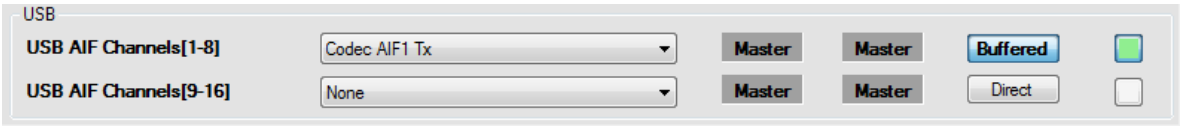
If BCLK and/or LRCLK for an AIF device are set to "Slave" mode, the Rx Source should not be set to "None", as this will mean that no clocks are provided to the AIF Slave device.

5.2.2 High Frequency Mode

Path delays in AIF systems can cause problems when the round trip delay between the AIF master and slave devices is comparable to the period of the BCLK signal. In these scenarios, the return data received by the slave may be corrupted.

Lochnagar 2 provides a buffered "High Frequency Mode" setting that will compensate for long round trip delays by introducing a single audio frame of buffering into the AIF master return data.

Typically, this is required when the BCLK signal is higher than 12.288 MHz (from USB AIF, this will typically be for 96 kHz or 192 kHz sampling rates), but depending on the exact audio routing setup on the Lochnagar 2 board, it may also be required at lower BCLK rates. This is also required to compensate for minicards that have long PCB tracks or cabling between the Lochnagar 2 and the DUT.



The High Frequency Mode setting is only available on AIF peripherals where both BCLK and LRCLK are configured as AIF master.

There are two potential settings:

- Direct Mode = No buffering or delay is added onto this AIF signal by the Lochnagar 2 board
- Buffered Mode = A single audio frame of delay is introduced to the data received by this AIF master from the Rx Source.

Direct Mode is the default setting as it provides the lowest possible latency through the system.
If audio corruption is observed at the AIF master, it is possible to resolve this by enabling the "Buffered" High Frequency Mode setting.

5.2.3 Example Configuration

To set up an AIF connection between the USB audio streaming and Codec AIF1 port:

1. Find the Codec AIF1 row on the **AIF** tab of the Lochnagar 2 plugin.
2. Select a Rx Source for this audio connection. Choose USB AIF Channels[1-8] Tx to connect it to the USB streaming peripheral.
3. Select whether Codec AIF1 is master or slave for the BCLK and LRCLK. Since USB streaming operates as master only, they must both be set to Slave in this example.
4. If audio is required in both directions, find the row for USB AIF Channels[1-8], and set the Rx Source to Codec AIF1 Tx. This will make the audio bidirectional.
5. If required, select the Buffered High Frequency Mode on the USB AIF Channels[1-8] row to add optional buffering into the return path. This may be required if the return data from the codec is corrupted due to path length delays.
6. Enable both interfaces using the buttons on the right of each row.

It is also important to make sure that the codec has an MCLK that is connected to a synchronous clock source.
In this scenario, the **Clocking** panel of the plugin should be used to set MCLK1 or MCLK2 to the USB MCLK.

5.2.4 Advanced Clocking Configurations

Audio paths do not need to be set up directly between two AIF interfaces, and BCLK/LRCLK do not necessarily have to be driven by the same master or in the same direction, assuming that the Slave device also supports that mode. A single AIF master could potentially clock multiple slave devices by daisy-chaining the audio from one slave AIF port to the next.

This flexibility means that the Lochnagar 2 can be set up to emulate almost any potential AIF configuration in order to develop solutions or replicate problems.

Note that there is no protection for scenarios where the FPGA is configured incorrectly, so it is also important to make sure that the AIF interface connected to the FPGA is configured in the appropriate manner. If Codec AIF1 is set up as a Master on the DUT and also in the FPGA, the two devices will drive against each other on the line and potentially create mid-rail voltages.

5.3 AIF interfaces on codec minicard

The codec minicard supports up to three AIF interfaces (for smaller cards with two connectors) or five AIF interfaces (for larger cards that span over three connectors).

5.4 AIF interfaces on the expansion headers

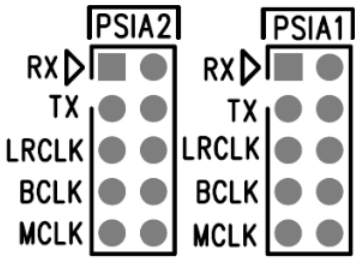
The expansion headers on the underside of Lochnagar 2 are designed to connect Lochnagar 2 to Linux Application Processor systems. The headers on the underside support up to four AIF interfaces.

5.5 PSIA Headers

These headers are designed to connect to Audio Precision testing equipment through the PSIA (Programmable Serial Interface Adapter) hardware.

This is essentially a standard I2S-based digital audio interface with 3.3V signal levels, consisting of the following signals:

The silkscreen markings on Lochnagar 2 will help the user determine which pin is which. Note that TX and RX directions are with respect to the external PSIA hardware, therefore the pin marked "RX" is an output from the FPGA.



- RXDAT (pin 1)
- TXDAT (pin 3)
- LRCLK (pin 5)
- BCLK (pin 7)
- MCLK (pin 9)
- Ground signals (pins 2, 4, 6, 8, 10)

Clocking

When using the PSIA with a Cirrus codec device, the codec can be used as either AIF clock master or clock slave.
The **Clocking** panel of the Lochnagar 2 Plugin should be used to configure the MCLKs of the codec and PSIA ports appropriately.