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WM9081

Mono DAC with 2.6W Class AB/D Speaker Driver, Dynamic Range Controller and ReTune™ Mobile Parametric Equalizer

DESCRIPTION

The WM9081 is designed to provide high power output at low distortion levels in space-constrained portable applications.

ReTune™ Mobile Parametric EQ with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop.

Digital input enables the power drivers to be located close to the speakers in multi-channel systems without the need for troublesome long analogue connections. Location of the power drivers close to the speakers also removes the need for bulky and expensive class D filters and reduces PCB track lengths, minimising emissions. The digital input can also help to minimise crosstalk to the speaker output signal from high gain microphone inputs, enhancing stability and reducing the risk of 'howling' during speakerphone operation.

Four control interface addresses and four-channel TDM are supported to allow multiple devices to be configured and driven independently.

The device is controlled via a standard 2-wire, 3-wire, or 4-wire control interface or by hardware control pins.

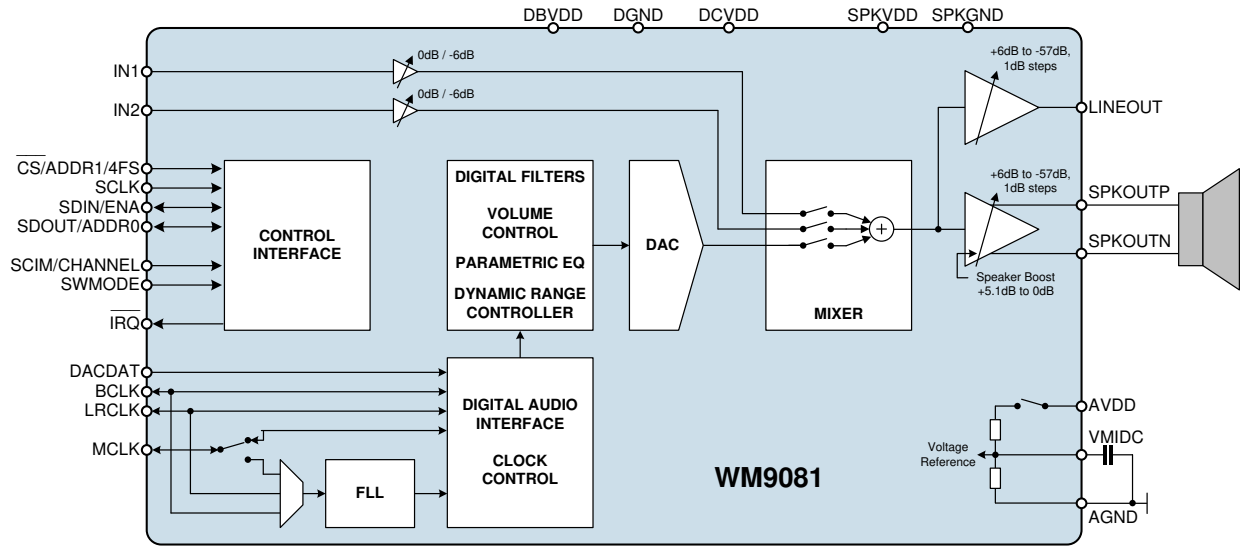
FEATURES

- High-power, high performance DAC and speaker driver
  - 92dB SNR ('A-weighted') in Class D mode
  - 97dB SNR ('A-weighted') in Class AB mode
  - <0.05% THD+N @0.5W continuous into 4Ω (Class D)
  - <0.10% THD+N @2W continuous into 4Ω (Class D)
  - 2.6W maximum peak power
- ReTune™ Mobile Parametric Equalizer
  - Fully programmable filter coefficients
- Programmable dynamic range controller
  - Boosts small signals to maximise loudness
  - Protects against battery droop and clipping
- Speaker common mode boost
  - Maximises power for a given SPKVDD/AVDD ratio
- Low power FLL
  - Provides all necessary internal clocks
  - 32kHz to 27MHz input frequency
- All common sample rates from 8kHz to 96kHz supported
- Standard 2-wire, 3-wire, 4-wire and hardware control modes
- Data formats: LJ, RJ, I^2S, DSP, all with TDM support
- Thermal shutdown interrupt
- 4x4 COL package (0.45mm lead pitch)
- Operating temperature range: -40°C to 85°C

APPLICATIONS

- Portable navigation systems
- Mobile phones
- Flat panel TVs

BLOCK DIAGRAM



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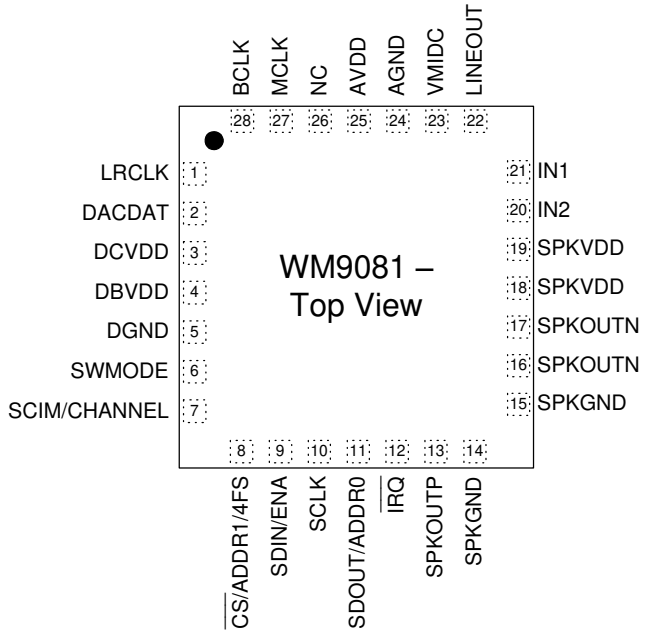
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM9081GICN/V	-40°C to +85°C	28-lead COL (4x4x0.55mm) (Pb-free)	MSL3	260°C
WM9081GICN/RV	-40°C to +85°C	28-lead COL (4x4x0.55mm) (Pb-free, Tape and reel)	MSL3	260°C

Note:
Reel quantity = 3500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	LRCLK	Digital Input / Output	Audio interface DAC left / right clock
2	DACDAT	Digital Input	DAC digital audio data
3	DCVDD	Supply	Digital core supply
4	DBVDD	Supply	Digital buffer (I/O) supply
5	DGND	Supply	Digital ground (Return path for both DCVDD and DBVDD)
6	SWMODE	Digital Input	Selects hardware or software control mode
7	SCIM/CHANNEL	Digital Input	2-wire or 3-wire control select (Software mode) / Left / right data channel select (Hardware mode)
8	$\overline{CS}$/ADDR1/4FS	Digital Input	3-wire chip select or 2-wire address select (Software mode) / Normal fs input or 4fs input select (Hardware mode)
9	SDIN/ENA	Digital Input / Output	Control interface data input (Software mode) / Device enable (Hardware mode)
10	SCLK	Digital Input	Control interface clock input (Software mode)
11	SDOUT/ADDR0	Digital Input/ Output	4-wire data output or 2-wire address select (Software mode)
12	$\overline{IRQ}$	Digital Output	Interrupt signal
13	SPKOUTP	Analogue Output	Positive BTL speaker output
14	SPKGND	Supply	Speaker ground (1) (Return path for SPKVDD)
15	SPKGND	Supply	Speaker ground (2) (Return path for SPKVDD)
16	SPKOUTN	Analogue Output	Negative BTL speaker output (1)
17	SPKOUTN	Analogue Output	Negative BTL speaker output (2)
18	SPKVDD	Supply	Speaker supply (1)
19	SPKVDD	Supply	Speaker supply (2)
20	IN2	Analogue Input	Line input
21	IN1	Analogue Input	Line input
22	LINEOUT	Analogue Output	Line output
23	VMIDC	Reference	Mid-rail voltage (VMID) decoupling connection
24	AGND	Supply	Analogue ground (Return path for AVDD)
25	AVDD	Supply	Analogue supply
26	NC		Not connected
27	MCLK	Digital Input / Output	Master clock
28	BCLK	Digital Input / Output	Audio interface bit clock

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (excluding SPKVDD)	-0.3V	+4.5V
SPKVDD	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Junction temperature, T_J	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

Notes

1. Analogue, digital and speaker grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.71	1.8	3.6	V
Digital supply range (Buffer)	DBVDD	1.71	1.8	3.6	V
Analogue supplies range	AVDD	2.7	3.3	3.6	V
Speaker supply range	SPKVDD	2.7	5.0	5.5	V
Ground	DGND, AGND, SPKGND		0		V
Ambient temperature, T_A		-40		+85	ºC
Junction temperature, T_J		-40		+125	ºC

Notes

1. All digital and analogue supplies are completely independent from each other (i.e. not internally connected).
2. DCVDD must be less than or equal to AVDD.
3. DCVDD must be less than or equal to DBVDD.
4. AVDD must be less than or equal to SPKVDD.
5. SPKVDD must be high enough to support the peak output voltage when using DCGAIN and ACGAIN functions, to avoid output waveform clipping.
6. Junction temperature is a function of ambient temperature and of the device operating conditions. The ambient temperature limits and the junction temperature limits must both be observed.

ELECTRICAL CHARACTERISTICS

COMMON TEST CONDITIONS

Unless otherwise stated, the following test conditions apply throughout the following sections:

- DCVDD = DBVDD = 1.8V, AVDD = 3.3V, SPKVDD = 5.0V
- PGA gain = 0dB
- ACGAIN=DCGAIN=1.52
- Audio signal: 1kHz sine wave, sampled at 48kHz with 24-bit data resolution, I^2S mode
- Ambient temperature: T_A = +25°C
- C_{VMID} = 4.7µF
- VMID_SEL[1:0] = 01 (2x40kΩ)

Additional, specific test conditions are given within the relevant sections below.

AUDIO DAC

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum theoretical full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.
4. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
5. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.

DAC TO SPEAKER OUTPUT

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Speaker Output (4.1Ω + 22µH BTL Load)					
SNR (A-weighted)	DAC to speaker output, class D	85	92		dB
THD+N (P_O=0.5W)			-72		dB
THD+N (P_O=1.0W)			-72		dB
THD+N (P_O=2.0W)			-68	-50	dB
SNR (A-weighted)	DAC to speaker output, class AB	90	97		dB
THD+N (P_O=0.5W)			-86		dB
THD+N (P_O=1.0W)			-86		dB
THD+N (P_O=2.0W)			-80	-50	dB

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Rejection (20Hz – 20kHz)					
SPKVDD PSRR	400mV pk-pk at 217Hz on SPKVDD; DAC to speaker output, class D		75		dB
	400mV pk-pk at 217Hz on SPKVDD; DAC to speaker output, class AB		85		dB
AVDD PSRR	100mV pk-pk at 217Hz on AVDD; DAC to speaker output, class D		60		dB
	100mV pk-pk at 217Hz on AVDD; DAC to speaker output, class AB		60		dB

DAC TO LINE OUTPUT

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Line Output (10kΩ / 50pF Load)					
SNR (A-weighted)	DAC to line out, 0dBFS input	90	99		dB
THD+N			-83	-75	dB
Power Supply Rejection					
AVDD PSRR	100mV pk-pk at 217Hz on AVDD; DAC to line output		50		dB

OUTPUT CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Speaker Load Resistance		4			Ω
Line Out Load Resistance		5	10	100	kΩ
Line Out Capacitance				2	nF
Maximum Continuous Speaker Output Power	Class D mode		2		W
	Class AB mode		2		W
Maximum Peak Speaker Output Power	Class D mode		2.6		W
	Class AB mode		2.6		W
SPKVDD Leakage Current	SPKVDD = 5.0V		0.15	1	µA
Line Output Programmable Gain Amplifier					
Minimum Gain			-57		dB
Maximum Gain			+6		dB
Gain Step Size			1		dB
Mute Attenuation		80	92		dB
Speaker Output Programmable Gain Amplifier					
Minimum Gain			-57		dB
Maximum Gain			+6		dB
Gain Step Size			1		dB
Mute Attenuation		80	92		dB
DAC Digital					
DAC maximum volume			0		dB
DAC minimum volume			-71.625		dB
DAC volume step size			0.375		dB
DAC soft mute time (Note: Scales linearly with sample rate) 0dBFS to mute	DAC_MUTERATE = 0		10.7		ms
	DAC_MUTERATE = 1		171		ms

ANALOGUE REFERENCE LEVELS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	EV
Reference Voltages					
VMID Midrail Reference Voltage		-3%	AVDD/2	+3%	V

ANALOGUE INPUTS (IN1, IN2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Input Signal Level				AVDD/3.3	Vrms
IN1 Input resistance	0dB PGA gain		25		kΩ
	-6dB PGA gain		50		kΩ
IN2 Input resistance	0dB PGA gain		25		kΩ
	-6dB PGA gain		50		kΩ

DIGITAL INTERFACES

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output					
Input HIGH Level		0.7× DBVDD			V
Input LOW Level				0.3× DBVDD	V
Output HIGH Level	I_{OL}=1mA	0.9× DBVDD			V
Output LOW Level	I_{OH}=-1mA			0.1× DBVDD	V
Input Capacitance			10		pF
Input Leakage		-0.5		0.5	µA

CLOCKING AND TIMING

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLL					
Input Frequency		8kHz		27MHz	
Lock time				TBA	Reference Clock Periods
MCLK					
Input Frequency				25.000	MHz
CLK_SYS					
Frequency				12.500	MHz
Power-up and Power-down Sequences					
Power-up Time	Hardware mode		42		ms
	Software mode		42		ms
Power-down Time	Hardware mode		48		ms
	Software mode		48		ms

TYPICAL POWER CONSUMPTION

The WM9081 power consumption is dependent on many parameters. Most significantly, it depends on supply voltages, sample rates, mode of operation, and output loading.

The power consumption on each supply rail varies approximately with the square of the voltage. Power consumption is greater at fast sample rates than at slower ones. When the digital audio interface is operating in Master mode, the DBVDD current is significantly greater than in Slave mode. The output load conditions (impedance, capacitance and inductance) can also impact significantly on the device power consumption.

COMMON TEST CONDITIONS

Unless otherwise stated, the following test conditions apply throughout the following sections:

- Ambient temperature = +25°C
- Audio signal = quiescent (zero amplitude)
- Sample rate = 48kHz
- MCLK = 12.288MHz
- Audio interface mode = slave
- Control mode: software

Additional, variant test conditions are quoted within the relevant sections below. Where applicable, power dissipated in the speaker or line loads is included.

POWER CONSUMPTION MEASUREMENTS

Off and Standby modes

Test conditions:

- No clocks applied unless stated
- No signal applied unless stated

Variant test conditions	AVDD		DCVDD		DBVDD		SPKVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	mW
Off (default settings)	3.3	0.05	1.8	0.01	1.8	0.01	5.0	0.00	0.18
Off (default settings), DACDAT, MCLK, BCLK and LRCLK applied	3.3	0.05	1.8	0.01	1.8	0.01	5.0	0.00	0.18
Off (lowest power settings)	3.3	0.01	1.8	0.00	1.8	0.00	5.0	0.00	0.03

DAC to Speaker Playback - DAC input to SPKOUTP/SPKOUTN pins with 4.1Ω + 22µH load.

Test conditions:

- Slave mode, MCLK = 12.288MHz, LRCLK = 48kHz
- Input signal: 0dBFS 1kHz sine wave

Variant test conditions	AVDD		DCVDD		DBVDD		SPKVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	mW
DAC to Class D Speaker Playback no signal	3.3	2.7	1.8	1.3	1.8	0.0	5.0	2.7	24.9
DAC to Class D Speaker Playback 0.5W	3.3	2.8	1.8	1.4	1.8	0.0	5.0	120.0	611.7
DAC to Class D Speaker Playback 1.0W	3.3	2.8	1.8	1.4	1.8	0.0	5.0	225.0	1136.7
DAC to Class D Speaker Playback 2.0W	3.3	2.8	1.8	1.4	1.8	0.0	5.0	435.0	2186.7

DAC to Lineout Playback - DAC input to LINEOUT pin with 10kΩ load.

Test conditions:

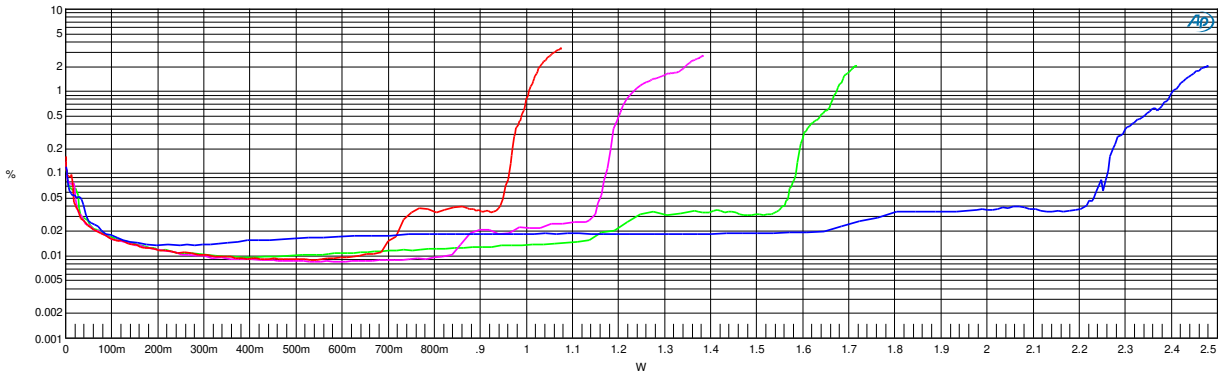
- Slave mode, MCLK = 12.288MHz, LRCLK = 48kHz
- Input signal: 0dBFS 1kHz sine wave

Variant test conditions	AVDD		DCVDD		DBVDD		SPKVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	mW
DAC to LINEOUT, no input signal	3.3	1.9	1.8	1.3	1.8	0.0	5.0	0.0	8.5
DAC to LINEOUT, 0dBFS input signal	3.3	1.9	1.8	1.4	1.8	0.0	5.0	0.0	9.0

TYPICAL PERFORMANCE DATA

Typical speaker driver THD+N performance is shown below for both 8Ω and 4Ω loads in Class D mode. Curves are shown for four typical SPKVDD supply voltage and gain combinations.

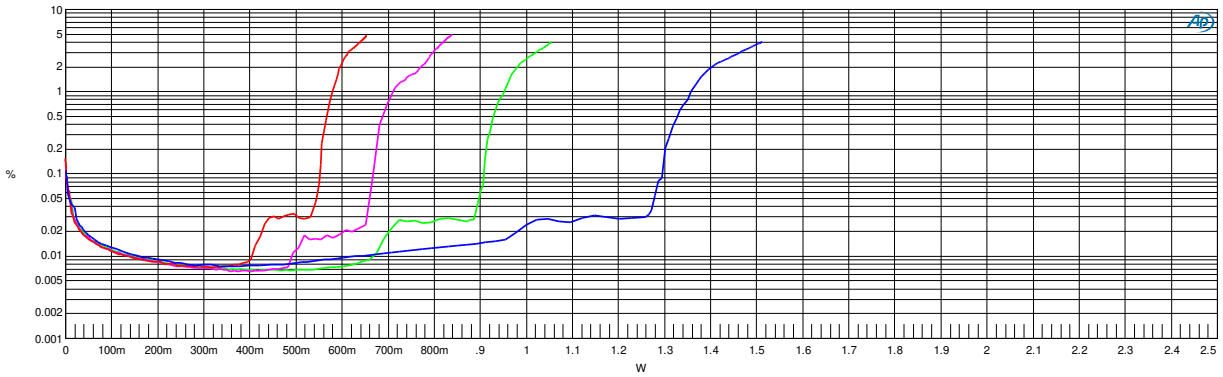
SPEAKER CLASS D INTO 4Ω + 10µH



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	2	Anlr.THD+N Ratio	Left	SPKVDD = 5.0V, AVDD = 3.3V, DCGAIN = ACGAIN = 3.6dB
2	1	Green	Solid	2	Anlr.THD+N Ratio	Left	SPKVDD = 4.2V, AVDD = 3.3V, DCGAIN = ACGAIN = 2.1dB
3	1	Magenta	Solid	2	Anlr.THD+N Ratio	Left	SPKVDD = 3.7V, AVDD = 3.0V, DCGAIN = ACGAIN = 2.1dB
4	1	Red	Solid	2	Anlr.THD+N Ratio	Left	SPKVDD = 3.3V, AVDD = 3.3V, DCGAIN = ACGAIN = 0dB

Device: WM9081 MMC=WPF
Input Signal: 1KHz; 0dBFS; 24-bit; 256fs (fs=48kHz)
Output Path: SPK Class D
Supplies: DBVDD=DCVDD=3.3V
BW Filter: 22Hz to 20kHz AES17
Additional Filtering: none
Load = 4R1 + 10uH

SPEAKER CLASS D INTO 8Ω + 10µH



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	2	Anlr.THD+N Ratio	Left	SPKVDD = 5.0V, AVDD = 3.3V, DCGAIN = ACGAIN = 3.6dB
2	1	Green	Solid	2	Anlr.THD+N Ratio	Left	SPKVDD = 4.2V, AVDD = 3.3V, DCGAIN = ACGAIN = 2.1dB
3	1	Magenta	Solid	2	Anlr.THD+N Ratio	Left	SPKVDD = 3.7V, AVDD = 3.0V, DCGAIN = ACGAIN = 2.1dB
4	1	Red	Solid	2	Anlr.THD+N Ratio	Left	SPKVDD = 3.3V, AVDD = 3.3V, DCGAIN = ACGAIN = 0dB

Device: WM9081 MMC=WPF
Input Signal: 1KHz; 0dBFS; 24-bit; 256fs (fs=48kHz)
Output Path: SPK Class D
Supplies: DBVDD=DCVDD=3.3V
BW Filter: 22Hz to 20kHz AES17
Additional Filtering: none
Load = 8R2 + 10uH

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

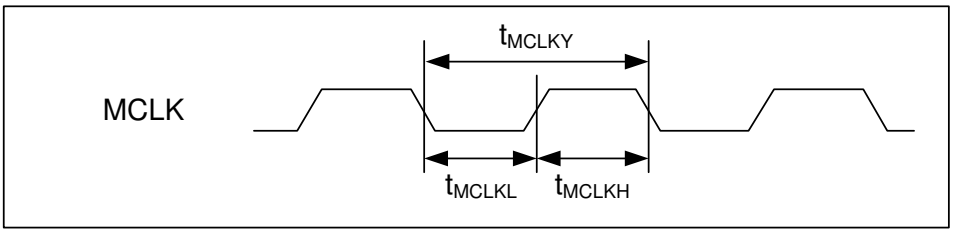


Figure 1 System Clock Timing Requirements

Test Conditions

DCVDD=DBVDD=1.8V, AVDD=3.3V, SPKVDD=5V, DGND=AGND=SPKGND=0V, T_A = +25ºC

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK cycle time	T_{MCLKY}		40			ns
MCLK duty cycle		= T_{MCLKH}/T_{MCLKL}	60:40		40:60	

AUDIO INTERFACE TIMING – MASTER MODE

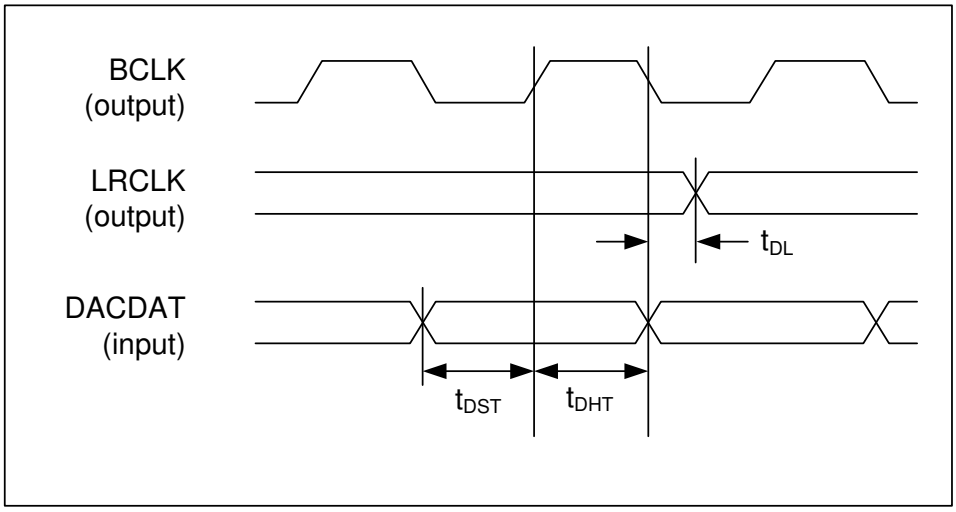


Figure 2 Digital Audio Data Timing - Master Mode

Test Conditions

DCVDD=DBVDD=1.8V, AVDD=3.3V, SPKVDD=5V, DGND=AGND=SPKGND=0V, T_A=+25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Timing Information					
LRCLK propagation delay from BCLK falling edge	t_{DL}			10	ns
DACDAT setup time to BCLK rising edge	t_{DST}	10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

AUDIO INTERFACE TIMING – SLAVE MODE

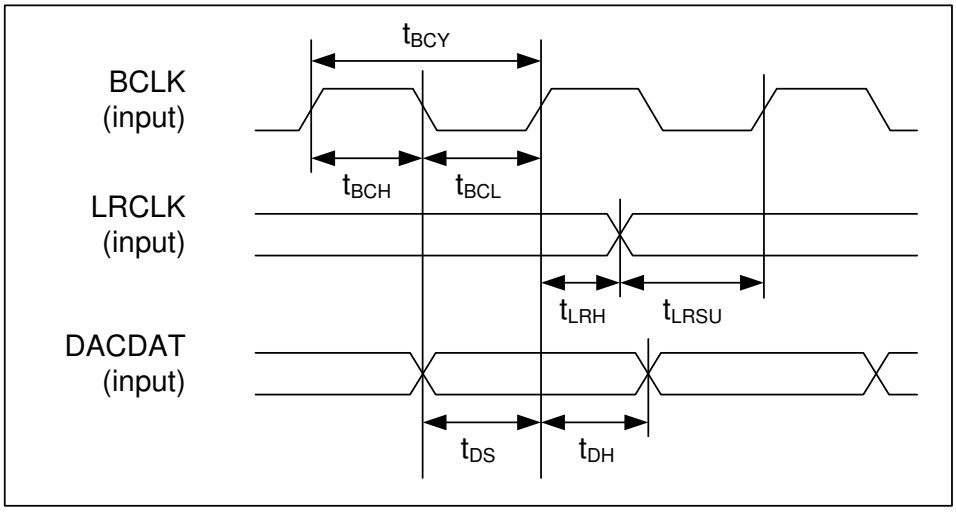


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD=DBVDD=1.8V, AVDD=3.3V, SPKVDD=5V, DGND=AGND=SPKGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	80			ns
BCLK pulse width high	t_{BCH}	40			ns
BCLK pulse width low	t_{BCL}	40			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	10			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
DACDAT set-up time to BCLK rising edge	t_{DS}	10			ns

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – 2-WIRE MODE

2-wire mode is selected by connecting the SWMODE pin high and connecting the SCIM_CHANNEL pin low.

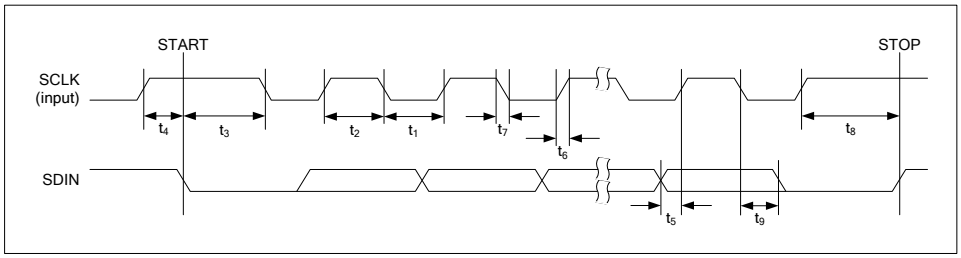


Figure 4 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD=DBVDD=1.8V, AVDD= 3.3V, SPKVDD=5V, DGND=AGND= SPKGND=0V, T_A=+25ºC, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency				526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

CONTROL INTERFACE TIMING – 3-WIRE MODE

3-wire mode is selected by connecting the SWMODE pin high and connecting the SCIM_CHANNEL pin high.

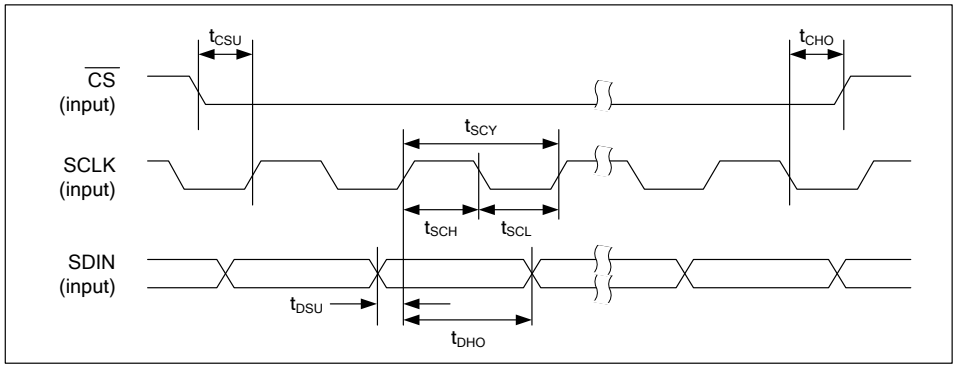


Figure 5 Control Interface Timing – 3-Wire Serial Control Mode (Write Cycle)

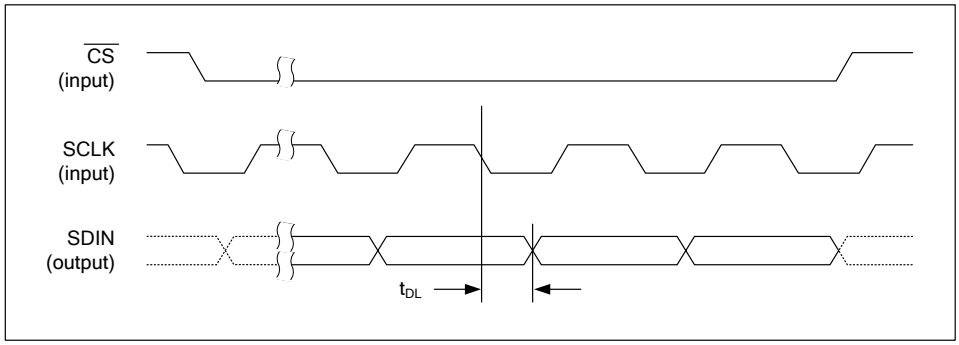


Figure 6 Control Interface Timing – 3-Wire Serial Control Mode (Read Cycle)

Test Conditions

DCVDD=DBVDD=1.8V, AVDD= 3.3V, SPKVDD=5V, DGND=AGND=SPKGND=0V, T_A=+25ºC, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
CSB falling edge to SCLK rising edge	t_{CSU}	40			ns
SCLK rising edge to CSB rising edge	t_{CHO}	10			ns
SCLK pulse cycle time	t_{SCY}	160			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SDIN to SCLK hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDOUT transition	t_{DL}			40	ns

CONTROL INTERFACE TIMING – 4-WIRE MODE

4-wire mode supports readback via SDOUT.

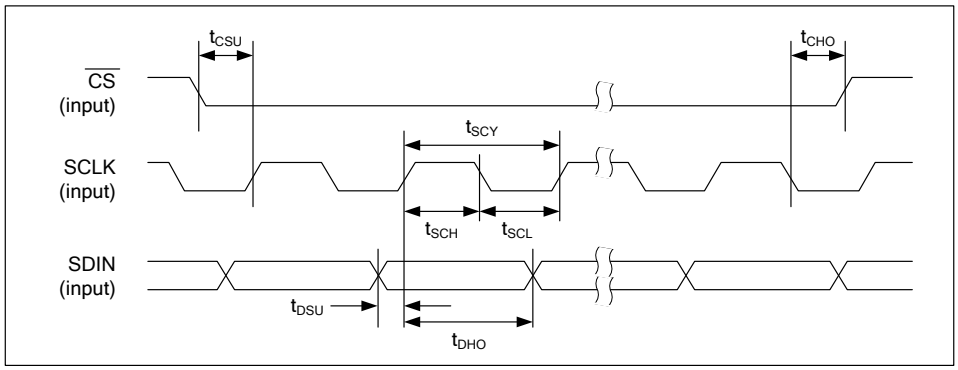


Figure 7 Control Interface Timing – 4-Wire Serial Control Mode (Write Cycle)

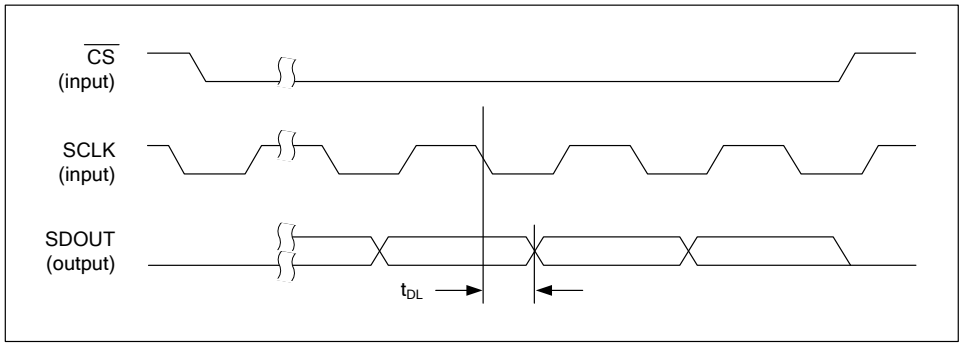


Figure 8 Control Interface Timing – 4-Wire Serial Control Mode (Read Cycle)

Test Conditions

DCVDD=DBVDD=1.8V, AVDD= 3.3V, SPKVDD=5V, DGND=AGND=SPKGND=0V, T_A =+25ºC, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB falling edge	t_{CSU}	40			ns
SCLK rising edge to CSB rising edge	t_{SHO}	40			ns
SCLK pulse cycle time	t_{SCY}	160			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SDIN to SCLK hold time	t_{DHO}	10			ns
SDOUT propagation delay from SCLK rising edge	t_{DL}			10	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDOUT transition	t_{DL}			40	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM9081 is designed to provide high quality, high power output to a loudspeaker at low distortion levels in space-constrained portable applications. The device is well-suited to both mono and multi-channel speaker systems.

Digital input enables the power drivers to be located close to the speakers in multi-channel systems without the need for troublesome long analogue connections. Location of the power drivers close to the speakers also removes the need for bulky and expensive class D filters and reduces PCB track lengths, minimising emissions.

The WM9081 supports both hardware and software control modes.

In Hardware control modes, the digital audio interface format is fixed and either the left or right channel can be routed to the Class D speaker driver. The WM9081 is a slave device only on the audio interface; EQ and Dynamic Range Control functions are not supported.

In Software control modes, the digital audio interface is highly programmable. Ready-programmed control sequences can be commanded to enable/disable the speaker driver or line output. Programmable EQ and Dynamic Range Control is supported in the digital domain. Analogue audio input paths can also be mixed into the speaker or line output drivers. The speaker driver can be configured to operate either in Class AB or in Class D mode.

ReTune™ Mobile parametric EQ with fully programmable coefficients is integrated for optimization of speaker characteristics. A simple set-up mode is also available.

A programmable dynamic range controller is also available for maximizing loudness whilst also protecting speakers from being overdriven, preventing battery droop, waveform clipping, thermal overloads and premature system shutdown.

Figure 9 shows the DAC signal path and clocking architecture of the WM9081.

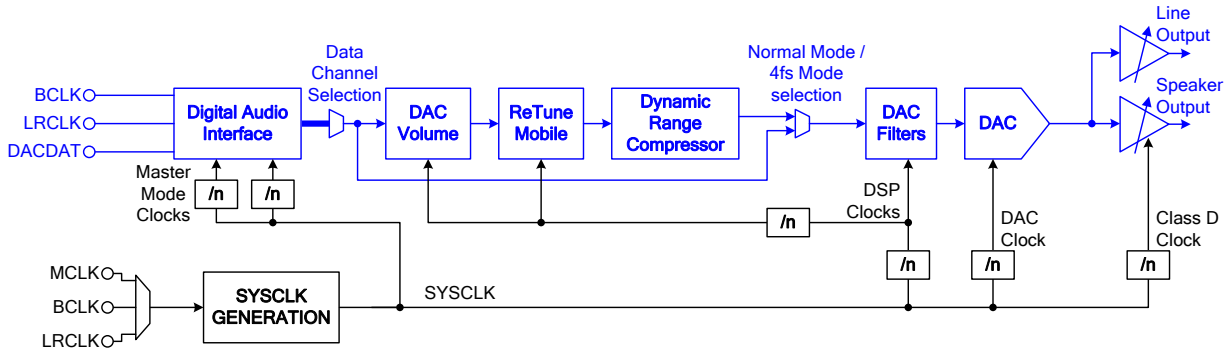


Figure 9 DAC Signal Path and Clocking Architecture

Digital audio transmission within the system also reduces crosstalk between, for example, microphone input signals and speaker output signals, enhancing stability and reducing the risk of 'howling' during speakerphone operation where very high microphone gain is used.

Four control interface addresses and four stereo TDM slots are supported to allow multiple WM9081 devices to be configured and driven independently.

CONTROL INTERFACE (SOFTWARE MODE)

The WM9081 can be controlled in hardware mode or in software modes. In hardware mode, the device is configured according to logic levels applied to hardware pins. In software mode, the device is configured using control register writes via a serial control interface. See “Control Interface (Hardware Mode)” for details of hardware control mode.

Software Control Mode is selected by logic 1 on the SWMODE pin. The logic level is referenced to the DBVDD power domain. When Software Mode is selected, the associated multi-function control pins are defined as described in Table 1.

PIN	DESCRIPTION
SCIM/CHANNEL	Software Control Interface Mode 0 = 2-wire 1 = 3-/4-wire
SDIN/ENA	Serial Data Input
SCLK	Serial Data Clock
SDOUT/ADDR0	2 wire mode - Device Address[0] 3-wire mode - Not used 4-wire mode - Serial Data Output
CS /ADDR1/4FS	2 wire mode - Device Address[1] 3-/4-wire mode - Chip Select

Table 1 Software Control Pin Configuration

A typical system configuration for software control mode is illustrated in Figure 10.

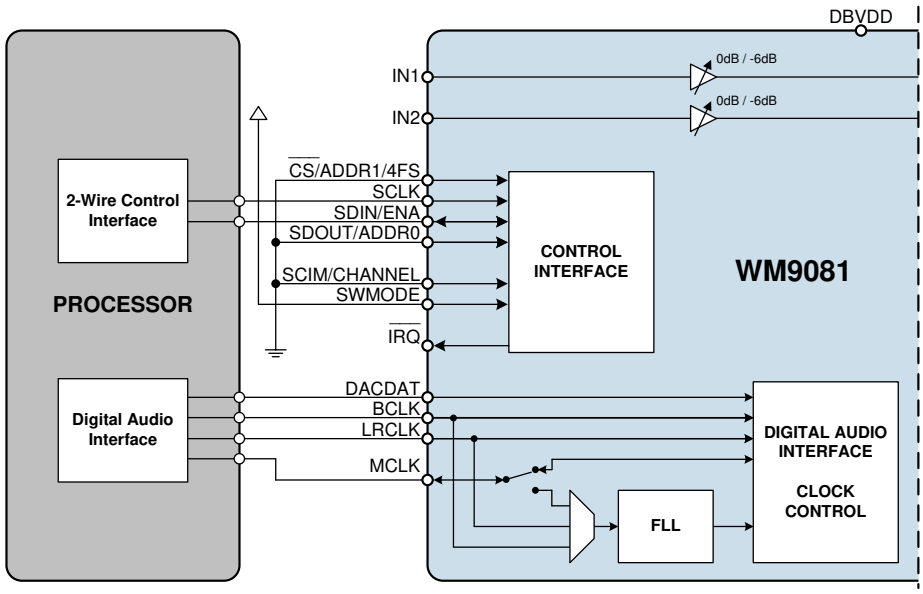


Figure 10 Software Control Mode Example – 2-Wire Control, Slave Mode, Device ID = D8h

In Software Control Mode, the WM9081 is controlled by writing to its control registers. Readback is available for all registers, including device ID and power management status bits. The control interface can operate as a 2-, 3- or 4-wire control interface: Readback is provided on the bi-directional pin SDIN in 2-wire and 3-wire modes. The WM9081 Software Control interface is supplied by the DBVDD power domain.

The available Software Control interface modes are summarised as follows:

- 2-wire mode uses pins SCLK and SDIN.
- 3-wire mode uses pins CS, SCLK and SDIN.
- 4-wire mode uses pins CS, SCLK, SDIN and SDOUT.

2-wire mode is selected by setting the SCIM/CHANNEL pin to logic 0. When this pin is set to logic 1, then 3-wire or 4-wire mode is selected according to the SPI_4WIRE register bit, as defined in Table 2.

In 4-wire mode, the electrical characteristics of the SDOUT pin are configurable using the SPI_CFG register bit.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) MW Slave 1	5	SPI_CFG	0	Controls the SDOUT pin in 4 wire mode 0 = SDOUT output is CMOS 1 = SDOUT output is open drain
	4	SPI_4WIRE	0	Selects 3-wire or 4-wire mode 0 = 3-wire mode using bi-directional SDIN pin 1 = 4-wire mode using SDOUT

Table 2 Software Control Mode Configuration

2-WIRE CONTROL MODE

In 2-wire mode, the WM9081 is a slave device on the control interface; SCLK is a clock input, while SDIN is a bi-directional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the WM9081 transmits logic 1 by tri-stating the SDIN pin, rather than pulling it high. An external pull-up resistor is required to pull the SDIN line high so that the logic 1 can be recognised by the master.

In order to allow many devices to share a single 2-wire control bus, every device on the bus has a unique 7-bit device ID (this is not the same as the 8-bit address of each register in the WM9081). The device ID is determined by the logic level on the ADDR0 and ADDR1 pins as shown in Table 3. The LSB of the device ID is the Read/Write bit; this bit is set to logic 1 for “Read” and logic 0 for “Write”.

ADDR1	ADDR0	DEVICE ID
0	0	1101 1000 (D8h)
0	1	1101 1010 (DAh)
1	0	1101 1100 (DCh)
1	1	1101 1110 (DEh)

Table 3 Control Interface Device ID Selection

The WM9081 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device ID, register address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit device ID + Read/Write bit, MSB first). If the device ID received matches the device ID of the WM9081, then the WM9081 responds by pulling SDIN low on the next clock pulse (ACK). If the device ID is not recognised or the R/W bit is ‘1’ when operating in write only mode, the WM9081 returns to the idle condition and waits for a new start condition and valid address.

If the device ID matches the device ID of the WM9081, the data transfer continues as described below. The controller indicates the end of data transfer with a low to high transition on SDIN while SCLK remains high. After receiving a complete address and data sequence the WM9081 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device returns to the idle condition.

The WM9081 supports the following read and write operations:

- Single write
- Single read
- Multiple write using auto-increment
- Multiple read using auto-increment

The sequence of signals associated with a single register write operation is illustrated in Figure 11.

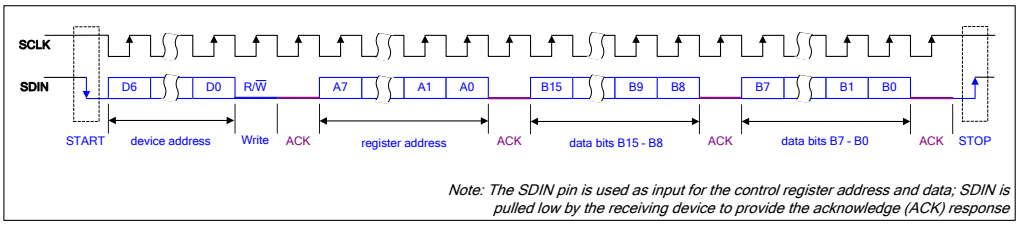


Figure 11 Control Interface 2-wire Register Write

The sequence of signals associated with a single register read operation is illustrated in Figure 12.

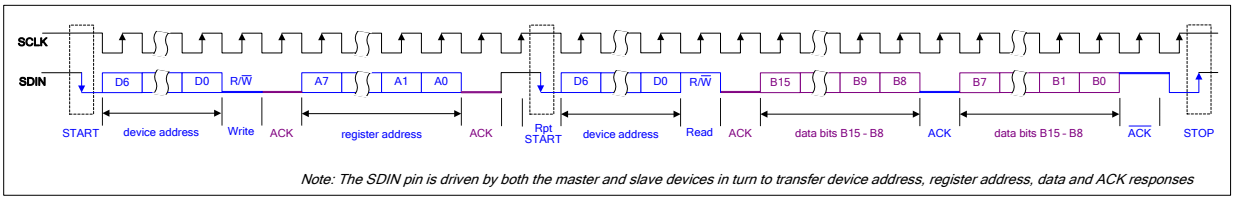


Figure 12 Control Interface 2-wire Register Read

The Control Interface also supports other register operations, as listed above. The interface protocol for these operations is summarised below. The terminology used in the following figures is detailed in Table 4.

Note that, for multiple write and multiple read operations, the auto-increment option must be enabled. This feature is enabled by default; it is described in Table 5 below.

TERMINOLOGY	DESCRIPTION
S	Start Condition
Sr	Repeated start
A	Acknowledge
P	Stop Condition
R/W	0 = Write 1 = Read
[White field]	Data flow from bus master to WM9081
[Grey field]	Data flow from WM9081 to bus master

Table 4 Control Interface Terminology

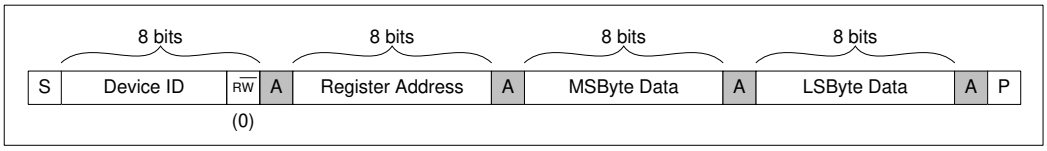


Figure 13 Single Register Write to Specified Address

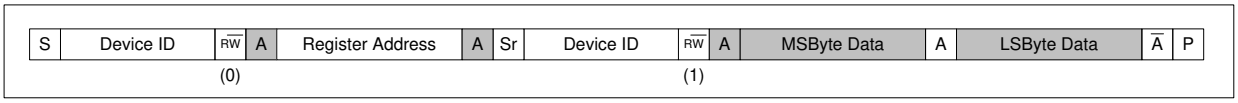


Figure 14 Single Register Read from Specified Address

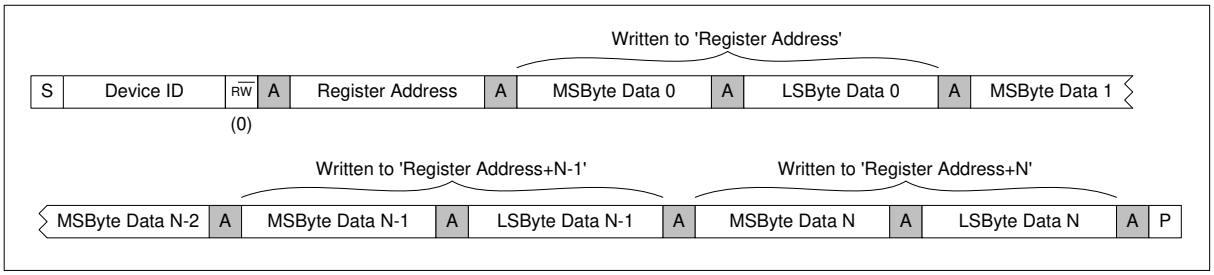


Figure 15 Multiple Register Write to Specified Address using Auto-increment

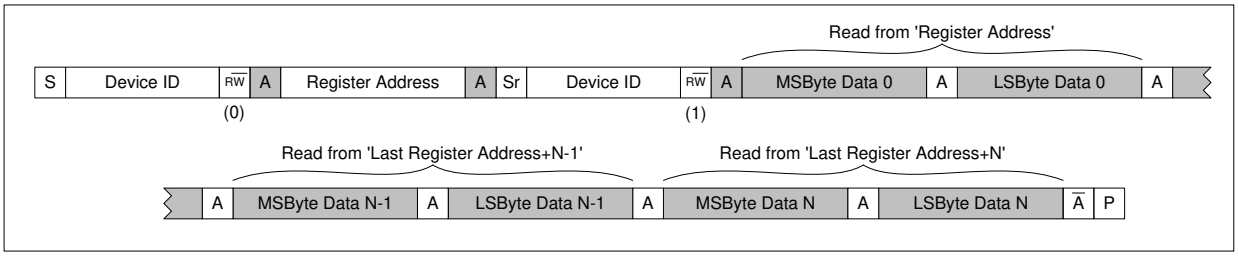


Figure 16 Multiple Register Read from Specified Address using Auto-increment

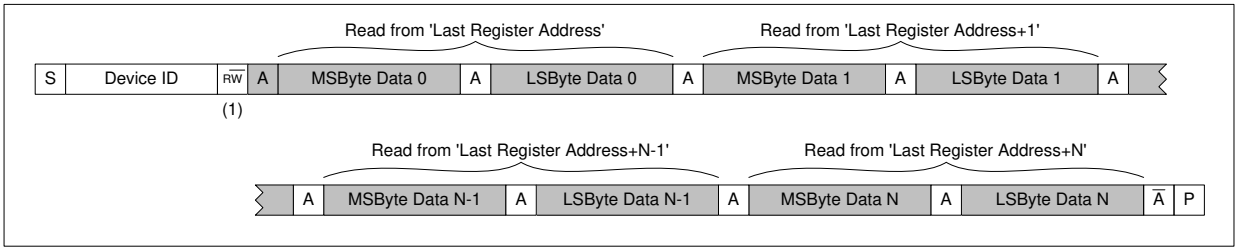


Figure 17 Multiple Register Read from Last Address using Auto-increment

Multiple Write and Multiple Read operations enable the host processor to access sequential blocks of the data in the WM9081 register map faster than is possible with single register operations. The auto-increment option is enabled when the AUTO_INC register bit is set. This bit is defined in Table 5. Auto-increment is enabled by default.

SMBUS Alert Response Address protocol is supported by the WM9081 when the ARA_ENA register bit is set. This function enables a bus controller to poll multiple devices on the I2C bus simultaneously in order to respond to Interrupt events efficiently. The WM9081 does not support automatic clearing of the SMBALERT# (implemented as IRQ on this device); a host device must service the alert and manually clear the IRQ status before proceeding to any other alerting devices in the system. The WM9081 device address used by this protocol is set as described in Table 5.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) MW Slave 1	3	ARA_ENA	0	Alert Response Address protocol enable 0 = Disabled 1 = Enabled
	1	AUTO_INC	1	Enable Auto-Increment function 0 = Disabled 1 = Enabled

Table 5 Auto-Increment and Alert Response Address Control

3-WIRE CONTROL MODE

The WM9081 is controlled by writing to registers through a 3-wire serial control interface. A control word consists of 24 bits. The first bit is the read/write bit (R/W), which is followed by 7 address bits (A6 to A0) that determine which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register.

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on $\overline{CS}$ latches in a complete control word consisting of the last 24 bits.

In Write operations (R/W=0), all SDIN bits are driven by the controlling device.

In Read operations (R/W=1), the SDIN pin is driven by the controlling device to clock in the register address, after which the WM9081 drives the SDIN pin to output the applicable data bits.

The 3-wire control mode timing is illustrated in Figure 18.

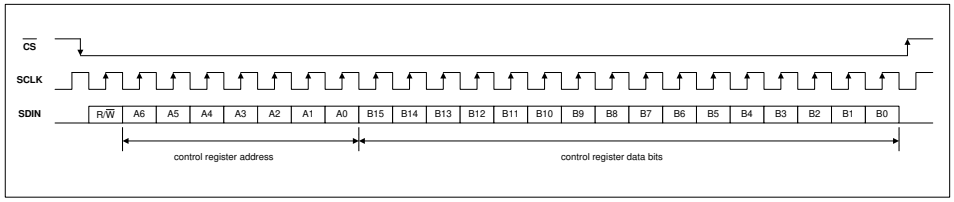


Figure 18 3-Wire Serial Control Interface

4-WIRE CONTROL MODE

In Write operations, this mode is the same as 3-wire Control Mode.

In Read operations, the SDIN pin is ignored following receipt of the valid register address. The data bits are output by the WM9081 on the SDOUT pin.

The SDOUT pin can be configured as CMOS or Open Drain, as described in Table 2. In CMOS mode, SDOUT is driven low when not outputting register data bits. In Open Drain mode, SDOUT is undriven when not outputting register data bits.

The 4-wire control mode timing is illustrated in Figure 19.

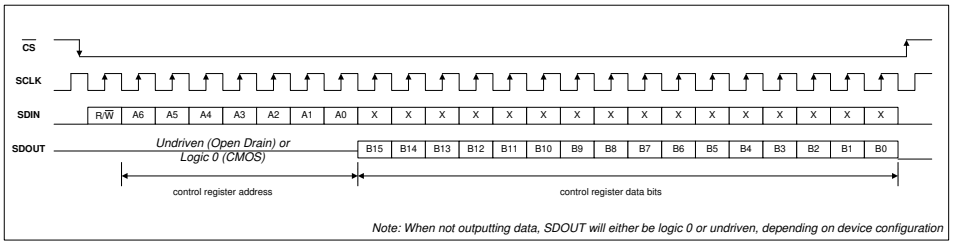


Figure 19 4-Wire Serial Control Interface

CONTROL INTERFACE (HARDWARE MODE)

The WM9081 can be controlled in hardware mode or in software modes. In hardware mode, the device is configured according to logic levels applied to hardware pins. In software mode, the device is configured using control register writes via a serial control interface. See "Control Interface (Software Mode)" for details of software control mode.

Hardware Control Mode selected by logic 0 on the SWMODE pin. The logic level is referenced to the DBVDD power domain. When Hardware Mode is selected, the associated multi-function control pins are defined as described in Table 7.

Note that two variants of Hardware Control Mode are supported; these are selected according to the logic level on the CS/ADDR1/4FS pin, as described in Table 7. In Normal mode, the WM9081 is clocked via a 12.288MHz input to the MCLK pin. In 4FS mode, the WM9081 is clocked via the BCLK pin. The selected channel of the received audio signal is routed to the Class D speaker output.

PIN	DESCRIPTION
SCIM/CHANNEL	Left/Right Channel select 0 = Left channel 1 = Right channel
SDIN/ENA	Device Enable (Normal mode) 0 = Disabled 1 = Enabled
SCLK	Not used
SDOUT/ADDR0	Not used
CS /ADDR1/4FS	4FS Mode select 0 = Normal 1 = 4FS Mode enabled

Table 6 Hardware Control Pin Configuration

A typical system configuration using hardware (normal) control is illustrated in Figure 20.

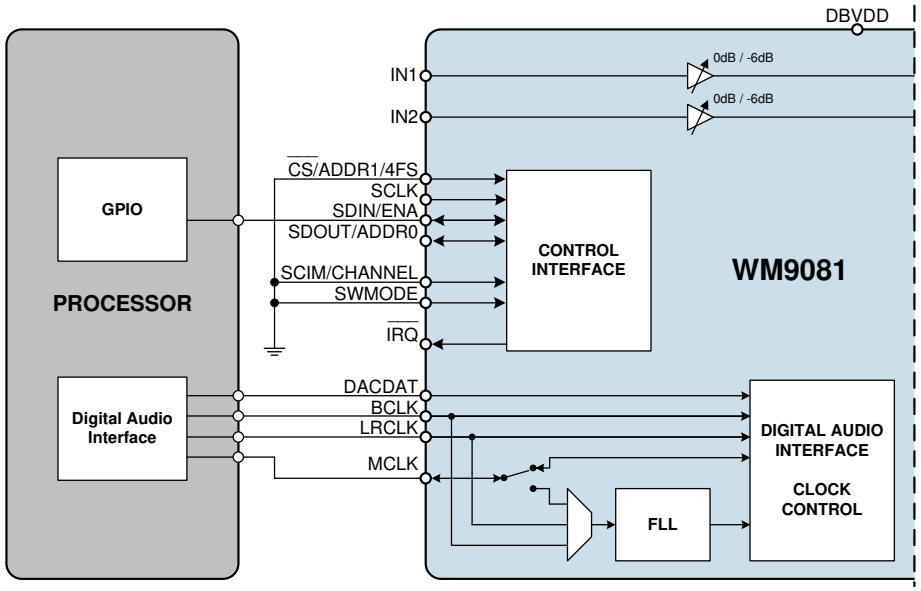


Figure 20 Hardware Control Mode Example – Normal Mode, Left Channel

A typical system configuration using 4FS mode is illustrated in Figure 21.

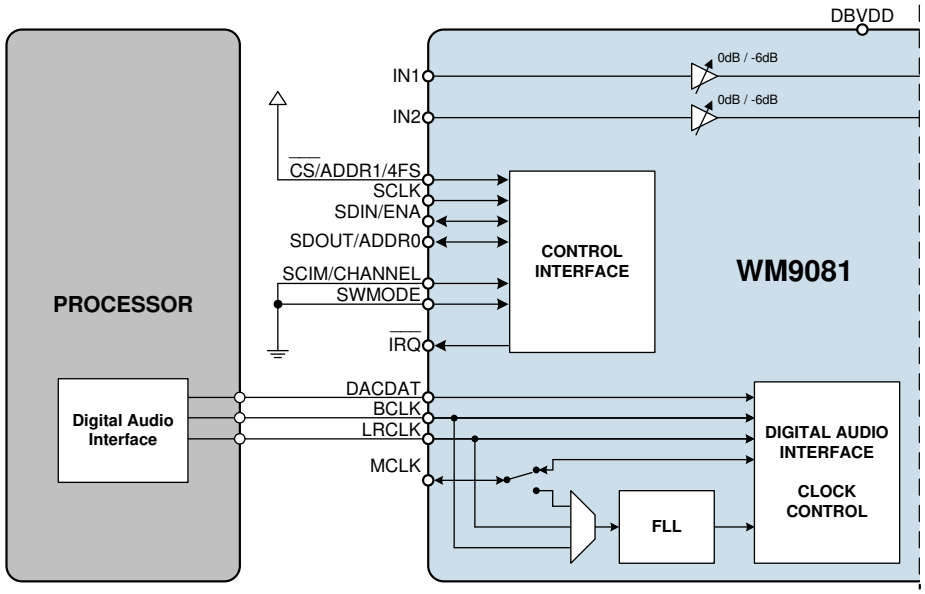


Figure 21 Hardware Control Mode Example – 4FS Mode, Left Channel

DEVICE ENABLE

The WM9081 is enabled by logic 1 on the SDIN/ENA pin. The logic level is referenced to the DBVDD power domain.

Note that in 4FS mode (see below), the WM9081 starts up and shuts down automatically according to the BCLK signal. In 4FS mode, the SDIN/ENA pin is ignored and may be set to either Logic 0 or Logic 1.