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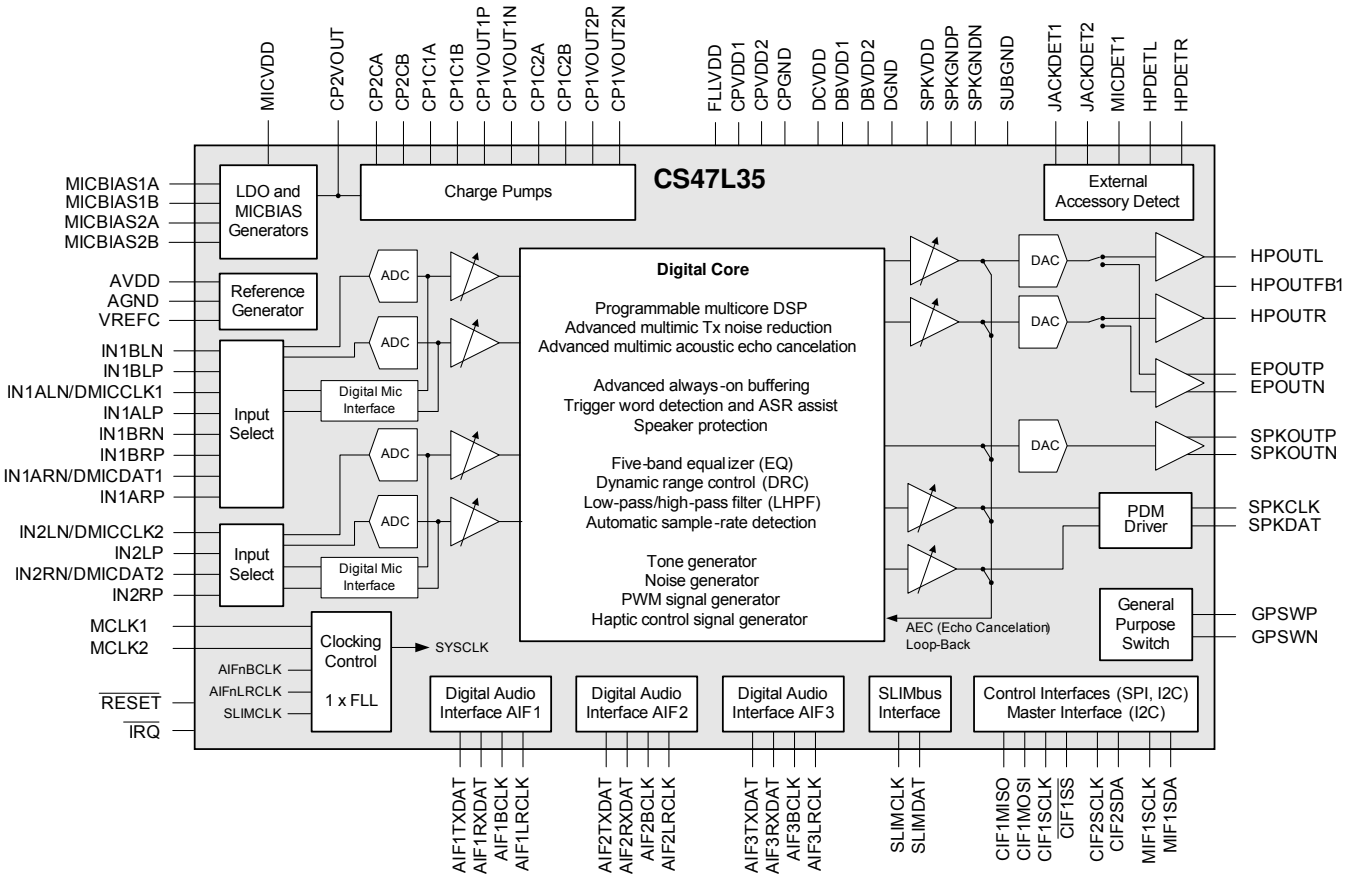
Smart Codec with Low-Power Audio DSP

Features

- 450 MIPS, 450 MMAC multicore audio-signal processor
- Programmable wideband, multimic audio processing
  - Transmit-path noise reduction and echo cancelation
  - Wind-noise, side-tone, and other programmable filters
- Integrated multichannel 24-bit hi-fi audio hub codec
  - 101-dB signal-to-noise ratio (SNR) mic input (48 kHz)
  - 122-dB SNR headphone playback (48 kHz)
- Up to six analog or four digital microphone (DMIC) inputs
- Stereo headphone/earpiece/line output driver: 30 mW into 32-Ω load at 0.1% total harmonic distortion + noise (THD+N)
- Earpiece, speaker, and digital (pulse-density modulation, PDM) output interfaces
- SLIMbus® audio and control interface
- Three full digital-audio interfaces
  - Standard sample rates from 8 to 192 kHz
  - Multichannel time-division multiplexing (TDM) support on AIF1
- Flexible clocking, derived from MCLK*n*, AIF*n*, or SLIMbus
- Low-power frequency-locked loop (FLL) supports reference clocks down to 32 kHz
- Configurable functions on up to 16 general-purpose input/output (GPIO) pins
- Sensor-hub connectivity, with event time-stamp functions
- Integrated regulators and charge pumps
- Small W-CSP package, 0.4-mm ball array

Applications

- Smartphones and multimedia handsets
- Tablets and mobile Internet devices



Description

The CS47L35 is a highly integrated, low-power audio hub for smartphones, tablets, and other portable audio devices. It combines an advanced DSP feature set with a flexible, high-performance audio hub codec. The CS47L35 combines three programmable DSP cores with a variety of power-efficient fixed-function audio processors. Flexible GPIO and an I²C master interface are also incorporated, enabling sensor-hub connectivity.

The DSP cores support multiple concurrent audio features, including multimic wideband noise reduction, high-performance acoustic-echo cancelation (AEC), speech enhancement, advanced media enhancement, and many more. The DSP cores are supported by a fully flexible, all-digital mixing and routing engine with sample-rate converters, for wide use-case flexibility. Support for third-party DSP programming provides far-reaching opportunities for product differentiation.

A SLIMbus interface supports multichannel audio paths and host control register access. Three further digital audio interfaces are provided, each supporting a wide range of standard audio sample rates and serial interface formats. Automatic sample-rate detection enables seamless wideband/narrowband voice-call handover.

The stereo headphone driver provides ground-referenced output, with noise levels as low as 0.8 μV_{RMS} for hi-fi quality line or headphone output. The CS47L35 also features a mono bridge-tied load (BTL) earpiece output, mono 2.7-W Class D speaker driver, two channels of stereo PDM output, and an IEC-60958-3–compatible S/PDIF transmitter. A signal generator for controlling haptics devices is included; vibe actuators can connect directly to the Class D speaker output, or via an external driver on the PDM output interface.

The CS47L35 supports up to six analog inputs, and up to four PDM digital inputs. Microphone activity detection with interrupt is available. A smart accessory interface supports most standard 3.5-mm accessories. Impedance sensing and measurement is provided for external accessory and push-button detection (Android™ headset specification compliant).

The CS47L35 is configured using the SLIMbus, SPI™, or I²C interfaces. The integrated FLL provides support for a wide range of system-clock frequencies. The device is powered from 1.8- and 1.2-V supplies. (A separate 4.2-V battery supply is typically required for the Class D speaker drivers). The power, clocking, and output driver architectures are designed to maximize battery life in voice, music, and standby modes. Low-power (10 μA) Sleep Mode is supported, with configurable wake-up events.

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1 Pin Descriptions

1.1 WLCSP Pinout

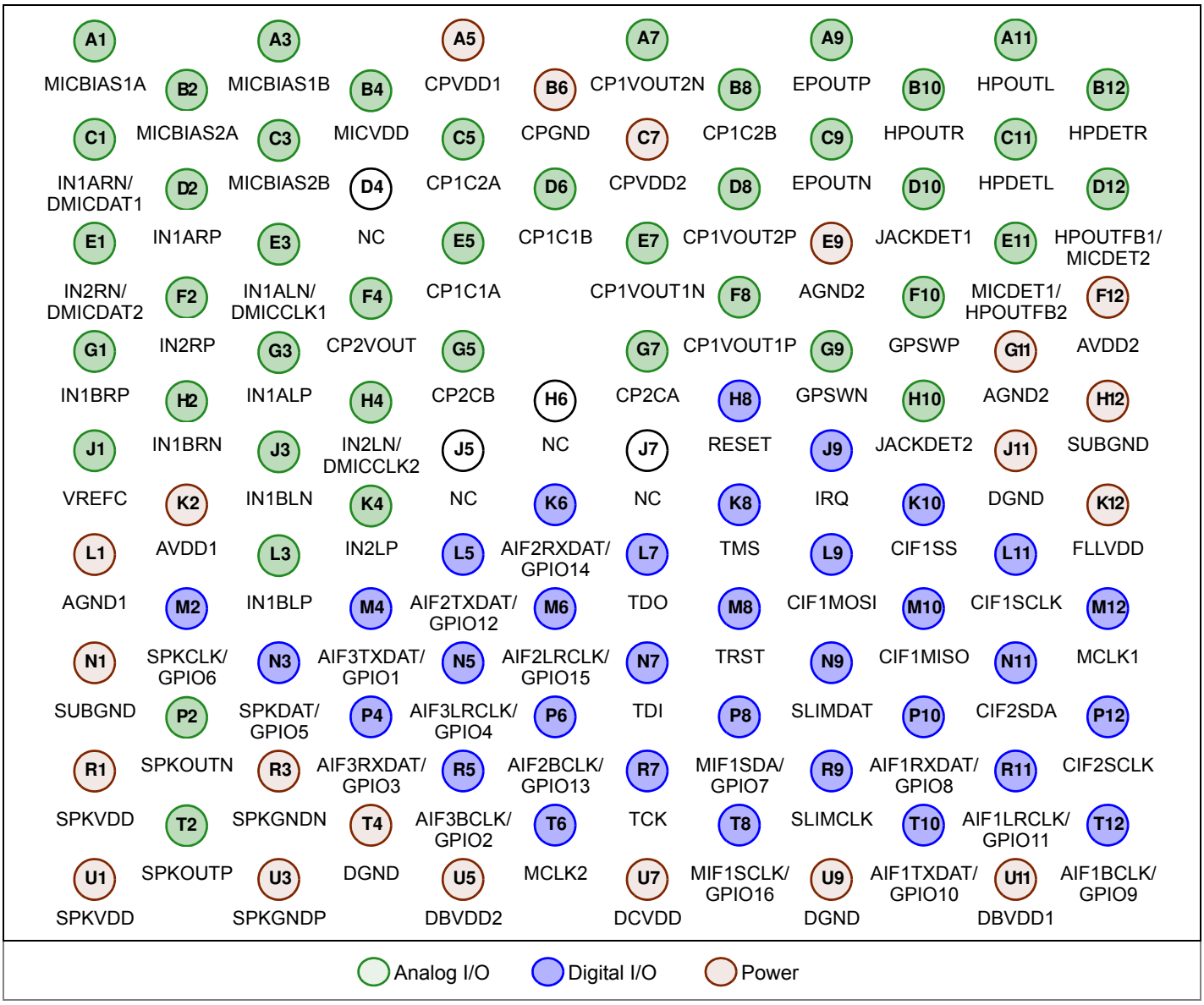


Figure 1-1. Top-Down (Through-Package) View—101-Ball WLCSP Package

1.2 Pin Descriptions

Table 1-1 describes each pin on the CS47L35. Note that pins that share a common name should be tied together on the printed circuit board (PCB). All digital output pins are CMOS outputs, unless otherwise stated.

Table 1-1. Pin Descriptions

Name	Ball #	Power Supply	I/O	Description
			Analog I/O	
CP1C1A	E5	—	O	Charge Pump 1 fly-back capacitor 1 pin
CP1C1B	D6	—	O	Charge Pump 1 fly-back capacitor 1 pin
CP1C2A	C5	—	O	Charge Pump 1 fly-back capacitor 2 pin
CP1C2B	B8	—	O	Charge Pump 1 fly-back capacitor 2 pin
CP1VOUT1N	E7	—	O	Charge Pump 1 negative output 1 decoupling pin
CP1VOUT1P	F8	—	O	Charge Pump 1 positive output 1 decoupling pin
CP1VOUT2N	A7	—	O	Charge Pump 1 negative output 2 decoupling pin
CP1VOUT2P	D8	—	O	Charge Pump 1 positive output 2 decoupling pin
CP2CA	G7	—	O	Charge Pump 2 fly-back capacitor pin
CP2CB	G5	—	O	Charge Pump 2 fly-back capacitor pin
CP2VOUT	F4	—	O	Charge Pump 2 output decoupling pin/supply for LDO2
EPOUTN	C9	—	O	Earpiece negative output
EPOUTP	A9	—	O	Earpiece positive output
GPSWN	G9	—	I/O	General-purpose bidirectional switch contact
GPSWP	F10	—	I/O	General-purpose bidirectional switch contact
HPDETL	C11	—	I	Headphone left (HPOUTL) sense input
HPDETR	B12	—	I	Headphone right (HPOUTR) sense input
HPOUTFB1/MICDET2	D12	—	I	HPOUTL and HPOUTR ground feedback pin 1/mic and accessory sense input 2
HPOUTL	A11	—	O	Left headphone output
HPOUTR	B10	—	O	Right headphone output
IN1ALN/DMICCLK1	E3	MICVDD or MICBIAS*nx*	I/O	Left-channel negative differential mic/line input /DMIC Clock Output 1
IN1ALP	G3	MICVDD	I	Left-channel single-ended mic/line input/left-channel positive differential mic/line input
IN1ARN/DMICDAT1	C1	MICVDD or MICBIAS*nx*	I	Right-channel negative differential mic/line input/DMIC Data Input 1
IN1ARP	D2	MICVDD	I	Right-channel single-ended mic/line input/right-channel positive differential mic/line input
IN1BLN	J3	MICVDD	I	Left-channel negative differential mic/line input. Also suitable for connection to external accessory interfaces.
IN1BLP	L3	MICVDD	I	Left-channel single-ended mic/line input/left-channel positive differential mic/line input. Also suitable for connection to external accessory interfaces.
IN1BRN	H2	MICVDD	I	Right-channel negative differential mic/line input. Also suitable for connection to external accessory interfaces.
IN1BRP	G1	MICVDD	I	Right-channel single-ended mic/line input/right-channel positive differential mic/line input. Also suitable for connection to external accessory interfaces.
IN2LN/DMICCLK2	H4	MICVDD or MICBIAS*nx*	I/O	Left-channel negative differential mic/line input/DMIC Clock Output 2

Table 1-1. Pin Descriptions *(Cont.)*

Name	Ball #	Power Supply	I/O	Description
IN2LP	K4	MICVDD	I	Left-channel single-ended mic/line input/left-channel positive differential mic/line input
IN2RN/DMICDAT2	E1	MICVDD or MICBIAS*nx*	I	Right-channel negative differential mic/line input/DMIC Data Input 2
IN2RP	F2	MICVDD	I	Right-channel single-ended mic/line input/right-channel positive differential mic/line input
JACKDET1	D10	AVDD	I	Jack detect input 1
JACKDET2	H10	AVDD	I	Jack detect input 2
MICBIAS1A	A1	—	O	Microphone bias 1A
MICBIAS1B	A3	—	O	Microphone bias 1B
MICBIAS2A	B2	—	O	Microphone bias 2A
MICBIAS2B	C3	—	O	Microphone bias 2B
MICDET1/HPOUTFB2	E11	—	I	Microphone and accessory sense input 1/HPOUTL and HPOUTR ground feedback pin 2
MICVDD	B4	—	O	LDO2 output decoupling pin (generated internally by CS47L35). (Can also be used as reference/supply for external microphones.)
SPKOUTN	P2	—	O	Speaker negative output
SPKOUTP	T2	—	O	Speaker positive output
VREFC	J1	—	O	Band-gap reference external capacitor connection
				Digital I/O
AIF1BCLK/GPIO9	T12	DBVDD1	I/O	Audio interface 1 bit clock/GPIO. GPIO output is selectable CMOS or open drain; BCLK output is CMOS.
AIF1LRCLK/GPIO11	R11	DBVDD1	I/O	Audio interface 1 left/right clock/GPIO. GPIO output is selectable CMOS or open drain; LRCLK output is CMOS.
AIF1RXDAT/GPIO8	P10	DBVDD1	I/O	Audio interface 1 RX digital audio data/GPIO. GPIO output is selectable CMOS or open drain.
AIF1TXDAT/GPIO10	T10	DBVDD1	I/O	Audio interface 1 TX digital audio data/GPIO. GPIO output is selectable CMOS or open drain; TXDAT output is CMOS.
AIF2BCLK/GPIO13	P6	DBVDD2	I/O	Audio interface 2 bit clock/GPIO. GPIO output is selectable CMOS or open drain; BCLK output is CMOS.
AIF2LRCLK/GPIO15	M6	DBVDD2	I/O	Audio interface 2 left/right clock/GPIO. GPIO output is selectable CMOS or open drain; LRCLK output is CMOS.
AIF2RXDAT/GPIO14	K6	DBVDD2	I/O	Audio interface 2 RX digital audio data/GPIO. GPIO output is selectable CMOS or open drain.
AIF2TXDAT/GPIO12	L5	DBVDD2	I/O	Audio interface 2 TX digital audio data/GPIO. GPIO output is selectable CMOS or open drain; TXDAT output is CMOS.
AIF3BCLK/GPIO2	R5	DBVDD2	I/O	Audio interface 3 bit clock/GPIO. GPIO output is selectable CMOS or open drain; BCLK output is CMOS.
AIF3LRCLK/GPIO4	N5	DBVDD2	I/O	Audio interface 3 left/right clock/GPIO. GPIO output is selectable CMOS or open drain; LRCLK output is CMOS.
AIF3RXDAT/GPIO3	P4	DBVDD2	I/O	Audio interface 3 RX digital audio data/GPIO. GPIO output is selectable CMOS or open drain.
AIF3TXDAT/GPIO1	M4	DBVDD2	I/O	Audio interface 3 TX digital audio data/GPIO. GPIO output is selectable CMOS or open drain; TXDAT output is CMOS.
CIF1MISO	M10	DBVDD1	O	Control interface 1 (SPI) Master In Slave Out data. The CIFMISO is high impedance if $\overline{\text{CIF1SS}}$ is not asserted.
CIF1MOSI	L9	DBVDD1	I	Control interface 1 (SPI) Master Out Slave In data
CIF1SCLK	L11	DBVDD1	I	Control interface 1 (SPI) clock input
$\overline{\text{CIF1SS}}$	K10	DBVDD1	I	Control interface 1 (SPI) slave select (SS)
CIF2SCLK	P12	DBVDD1	I	Control interface 2 (I^2C) clock input

Table 1-1. Pin Descriptions *(Cont.)*

Name	Ball #	Power Supply	I/O	Description
CIF2SDA	N11	DBVDD1	I/O	Control interface 2 (I^2C) data input and output. The SDA output is open drain.
$\overline{IRQ}$	J9	DBVDD1	O	Interrupt request output (default is active low). The pin configuration is selectable CMOS or open drain.
MCLK1	M12	DBVDD1	I	Master clock 1
MCLK2	T6	DBVDD2	I	Master clock 2
MIF1SCLK/GPIO16	T8	DBVDD1	I/O	Master (I^2C) Interface 1 clock output/GPIO. GPIO output is selectable CMOS or open drain; SCLK output is open drain.
MIF1SDA/GPIO7	P8	DBVDD1	I/O	Master (I^2C) Interface 1 data input and output/GPIO. GPIO output is selectable CMOS or open drain; SDA output is open drain.
$\overline{RESET}$	H8	DBVDD1	I	Digital reset input (active low)
SLIMCLK	R9	DBVDD1	I/O	SLIMbus clock I/O
SLIMDAT	N9	DBVDD1	I/O	SLIMbus data I/O
SPKCLK/GPIO6	M2	DBVDD2	I/O	Digital speaker (PDM) 1 clock output/GPIO. GPIO output is selectable CMOS or open drain; SPKCLK output is CMOS.
SPKDAT/GPIO5	N3	DBVDD2	I/O	Digital speaker (PDM) 1 data output/GPIO. GPIO output is selectable CMOS or open drain; SPKDAT output is CMOS.
TCK	R7	DBVDD2	I	JTAG clock input. Internal pull-down holds this pin at Logic 0 for normal operation.
TDI	N7	DBVDD2	I	JTAG data input. Internal pull-down holds this pin at Logic 0 for normal operation.
TDO	L7	DBVDD2	O	JTAG data output
TMS	K8	DBVDD2	I	JTAG mode select input. Internal pull-down holds this pin at Logic 0 for normal operation.
TRST	M8	DBVDD2	I	JTAG test access port reset (active low). Internal pull-down holds this pin at Logic 0 for normal operation.
				Supply
AGND1	L1	—	—	Analog ground (return path for AVDD1)
AGND2	E9, G11	—	—	Analog ground (return path for AVDD2)
AVDD1	K2	—	—	Analog supply
AVDD2	F12	—	—	Analog supply
CPGND	B6	—	—	Charge pump ground (return path for CPVDD1, CPVDD2)
CPVDD1	A5	—	—	Supply for Charge Pump 1 and Charge Pump 2
CPVDD2	C7	—	—	Secondary supply for Charge Pump 1
DBVDD1	U11	—	—	Digital buffer (I/O) supply (core functions, AIF1, CIF1, CIF2, SLIMbus, MIF1)
DBVDD2	U5	—	—	Digital buffer (I/O) supply (AIF2, AIF3, PDM, MCLK2, JTAG)

Table 1-1. Pin Descriptions *(Cont.)*

Name	Ball #	Power Supply	I/O	Description
DCVDD	U7	—	—	Digital core supply
DGND	J11, T4, U9	—	—	Digital ground (return path for DCVDD and DBVDD*n*)
FLLVDD	K12	—	—	Analog supply (FLL1)
SPKGNDN	R3	—	—	Speaker driver ground (return path for SPKVDD) [1]
SPKGNDP	U3	—	—	Speaker driver ground (return path for SPKVDD) [1]
SPKVDD	R1, U1	—	—	Speaker driver supply
SUBGND	H12, N1	—	—	Substrate ground
No Connect				
NC	D4, H6, J5, J7	—	—	—

1. Separate P/N ground connections are provided for the Class D speaker output, which provides flexible support for current monitoring and output-protection circuits. If this option is not used, these ground connections should be tied together on the PCB.

2 Typical Connection Diagram

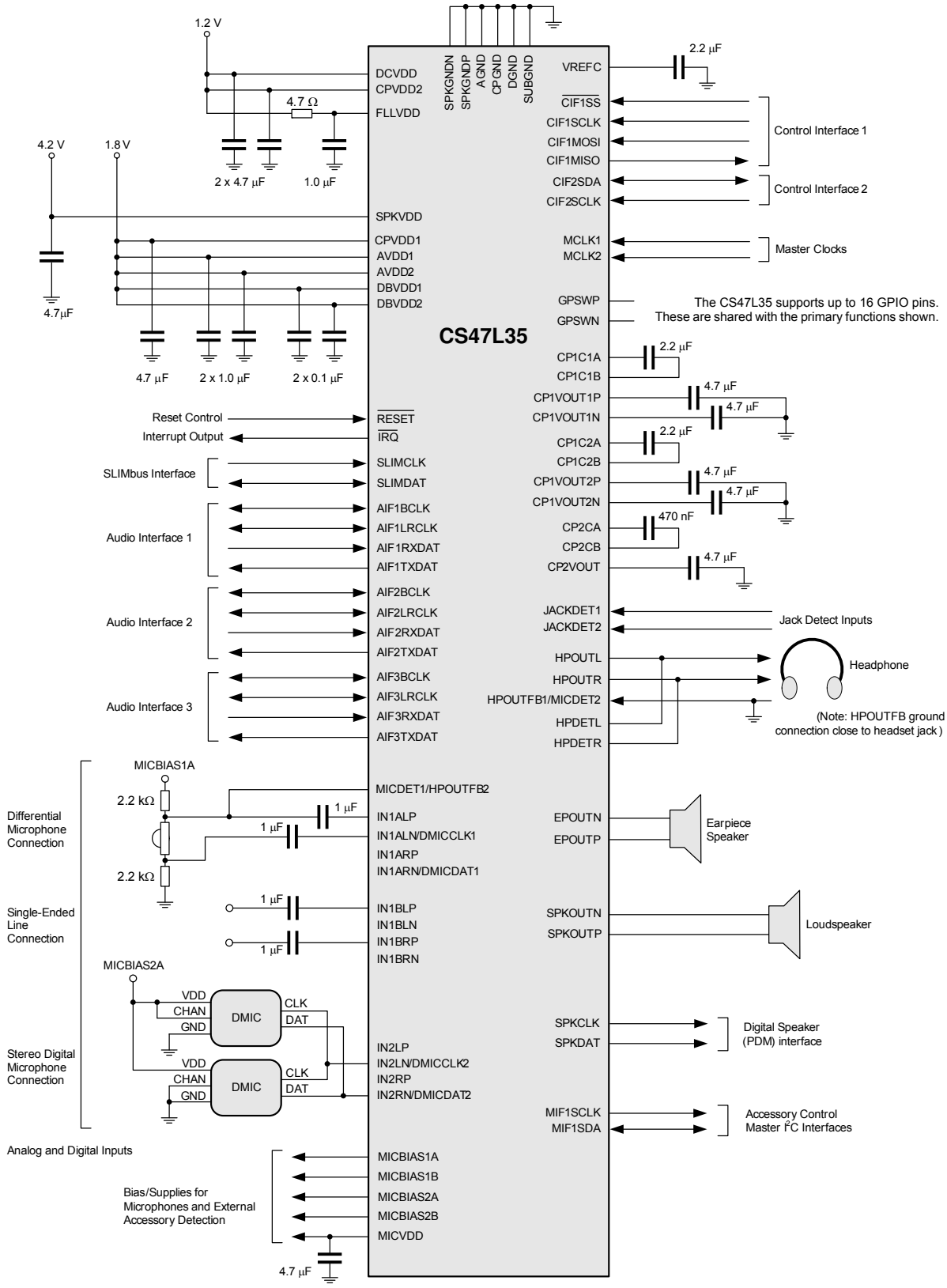


Figure 2-1. Typical Connection Diagram

3 Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

Table 3-1. Parameter Definitions

Parameter	Definition
Channel separation	Left-to-right and right-to-left channel separation is the difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
Common-mode rejection ratio (CMRR)	The ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
Dynamic range (DR)	A measure of the difference between the maximum full scale output signal and the sum of all harmonic distortion products plus noise, with a low-level input signal applied. Typically, an input signal level 60 dB below full scale is used.
Power-supply rejection ratio (PSRR)	The ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
Signal-to-noise ratio (SNR)	A measure of the difference in level between the maximum full scale output signal and the output with no input signal applied.
Total harmonic distortion (THD)	The ratio of the RMS sum of the harmonic distortion products in the specified bandwidth [1] relative to the RMS amplitude of the fundamental (i.e., test frequency) output.
Total harmonic distortion plus noise (THD+N)	The ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth [1] relative to the RMS amplitude of the fundamental (i.e., test frequency) output.

1. All performance measurements are specified with a 20-kHz low-pass brick-wall filter and, where noted, an A-weighted filter. The low-pass filter removes out-of-band noise.

Table 3-2. Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under electrical characteristics at the test conditions specified.

Parameter		Symbol	Minimum	Maximum
Supply voltages		DCVDD [1], FLLVDD [1] CPVDD1, CPVDD2 DBVDD1, DBVDD2, AVDD [2], MICVDD SPKVDD	–0.3 V –0.3 V –0.3 V –0.3 V	1.6 V 2.5 V 5.0 V 6.0 V
Voltage range digital inputs	DBVDD1 domain DBVDD2 domain	— —	SUBGND – 0.3 V SUBGND – 0.3 V	DBVDD1 + 0.3 V DBVDD2 + 0.3 V
Voltage range analog inputs		IN1Axx, IN2xx IN1Bxx HPOUTFB*n* [3] MICDET*n* [3] JACKDET1, HPDETL, HPDETR JACKDET2 [4], GPSWP, GPSWN	SUBGND – 0.3 V SUBGND – 0.9 V SUBGND – 0.3 V SUBGND – 0.3 V CP1VOUT2N – 0.3 V [5] SUBGND – 0.3 V	MICVDD + 0.3 V MICVDD + 0.3 V SUBGND + 0.3 V MICVDD + 0.3 V AVDD + 0.3 V MICVDD + 0.3 V
Ground		AGND [6], DGND, CPGND, SPKGND	SUBGND – 0.3 V	SUBGND + 0.3 V
Operating temperature range		T_A	–40ºC	+85ºC
Operating junction temperature		T_J	–40ºC	+125ºC
Storage temperature after soldering		—	–65ºC	+150ºC

ESD-sensitive device. The CS47L35 is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device. This device is qualified to current JEDEC ESD standards.

1. The DCVDD and FLLVDD pins should be tied together. The associated power domain is referred to as DCVDD.
2. The AVDD1 and AVDD2 pins should be tied together. The associated power domain is referred to as AVDD.
3. The HPOUTFB*n* and MICDET*n* functions share common pins. The absolute maximum rating varies according to the applicable function of each pin.
4. If AVDD > MICVDD (e.g., if LDO2 is disabled), the maximum JACKDET2 voltage is AVDD + 0.3 V.
5. CP1VOUT2N is an internal supply, generated by the CS47L35 charge pump (CP1). Its voltage can vary between CPGND and –CPVDD1.
6. The AGND1 and AGND2 pins should be tied together. The associated ground domain is referred to as AGND.

Table 3-3. Recommended Operating Conditions

Parameter		Symbol	Minimum	Typical	Maximum	Units
Digital supply range [1]	Core and FLL	DCVDD [2], FLLVDD [3]	1.14	1.2	1.26	V
Digital supply range	I/O	DBVDD1, DBVDD2	1.71	—	3.6 [4]	V
Charge pump supply range	CPVDD1	CPVDD1	1.71	1.8	1.89	V
	CPVDD2	CPVDD2	1.14	1.2	1.26	V
Speaker supply range		SPKVDD	2.4		5.5	V
Analog supply range [5,6]		AVDD	1.71	1.8	1.89	V
Mic bias supply [7]		MICVDD	0.9	2.5	3.78	V
Ground [8]		DGND, AGND, CPGND, SPKGND, SUBGND	—	0	—	V
Power supply rise time [9,10]		DCVDD	10	—	2000	µs
		All other supplies	10	—	—	µs
Operating temperature range		T_A	–40	—	85	ºC

Note: There are no power sequencing requirements; the supplies may be enabled and disabled in any order.

1. The DCVDD and FLLVDD pins should be tied together. The associated power domain is referred to as DCVDD.
2. Sleep mode is supported for when DCVDD is below the limits noted, provided that AVDD and DBVDD1 are present
3. It is recommended to connect a 4.7-Ω resistor in series with the FLLVDD pin connection. Note that the minimum voltage limit applies at the supply end of the 4.7-Ω resistor in this case.
4. If the SLIMbus interface is enabled, the maximum DBVDD1 voltage is 1.98 V.
5. The AVDD1 and AVDD2 pins should be tied together. The associated power domain is referred to as AVDD
6. The AGND1 and AGND2 pins should be tied together. The associated ground domain is referred to as AGND
7. An internal charge pump and LDO (powered by CPVDD1) provide the mic bias supply; the MICVDD pin must not be connected to an external supply.
8. The impedance between DGND, AGND, and SUBGND must not exceed 0.1 Ω.
   The impedance between SPKGND and SUBGND must not exceed 0.2 Ω.
9. If the DCVDD rise time exceeds 2 ms, RESET must be asserted (low) during the rise and held asserted until after DCVDD is within the recommended operating limits.
10. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100 nF per pin. However, Cirrus Logic strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed. The specified minimum power supply rise times also assume a maximum PCB inductance of 10 nH between decoupling capacitor and pin.

Table 3-4. Analog Input Signal Level—IN1AL, IN1BL, IN1AR, IN1BR, IN2L, IN2R

Test conditions (unless specified otherwise): AVDD = 1.8V; with the exception of the condition noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter		Minimum	Typical	Maximum	Units
Full-scale input signal level (0 dBFS output)	Single-ended PGA input, 0 dB PGA gain	—	0.5	—	V_{RMS}
		—	–6	—	dBV
	Differential PGA input, 0 dB PGA gain	—	1	—	V_{RMS}
		—	0	—	dBV

Notes:
- The full-scale input signal level is also the maximum analog input level, before clipping occurs.
- The full-scale input signal level changes in proportion with AVDD. For differential input, it is calculated as AVDD/1.8.
- A 1.0V_{RMS} differential signal equates to 0.5V_{RMS}/–6dBV per input.
- A sinusoidal input signal is assumed.

Table 3-5. Analog Input Pin Characteristics

Test conditions (unless specified otherwise): T_A = +25ºC; with the exception of the condition noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter		Minimum	Typical	Maximum	Units
Input resistance	Single-ended PGA input, All PGA gain settings	9	10.5	—	kΩ
	Differential PGA input, All PGA gain settings	18	21	—	kΩ
Input capacitance		—	—	5	pF

Table 3-6. Analog Input Gain—Programmable Gain Amplifiers (PGAs)

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter		Minimum	Typical	Maximum	Units
Minimum programmable gain		—	0	—	dB
Maximum programmable gain		—	31	—	dB
Programmable gain step size	Guaranteed monotonic	—	1	—	dB

Table 3-7. Digital Input Signal Level—DMICDAT1, DMICDAT2

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter		Minimum	Typical	Max	Units
Full-scale input signal level (0 dBFS output)	0 dB gain	—	–6	—	dBFS

Note: The DMIC input signal level is measured in dBFS, where 0 dBFS is a signal level equal to the full-scale range (FSR) of the PDM input. The FSR is defined as the amplitude of a 1-kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively—this is the largest 1-kHz sine wave that can fit in the digital output range without clipping.

Table 3-8. Output Characteristics

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter			Minimum	Typical	Max	Units
Line/headphone/earpiece output driver (HPOUTL, HPOUTR)	Load resistance	Normal operation, Single-Ended Mode	6	—	—	Ω
		Normal operation, Differential (BTL) Mode	15	—	—	Ω
		Device survival with load applied indefinitely	0	—	—	Ω
	Load capacitance	Single-Ended Mode	—	—	500	pF
		Differential (BTL) Mode	—	—	200	pF
Earpiece output driver (EPOUT)	Load resistance	Normal operation	15	—	—	Ω
		Device survival with load applied indefinitely	0	—	—	Ω
	Load capacitance		—	—	200	pF
Speaker output driver (SPKOUTP+SPKOUTN)	Load resistance	Normal operation	4	—	—	Ω
		Device survival with load applied indefinitely	0	—	—	Ω
	Load capacitance		—	—	200	pF
Digital speaker output (SPKDAT)	Full-scale output level [1]	0 dBFS digital core output, 0 dB gain	—	–6	—	dBFS

1. The digital output signal level is measured in dBFS, where 0 dBFS is a signal level equal to the full-scale range (FSR) of the PDM output. The FSR is defined as the amplitude of a 1-kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively—this is the largest 1-kHz sine wave that can fit in the digital output range without clipping.

Table 3-9. Input/Output Path Characteristics

Test conditions (unless specified otherwise): DBVDD1 = DBVDD2 = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 2.5 V (powered from internal LDO); SPKVDD = 4.2 V; T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter			Min	Typ	Max	Units
Line/headphone/earpiece output driver (HPOUTL, HPOUTR)	DC offset at Load	Single-ended mode	—	50	—	µV
		Differential (BTL) mode	—	75	—	µV
Earpiece output driver (EPOUT+EPOUTN)	DC offset at Load		—	75	—	µV
Speaker output driver (SPKOUTP+SPKOUTN)	DC offset at Load		—	300	—	µV
	SPKVDD leakage current		—	1	—	µA
Analog input paths (IN*n*L, IN*n*R) to ADC (Differential Input Mode)	SNR (A-weighted), defined in Table 3-1	48 kHz sample rate	91	101	—	dB
		16 kHz sample rate (wideband voice)	—	105	—	dB
	THD, defined in Table 3-1	–1 dBV input	—	–87	—	dB
	THD+N, defined in Table 3-1	–1 dBV input	—	–86	–76	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	100	—	dB
	Input-referred noise floor	A-weighted, PGA gain = +20 dB	—	3.2	—	μV_{RMS}
	CMRR, defined in Table 3-1	PGA gain = +30 dB	—	80	—	dB
		PGA gain = 0 dB	—	70	—	dB
	PSRR (DBVDD*n*, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	90	—	dB
		100 mV (peak-peak) 10 kHz	—	75	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	95	—	dB
		100 mV (peak-peak) 10 kHz	—	90	—	dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	100	—	dB
		100 mV (peak-peak) 10 kHz	—	95	—	dB

Table 3-9. Input/Output Path Characteristics *(Cont.)*

Test conditions (unless specified otherwise): DBVDD1 = DBVDD2 = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 2.5 V (powered from internal LDO); SPKVDD = 4.2 V; T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter			Min	Typ	Max	Units
Analog input paths (IN*n*LP, IN*n*RP) to ADC (Single-Ended Input Mode)	SNR (A-weighted), defined in Table 3-1	48-kHz sample rate	89	99	—	dB
		16-kHz sample rate (wideband voice)	—	102	—	dB
	THD, defined in Table 3-1	–7dB V input	—	–86	—	dB
	THD+N, defined in Table 3-1	–7dB V input	—	–85	–75	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	100	—	dB
	Input-referred noise floor	A-weighted, PGA gain = +20 dB	—	4	—	μV_{RMS}
	PSRR (DBVDD*n*, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	77	—	dB
		100 mV (peak-peak) 10 kHz	—	50	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	95	—	dB
		100 mV (peak-peak) 10 kHz	—	65	—	dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	100	—	dB
		100 mV (peak-peak) 10 kHz	—	80	—	dB
DAC to line output (HPOUTL, HPOUTR; Load = 10 kΩ, 50 pF)	Full-scale output signal level	0 dBFS input	—	1	—	V_{RMS}
			—	0	—	dBV
	SNR, defined in Table 3-1	A-weighted, output signal = 1 V_{RMS}	—	122	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	105	115	—	dB
	THD, defined in Table 3-1	0 dBFS input	—	–95	—	dB
	THD+N, defined in Table 3-1	0 dBFS input	—	–93	–83	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	100	—	dB
	Output noise floor	A-weighted	—	0.8	—	μV_{RMS}
	PSRR (DBVDD*n*, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	100	—	dB
		100 mV (peak-peak) 10 kHz	—	73	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	105	—	dB
		100 mV (peak-peak) 10 kHz	—	80	—	dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	110	—	dB
		100 mV (peak-peak) 10 kHz	—	100	—	dB
DAC to headphone output (HPOUTL, HPOUTR; R_L = 32 Ω)	Maximum output power	0.1% THD+N	—	30	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 1 V_{RMS}	—	122	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	105	115	—	dB
	THD, defined in Table 3-1	P_O = 20 mW	—	–93	—	dB
	THD+N, defined in Table 3-1	P_O = 20 mW	—	–91	—	dB
	THD, defined in Table 3-1	P_O = 2 mW	—	–92	—	dB
	THD +N, defined in Table 3-1	P_O = 2 mW	—	–90	–80	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	100	—	dB
	Output noise floor	A-weighted	—	0.8	—	μV_{RMS}
	PSRR (DBVDD*n*, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	100	—	dB
		100 mV (peak-peak) 10 kHz	—	73	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	105	—	dB
		100 mV (peak-peak) 10 kHz	—	80	—	dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	110	—	dB
		100 mV (peak-peak) 10 kHz	—	100	—	dB
DAC to headphone output (HPOUTL, HPOUTR; R_L = 16 Ω)	Maximum output power	0.1% THD+N	—	39	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 1 V_{RMS}	—	122	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	105	115	—	dB
	THD, defined in Table 3-1	P_O = 20 mW	—	–89	—	dB
	THD+N, defined in Table 3-1	P_O = 20 mW	—	–88	—	dB
	THD, defined in Table 3-1	P_O = 2 mW	—	–92	—	dB
	THD+N, defined in Table 3-1	P_O = 2 mW	—	–90	–80	dB
	Channel separation (L/R), defined in Table 3-1	100 Hz to 10 kHz	—	100	—	dB
	Output noise floor	A-weighted	—	0.8	—	μV_{RMS}
	PSRR (DBVDD*n*, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	100	—	dB
		100 mV (peak-peak) 10 kHz	—	73	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	105	—	dB
		100 mV (peak-peak) 10 kHz	—	80	—	dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	110	—	dB
		100 mV (peak-peak) 10 kHz	—	100	—	dB

Table 3-9. Input/Output Path Characteristics *(Cont.)*

Test conditions (unless specified otherwise): DBVDD1 = DBVDD2 = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 2.5 V (powered from internal LDO); SPKVDD = 4.2 V; T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter			Min	Typ	Max	Units
DAC to earpiece output (EPOUTP+EPOUTN, R_L = 32 Ω BTL)	Maximum output power	0.1% THD+N	—	99	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 1.41 V_{RMS}	—	127	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	108	118	—	dB
	THD, defined in Table 3-1	P_O = 75 mW	—	–94	—	dB
	THD+N, defined in Table 3-1	P_O = 75 mW	—	–92	—	dB
	THD, defined in Table 3-1	P_O = 5 mW	—	–94	—	dB
	THD+N, defined in Table 3-1	P_O = 5 mW	—	–92	–82	dB
	Output noise floor	A-weighted	—	0.6	—	μV_{RMS}
	PSRR (DBVDD*n*, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	125 90	— —	dB dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	125 90	— —	dB dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	125 110	— —	dB dB
DAC to earpiece output (EPOUTP+EPOUTN, R_L = 16 Ω BTL)	Maximum output power	0.1% THD+N	—	110	—	mW
	SNR, defined in Table 3-1	A-weighted, output signal = 1.41 V_{RMS}	—	127	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	108	118	—	dB
	THD, defined in Table 3-1	P_O = 75 mW	—	–87	—	dB
	THD+N, defined in Table 3-1	P_O = 75 mW	—	–85	—	dB
	THD, defined in Table 3-1	P_O = 5 mW	—	–92	—	dB
	THD+N, defined in Table 3-1	P_O = 5 mW	—	–90	–80	dB
	Output noise floor	A-weighted	—	0.6	—	μV_{RMS}
	PSRR (DBVDD*n*, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	125 90	— —	dB dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	125 90	— —	dB dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	125 110	— —	dB dB
DAC to speaker output (SPKOUTP+SPKOUTN, Load = 8 Ω, 22 μH, BTL)	Maximum output power	SPKVDD = 5.0 V, 1% THD+N SPKVDD = 4.2 V, 1% THD+N SPKVDD = 3.6 V, 1% THD+N	— — —	1.4 1.0 0.7	— — —	W W W
	SNR, defined in Table 3-1	A-weighted, output signal = 2.83 V_{RMS}	—	127	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	92	102	—	dB
	THD, defined in Table 3-1	P_O = 1.0 W	—	–40	—	dB
	THD+N, defined in Table 3-1	P_O = 1.0 W	—	–40	—	dB
	THD, defined in Table 3-1	P_O = 0.5 W	—	–70	—	dB
	THD+N, defined in Table 3-1	P_O = 0.5 W	—	–70	–60	dB
	Output noise floor	A-weighted	—	1.3	—	μV_{RMS}
	PSRR (DBVDD*n*, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	125 90	— —	dB dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	125 105	— —	dB dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz 100 mV (peak-peak) 10 kHz	— —	120 90	— —	dB dB

Table 3-9. Input/Output Path Characteristics *(Cont.)*

Test conditions (unless specified otherwise): DBVDD1 = DBVDD2 = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 2.5 V (powered from internal LDO); SPKVDD = 4.2 V; T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter			Min	Typ	Max	Units
DAC to speaker output (SPKOUTP+SPKOUTN, Load = 4 Ω, 15 µH, BTL)	Maximum output power	SPKVDD = 5.0 V, 1% THD+N	—	2.7	—	W
		SPKVDD = 4.2 V, 1% THD+N	—	1.9	—	W
		SPKVDD = 3.6 V, 1% THD+N	—	1.4	—	W
	SNR, defined in Table 3-1	A-weighted, output signal = 2.83 V_{RMS}	—	127	—	dB
	Dynamic range, defined in Table 3-1	A-weighted, –60 dBFS input	—	102	—	dB
	THD, defined in Table 3-1	P_O = 1.0 W	—	–71	—	dB
	THD+N, defined in Table 3-1	P_O = 1.0 W	—	–70	—	dB
	THD, defined in Table 3-1	P_O = 0.5 W	—	–71	—	dB
	THD+N, defined in Table 3-1	P_O = 0.5 W	—	–70	—	dB
	Output noise floor	A-weighted	—	1.3	—	μV_{RMS}
	PSRR (DBVDD*n*, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	125	—	dB
		100 mV (peak-peak) 10 kHz	—	90	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	125	—	dB
		100 mV (peak-peak) 10 kHz	—	105	—	dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	120	—	dB
		100 mV (peak-peak) 10 kHz	—	90	—	dB

Table 3-10. Digital Input/Output

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter			Minimum	Typical	Maximum	Units
Digital I/O (except DMICDAT1/2 and DMICCLK1/2) [1,3]	Input HIGH level	V_{DBVDDn} = 1.71–1.98 V	0.75 × DBVDD*n*	—	—	V
		V_{DBVDDn} = 2.5 V ±10%	0.8 × DBVDD*n*	—	—	V
		V_{DBVDDn} = 3.3 V ±10%	0.7 × DBVDD*n*	—	—	V
	Input LOW level	V_{DBVDDn} = 1.71–1.98 V	—	—	0.3 × DBVDD*n*	V
		V_{DBVDDn} = 2.5 V ±10%	—	—	0.25 × DBVDD*n*	V
		V_{DBVDDn} = 3.3 V ±10%	—	—	0.2 × DBVDD*n*	V
	Output HIGH level (I_{OH} = 1 mA)	V_{DBVDDn} = 1.71–1.98 V	0.75 × DBVDD*n*	—	—	V
		V_{DBVDDn} = 2.5 V ±10%	0.65 × DBVDD*n*	—	—	V
		V_{DBVDDn} = 3.3 V ±10%	0.7 × DBVDD*n*	—	—	V
	Output LOW level (I_{OL} = 1mA)	V_{DBVDDn} = 1.71–1.98 V	—	—	0.25 × DBVDD*n*	V
		V_{DBVDDn} = 2.5 V ±10%	—	—	0.3 × DBVDD*n*	V
		V_{DBVDDn} = 3.3 V ±10%	—	—	0.15 × DBVDD*n*	V
	Input capacitance		—	—	5	pF
	Input leakage		–1	—	1	µA
	Pull-up/pull-down resistance (where applicable)		35	—	55	kΩ
DMIC I/O (DMICDAT1/2 and DMICCLK1/2) [2,3]	DMICDAT*n* input HIGH Level		0.65 × V_{SUP}	—	—	V
	DMICDAT*n* input LOW Level		—	—	0.35 × V_{SUP}	V
	DMICCLK*n* output HIGH Level	I_{OH} = 1 mA	0.8 × V_{SUP}	—	—	V
	DMICCLK*n* output LOW Level	I_{OL} = –1 mA	—		0.2 × V_{SUP}	V
	Input capacitance		—	25		pF
	Input leakage		–1	—	1	µA
GPIO*n*	Clock output frequency	GPIO pin as OPCLK or FLL output	—	—	50	MHz

1. Digital I/O is referenced to DBVDD1 or DBVDD2.
2. DMICDAT1/2 and DMICCLK1/2 are referenced to a selectable supply, V_{SUP}, according to the IN*n*_DMIC_SUP fields.
3. Note that digital input pins should not be left unconnected or floating.

Table 3-11. Miscellaneous Characteristics

Test conditions (unless specified otherwise): DBVDD1 = DBVDD2 = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 2.5 V (powered from internal LDO); SPKVDD = 4.2 V; T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

Parameter			Min	Typ	Max	Units
Microphone bias (MICBIAS1A, MICBIAS1B, MICBIAS2A, MICBIAS2B) [1]	Minimum Bias Voltage [2]		—	1.5	—	V
	Maximum Bias Voltage		—	2.8	—	V
	Bias Voltage output step size		—	0.1	—	V
	Bias Voltage accuracy		–5%	—	+5%	V
	Bias Current [3]	Regulator Mode (MICB*n*_BYPASS = 0), $V_{MICVDD} - V_{MICBIAS}$ >200 mV	—	—	2.4	mA
		Bypass Mode (MICB*n*_BYPASS = 1)	—	—	5.0	mA
	Output Noise Density	Regulator Mode (MICB*n*_BYPASS = 0), MICB*n*_LVL = 0x4, Load current = 1 mA, Measured at 1 kHz	—	45	—	nV/√Hz
	Integrated noise voltage	Regulator Mode (MICB*n*_BYPASS = 0), MICB*n*_LVL = 0x4, Load current = 1 mA, 100 Hz to 7 kHz, A-weighted	—	4	—	μV_{RMS}
	PSRR (DBVDD*n*, CPVDD1, AVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	105	—	dB
		100 mV (peak-peak) 10 kHz	—	85	—	dB
	PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	110	—	dB
		100 mV (peak-peak) 10 kHz	—	90	—	dB
	PSRR (SPKVDD), defined in Table 3-1	100 mV (peak-peak) 217 Hz	—	105	—	dB
		100 mV (peak-peak) 10 kHz	—	90	—	dB
	Load capacitance [3]	Regulator Mode (MICB*n*_BYPASS = 0), MICB*n*_EXT_CAP = 0	—	—	50	pF
		Regulator Mode (MICB*n*_BYPASS = 0), MICB*n*_EXT_CAP = 1	0.1	1.0	10	µF
	Output discharge resistance	MICB*nx*_ENA = 0, MICB*nx*_DISCH = 1	—	2	—	kΩ
General-purpose switch [4]	Switch resistance	Switch closed, I = 1 mA	—	25	40	Ω
		Switch open	—	100	—	MΩ
External Accessory Detect	Load impedance detection range: Detection via HPDETL (ACCDET_MODE = 001) or HPDETR (ACCDET_MODE = 010)	HP_IMPEDANCE_RANGE = 00	4	—	30	Ω
		HP_IMPEDANCE_RANGE = 01	8	—	100	Ω
		HP_IMPEDANCE_RANGE = 10	100	—	1000	Ω
		HP_IMPEDANCE_RANGE = 11	1000	—	10000	Ω
	Load impedance detection range: Detection via MICDET1 or MICDET2 pin (ACCDET_MODE = 100)		400	—	6000	Ω
	Load impedance detection accuracy (HP_DACVAL, ACCDET_MODE = 001 or 010)	HP_IMPEDANCE_RANGE = 01 or 10	–5	—	+5	%
		HP_IMPEDANCE_RANGE = 00 or 11	–10	—	+10	%
	Load impedance detection accuracy (HP_LVL, ACCDET_MODE = 001, 010, or 100)		–20	—	+20	%
	Load impedance detection range—Detection via MICDET1 or MICDET2 pin (ACCDET_MODE = 000); 2.2 kΩ (±2%) MICBIAS resistor. [5]	for MICD_LVL[0] = 1	0	—	70	Ω
		for MICD_LVL[1] = 1	110	—	180	Ω
		for MICD_LVL[2] = 1	210	—	290	Ω
		for MICD_LVL[3] = 1	360	—	680	Ω
		for MICD_LVL[8] = 1	1000	—	30000	Ω
	Jack-detection input threshold voltage (JACKDET*n*)	Detection on JACKDET1, Jack insertion	—	0.9	—	V
		Detection on JACKDET1, Jack removal	—	1.65	—	V
		Detection on JACKDET2, Jack insertion	—	0.27	—	V
		Detection on JACKDET2, Jack removal	—	0.9	—	V
	Pull-up resistance (JACKDET*n*)		—	1	—	MΩ
MICVDD Charge Pump and Regulator (CP2 and LDO2)	Output voltage		0.9	2.7	3.3	V
	Programmable output voltage step size	LDO2_VSEL = 0x00–0x14 (0.9–1.4V)	—	25	—	mV
		LDO2_VSEL = 0x14 to 0x27 (1.4 V–3.3 V)	—	100	—	mV
	Maximum output current		—	8	—	mA
	Start-up time	4.7 µF on MICVDD	—	1.5	2.5	ms
Frequency-Locked Loop (FLL1)	Output frequency	FLL output as SYSCLK source	90	—	98.3	MHz
		FLL output as DSPCLK source	135	—	150	MHz
	Lock Time	F_{REF} = 32 kHz, F_{OUT} (DSPCLK source) = 147.456 MHz	—	10	—	ms
		F_{REF} = 12 MHz, F_{OUT} (DSPCLK source) = 147.456 MHz	—	1	—	ms
$\overline{\text{RESET}}$ pin input	$\overline{\text{RESET}}$ input pulse width [6]		1	—	—	µs

1. No capacitor on MICBIAS*n*. In Regulator Mode, it is required that $V_{MICVDD} - V_{MICBIAS}$ > 200 mV.
2. Regulator Mode (MICB*n*_BYPASS = 0), Load current ≤ 1.0 mA.
3. Bias current and load capacitance specifications are per MICBIAS generator (MICBIAS1 or MICBIAS2).
4. The GPSWN pin voltage must not exceed GPSWP + 0.3 V. See Table 3-2 for voltage limits applicable to the GPSWP and GPSWN pins.
5. These characteristics assume no other component is connected to MICDET*n*.
6. To trigger a hardware reset, the $\overline{\text{RESET}}$ input must be asserted for longer than this duration.

Table 3-12. Device Reset Thresholds

The following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter		Symbol	Minimum	Typical	Maximum	Units
AVDD reset threshold	V_{AVDD} rising	V_{AVDD}	—	—	1.66	V
	V_{AVDD} falling		1.06	—	1.44	V
DCVDD reset threshold	V_{DCVDD} rising	V_{DCVDD}	—	—	1.04	V
	V_{DCVDD} falling		0.49	—	0.66	V
DBVDD1 Reset threshold	V_{DBVDD1} rising	V_{DBVDD1}	—	—	1.66	V
	V_{DBVDD1} falling		1.06	—	1.44	V

Note: The reset thresholds are derived from simulations only, across all operational and process corners. Device performance is not assured outside the voltage ranges defined in Table 3-3.

Table 3-13. System Clock and Frequency-Locked Loop (FLL)

The following timing information is valid across the full range of recommended operating conditions.

Parameter			Minimum	Typical	Maximum	Units
Master clock timing (MCLK1, MCLK2) [1]	MCLK cycle time	MCLK as input to FLL, FLL1_REFCLK_DIV = 00	74	—	—	ns
		MCLK as input to FLL, FLL1_REFCLK_DIV = 01	37	—	—	ns
		MCLK as input to FLL, FLL1_REFCLK_DIV = 10	18	—	—	ns
		MCLK as input to FLL, FLL1_REFCLK_DIV = 11	12.5	—	—	ns
		MCLK as direct SYSCLK source	40	—	—	ns
	MCLK duty cycle	MCLK as input to FLL	80:20	—	20:80	%
		MCLK as direct SYSCLK source	60:40	—	40:60	%
Frequency-locked loop (FLL1)	FLL input frequency	FLL1_REFCLK_DIV = 00	0.032	—	13.5	MHz
		FLL1_REFCLK_DIV = 01	0.064	—	27	MHz
		FLL1_REFCLK_DIV = 11	0.128	—	54	MHz
		FLL1_REFCLK_DIV = 11	0.256	—	80	MHz
	FLL synchronizer input frequency	FLL1_SYNCCLK_DIV = 00	0.032	—	13.5	MHz
		FLL1_SYNCCLK_DIV = 01	0.064	—	27	MHz
		FLL1_SYNCCLK_DIV = 10	0.128	—	54	MHz
		FLL1_SYNCCLK_DIV = 11	0.256	—	80	MHz
Internal clocking	SYSCLK frequency	SYSCLK_FREQ = 000, SYSCLK_FRAC = 0	–1%	6.144	+1%	MHz
		SYSCLK_FREQ = 000, SYSCLK_FRAC = 1	–1%	5.6448	+1%	MHz
		SYSCLK_FREQ = 001, SYSCLK_FRAC = 0	–1%	12.288	+1%	MHz
		SYSCLK_FREQ = 001, SYSCLK_FRAC = 1	–1%	11.2896	+1%	MHz
		SYSCLK_FREQ = 010, SYSCLK_FRAC = 0	–1%	24.576	+1%	MHz
		SYSCLK_FREQ = 010, SYSCLK_FRAC = 1	–1%	22.5792	+1%	MHz
		SYSCLK_FREQ = 011, SYSCLK_FRAC = 0	–1%	49.152	+1%	MHz
		SYSCLK_FREQ = 011, SYSCLK_FRAC = 1	–1%	45.1584	+1%	MHz
		SYSCLK_FREQ = 100, SYSCLK_FRAC = 0	–1%	98.304	+1%	MHz
		SYSCLK_FREQ = 100, SYSCLK_FRAC = 1	–1%	90.3168	+1%	MHz
	DSPCLK frequency		5	—	150	MHz

1. If MCLK1 or MCLK2 is selected as a source for SYSCLK (either directly or via the FLL), the frequency must be within 1% of the SYSCLK_FREQ setting.

Table 3-14. Digital Microphone (DMIC) Interface Timing

The following timing information is valid across the full range of recommended operating conditions.

Parameter [1]	Symbol	Minimum	Typical	Maximum	Units
DMICCLK*n* cycle time	t_{CY}	160	163	1432	ns
DMICCLK*n* duty cycle	—	45	—	55	%
DMICCLK*n* rise/fall time (25-pF load, 1.8-V supply)	t_r, t_f	5	—	30	ns
DMICDAT*n* (Left) setup time to falling DMICCLK edge	t_{LSU}	15	—	—	ns
DMICDAT*n* (Left) hold time from falling DMICCLK edge	t_{LH}	0	—	—	ns
DMICDAT*n* (Right) setup time to rising DMICCLK edge	t_{RSU}	15	—	—	ns
DMICDAT*n* (Right) hold time from rising DMICCLK edge	t_{RH}	0	—	—	ns

Note: The voltage reference for the IN1 and IN2 DMIC interfaces is selectable, using the IN*n*_DMIC_SUP fields—each interface may be referenced to MICVDD, MICBIAS1B, MICBIAS2A, or MICBIAS2B levels.

1.DMIC interface timing

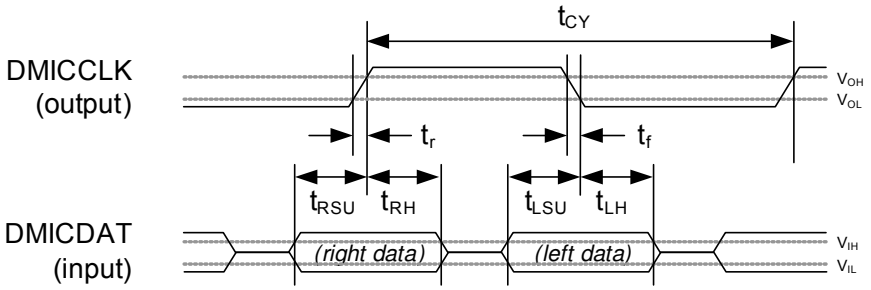
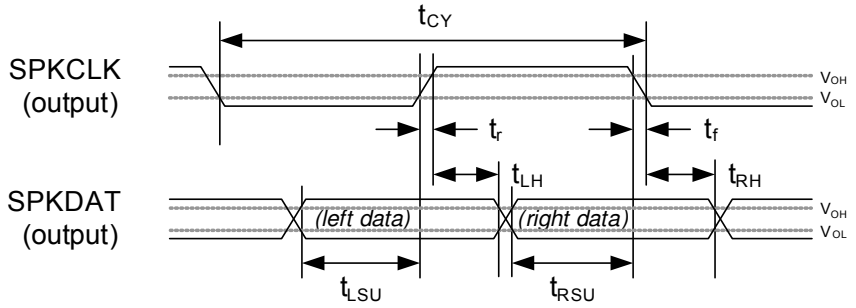


Table 3-15. Digital Speaker (PDM) Interface Timing

The following timing information is valid across the full range of recommended operating conditions.

Parameter		Symbol	Minimum	Typical	Maximum	Units
Mode A [1]	SPKCLK cycle time	t_{CY}	160	163	358	ns
	SPKCLK duty cycle	—	45	—	55	%
	SPKCLK rise/fall time (25-pF load)	t_r, t_f	2	—	8	ns
	SPKDAT set-up time to SPKCLK rising edge (left channel)	t_{LSU}	30	—	—	ns
	SPKDAT hold time from SPKCLK rising edge (left channel)	t_{LH}	30	—	—	ns
	SPKDAT set-up time to SPKCLK falling edge (right channel)	t_{RSU}	30	—	—	ns
	SPKDAT hold time from SPKCLK falling edge (right channel)	t_{RH}	30	—	—	ns
Mode B [2]	SPKCLK cycle time	t_{CY}	160	163	358	ns
	SPKCLK duty cycle	—	45	—	55	%
	SPKCLK rise/fall time (25-pF load)	t_r, t_f	2	—	8	ns
	SPKDAT enable from SPKCLK rising edge (right channel)	t_{REN}	—	—	15	ns
	SPKDAT disable to SPKCLK falling edge (right channel)	t_{RDIS}	—	—	5	ns
	SPKDAT enable from SPKCLK falling edge (left channel)	t_{LEN}	—	—	15	ns
	SPKDAT disable to SPKCLK rising edge (left channel)	t_{LDIS}	—	—	5	ns

1.Digital speaker (PDM) interface timing—Mode A



2. Digital speaker (PDM) interface timing—Mode B

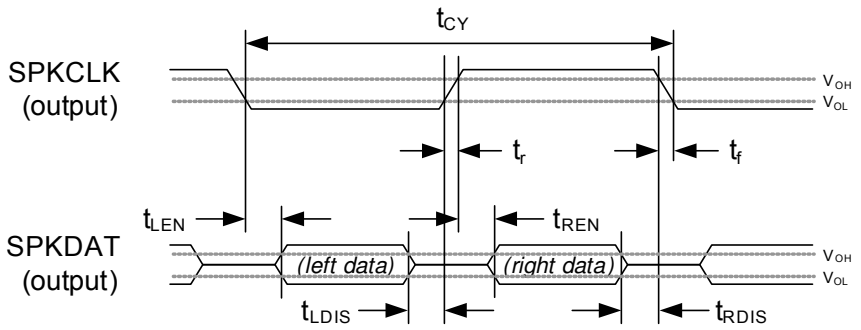


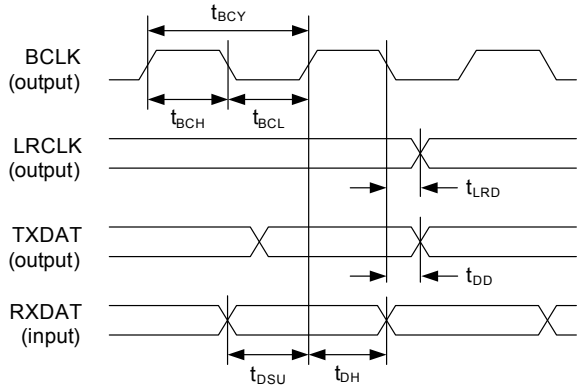
Table 3-16. Digital Audio Interface—Master Mode

Test conditions (unless specified otherwise): C_{LOAD} = 25 pF (output pins); BCLK slew (10% to 90%) = 3.7–5.6 ns; with the exception of the conditions noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter [1]		Symbol	Minimum	Typical	Maximum	Units
Master Mode	AIF*n*BCLK cycle time	t_{BCY}	40	—	—	ns
	AIF*n*BCLK pulse width high	t_{BCH}	18	—	—	ns
	AIF*n*BCLK pulse width low	t_{BCL}	18	—	—	ns
	AIF*n*LRCLK propagation delay from BCLK falling edge [2]	t_{LRD}	0	—	8.3	ns
	AIF*n*TXDAT propagation delay from BCLK falling edge	t_{DD}	0	—	5	ns
	AIF*n*RXDAT setup time to BCLK rising edge	t_{DSU}	11	—	—	ns
	AIF*n*RXDAT hold time from BCLK rising edge	t_{DH}	0	—	—	ns
Master Mode, Slave LRCLK	AIF*n*LRCLK setup time to BCLK rising edge	t_{LRSU}	14	—	—	ns
	AIF*n*LRCLK hold time from BCLK rising edge	t_{LRH}	0	—	—	ns

Note: The descriptions above assume noninverted polarity of AIF*n*BCLK.

1. Digital audio interface timing—Master Mode. Note that BCLK and LRCLK outputs can be inverted if required; the figure shows the default, noninverted polarity.



2. The timing of the AIF*n*LRCLK signal is selectable. If the LRCLK advance option is enabled, the LRCLK transition is timed relative to the preceding BCLK edge. Under the required condition that BCLK is inverted in this case, the LRCLK transition is still timed relative to the falling BCLK edge.

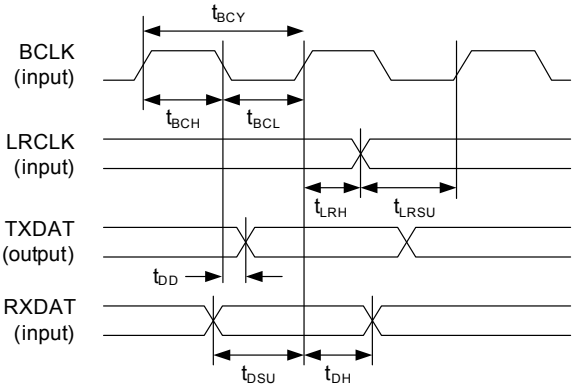
Table 3-17. Digital Audio Interface—Slave Mode

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

Parameter [1,2]		Symbol	Min	Typ	Max	Units
AIF*n*BCLK cycle time		t_{BCY}	40	—	—	ns
AIF*n*BCLK pulse width high	BCLK as direct SYSCLK source	t_{BCH}	16	—	—	ns
	All other conditions	t_{BCH}	14	—	—	ns
AIF*n*BCLK pulse width low	BCLK as direct SYSCLK source	t_{BCL}	16	—	—	ns
	All other conditions	t_{BCL}	14	—	—	ns
C_{LOAD} = 15 pF (output pins), BCLK slew (10%–90%) = 3 ns	AIF*n*LRCLK set-up time to BCLK rising edge	t_{LRSU}	7	—	—	ns
	AIF*n*LRCLK hold time from BCLK rising edge	t_{LRH}	0	—	—	ns
	AIF*n*TXDAT propagation delay from BCLK falling edge	t_{DD}	0	—	12.2	ns
	AIF*n*RXDAT set-up time to BCLK rising edge	t_{DSU}	2	—		ns
	AIF*n*RXDAT hold time from BCLK rising edge	t_{DH}	0	—		ns
	Master LRCLK, AIF*n*LRCLK propagation delay from BCLK falling edge	t_{LRD}	—	—	14.8	ns
C_{LOAD} = 25 pF (output pins), BCLK slew (10%–90%) = 6 ns	AIF*n*LRCLK set-up time to BCLK rising edge	t_{LRSU}	7	—		ns
	AIF*n*LRCLK hold time from BCLK rising edge	t_{LRH}	0	—		ns
	AIF*n*TXDAT propagation delay from BCLK falling edge	t_{DD}	0	—	14.2	ns
	AIF*n*RXDAT set-up time to BCLK rising edge	t_{DSU}	2	—		ns
	AIF*n*RXDAT hold time from BCLK rising edge	t_{DH}	0	—		ns
	Master LRCLK, AIF*n*LRCLK propagation delay from BCLK falling edge	t_{LRD}	—	—	15.9	ns

Note: The descriptions above assume noninverted polarity of AIF*n*BCLK.

1. Digital audio interface timing—Slave Mode. Note that BCLK and LRCLK inputs can be inverted if required; the figure shows the default, noninverted polarity.



2. If AIF*n*BCLK or AIF*n*LRCLK is selected as a source for SYSCLK (either directly or via the FLL), the frequency must be within 1% of the SYSCLK_FREQ setting.

Table 3-18. Digital Audio Interface Timing—TDM Mode

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

Parameter [1]		Min	Typ	Max	Units
Master Mode—C_{LOAD} (AIF*n*TXDAT) = 15 to 25 pF. BCLK slew (10%–90%) = 3.7ns to 5.6 ns.	AIF*n*TXDAT enable time from BCLK falling edge	0	—	—	ns
	AIF*n*TXDAT disable time from BCLK falling edge	—	—	6	ns
Slave Mode—C_{LOAD} (AIF*n*TXDAT) = 15 pF). BCLK slew (10%–90%) = 3 ns	AIF*n*TXDAT enable time from BCLK falling edge	2	—	—	ns
	AIF*n*TXDAT disable time from BCLK falling edge	—	—	12.2	ns
Slave Mode—C_{LOAD} (AIF*n*TXDAT) = 25 pF). BCLK slew (10%–90%) = 6 ns	AIF*n*TXDAT enable time from BCLK falling edge	2	—	—	ns
	AIF*n*TXDAT disable time from BCLK falling edge	—	—	14.2	ns

Note: If TDM operation is used on the AIF*n*TXDAT pins, it is important that two devices do not attempt to drive the AIF*n*TXDAT pin simultaneously. To support this requirement, the AIF*n*TXDAT pins can be configured to be tristated when not outputting data.

1. Digital audio interface timing—TDM Mode. The timing of the AIF*n*TXDAT tristating at the start and end of the data transmission is shown.

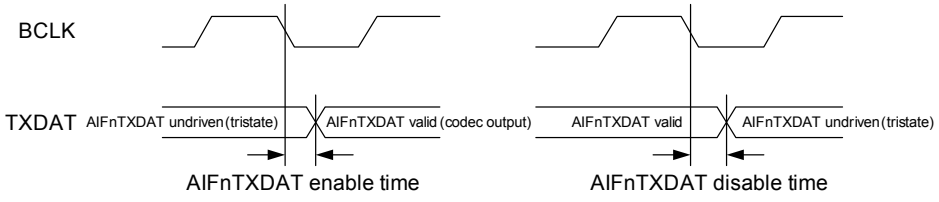


Table 3-19. Control Interface Timing—Two-Wire (I²C) Mode

The following timing information is valid across the full range of recommended operating conditions.

Parameter [1]		Symbol	Min	Typ	Max	Units
SCLK Frequency		—	—	—	3400	kHz
SCLK Low Pulse-Width		t_1	160	—	—	ns
SCLK High Pulse-Width		t_2	100	—	—	ns
Hold Time (Start Condition)		t_3	160	—	—	ns
Setup Time (Start Condition)		t_4	160	—	—	ns
SDA, SCLK Rise Time (10%–90%)	SCLK frequency > 1.7MHz	t_6	—	—	80	ns
	SCLK frequency > 1MHz	t_6	—	—	160	ns
	SCLK frequency ≤ 1MHz	t_6	—	—	2000	ns
SDA, SCLK Fall Time (90%–10%)	SCLK frequency > 1.7MHz	t_7	—	—	60	ns
	SCLK frequency > 1MHz	t_7	—	—	160	ns
	SCLK frequency ≤ 1MHz	t_7	—	—	200	ns
Setup Time (Stop Condition)		t_8	160	—	—	ns
SDA Setup Time (data input)		t_5	40	—	—	ns
SDA Hold Time (data input)		t_9	0	—	—	ns
SDA Valid Time (data/ACK output)	SCLK slew (90%–10%) = 20ns, C_{LOAD} (SDA) = 15 pF	t_{10}	—	—	40	ns
	SCLK slew (90%–10%) = 60ns, C_{LOAD} (SDA) = 100 pF	t_{10}	—	—	130	ns
	SCLK slew (90%–10%) = 160ns, C_{LOAD} (SDA) = 400 pF	t_{10}	—	—	190	ns
	SCLK slew (90%–10%) = 200ns, C_{LOAD} (SDA) = 550 pF	t_{10}	—	—	220	ns
Pulse width of spikes that are suppressed		t_{ps}	0	—	25	ns

1. Control interface timing—I²C Mode

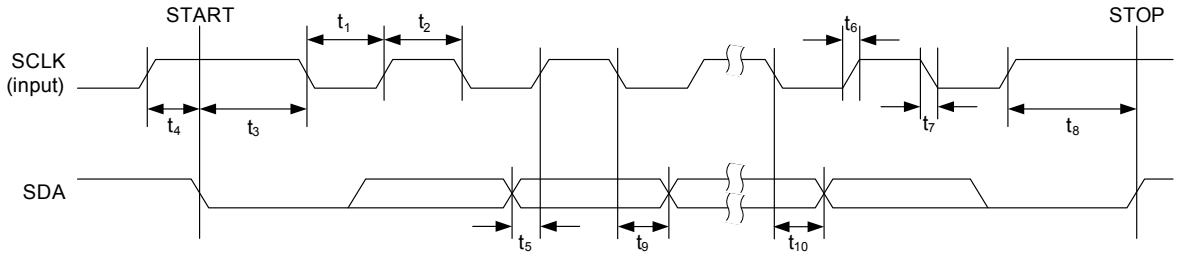
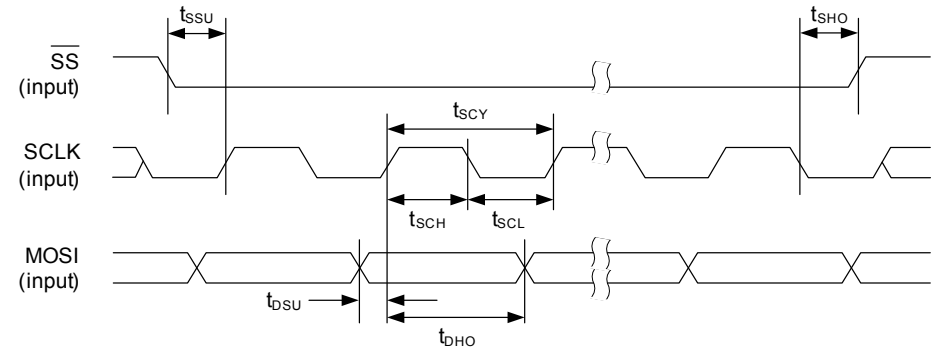


Table 3-20. Control Interface Timing—Four-Wire (SPI) Mode

The following timing information is valid across the full range of recommended operating conditions.

Parameter [1, 2]		Symbol	Min	Typ	Max	Units
$\overline{SS}$ falling edge to SCLK rising edge		t_{SSU}	2.6	—	—	ns
SCLK falling edge to $\overline{SS}$ rising edge		t_{SHO}	0	—	—	ns
SCLK pulse cycle time	SYSCLK disabled (SYSCLK_ENA = 0)	t_{SCY}	50.0	—	—	ns
	SYSCLK_ENA = 1, SYSCLK_FREQ = 000	t_{SCY}	76.8	—	—	ns
	SYSCLK_ENA = 1, SYSCLK_FREQ > 000	t_{SCY}	38.4	—	—	ns
SCLK pulse width low		t_{SCL}	15.3	—	—	ns
SCLK pulse width high		t_{SCH}	15.3	—	—	ns
MOSI to SCLK set-up time		t_{DSU}	1.5	—	—	ns
MOSI to SCLK hold time		t_{DHO}	1.7	—	—	ns
SCLK falling edge to MISO transition	SCLK slew (90%–10%) = 5 ns, C_{LOAD} (MISO) = 25 pF	t_{DL}	0	—	12.6	ns

1. Control interface timing—SPI Mode (write cycle)



2. Control interface timing—SPI Mode (read cycle)

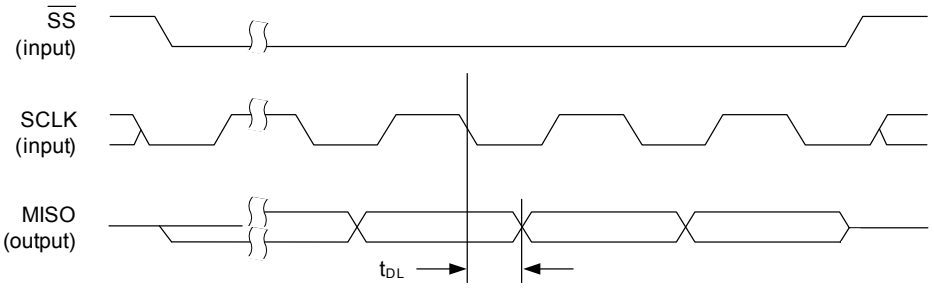


Table 3-21. SLIMbus Interface Timing

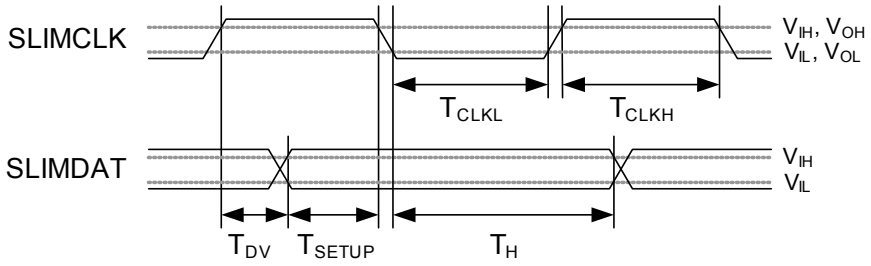
The following timing information is valid across the full range of recommended operating conditions.

Parameter [1]			Symbol	Minimum	Typ	Maximum	Units
SLIMCLK input	SLIMCLK cycle time		—	35	—	—	ns
	SLIMCLK pulse width high		T_{CLKH}	12	—	—	ns
	SLIMCLK pulse width low		T_{CLKL}	12	—	—	ns
SLIMCLK output	SLIMCLK cycle time		—	40	—	—	ns
	SLIMCLK pulse width high		T_{CLKH}	12	—	—	ns
	SLIMCLK pulse width low		T_{CLKL}	12	—	—	ns
	SLIMCLK slew rate (20%–80%)	C_{LOAD} = 15 pF, SLIMCLK_DRV_STR = 0	SR_{CLK}	0.09 x V_{DBVDD1}	—	0.22 x V_{DBVDD1}	V/ns
		C_{LOAD} = 70 pF, SLIMCLK_DRV_STR = 0	SR_{CLK}	0.02 x V_{DBVDD1}	—	0.05 x V_{DBVDD1}	V/ns
		C_{LOAD} = 70 pF, SLIMCLK_DRV_STR = 1	SR_{CLK}	0.04 x V_{DBVDD1}	—	0.11 x V_{DBVDD1}	V/ns
SLIMDAT input	SLIMDAT setup time to SLIMCLK falling edge		T_{SETUP}	3.5	—	—	ns
	SLIMDAT hold time from SLIMCLK falling edge		T_H	2	—	—	ns
SLIMDAT output	SLIMDAT time for data output valid (relative to SLIMCLK rising edge)	SLIMDAT_DRV_STR = 0, DBVDD1 = 1.71 V	T_{DV}	—	4.7	8.1	ns
		C_{LOAD} = 15 pF, SLIMDAT_DRV_STR = 1, DBVDD1 = 1.71 V	T_{DV}	—	4.3	7.3	ns
		C_{LOAD} = 30 pF, SLIMDAT_DRV_STR = 0, DBVDD1 = 1.71 V	T_{DV}	—	6.8	11.8	ns
		C_{LOAD} = 30 pF, SLIMDAT_DRV_STR = 1, DBVDD1 = 1.71 V	T_{DV}	—	5.8	10.0	ns
		C_{LOAD} = 50 pF, SLIMDAT_DRV_STR = 0, DBVDD1 = 1.71 V	T_{DV}	—	9.6	16.6	ns
		C_{LOAD} = 50 pF, SLIMDAT_DRV_STR = 1, DBVDD1 = 1.71 V	T_{DV}	—	7.9	13.7	ns
		C_{LOAD} = 70 pF, SLIMDAT_DRV_STR = 0, DBVDD1 = 1.71 V	T_{DV}	—	12.4	21.5	ns
		C_{LOAD} = 70 pF, SLIMDAT_DRV_STR = 1, DBVDD1 = 1.71 V	T_{DV}	—	10.0	17.4	ns
	SLIMDAT slew rate (20%–80%)	C_{LOAD} = 15 pF, SLIMDAT_DRV_STR = 0	SR_{DATA}	—	—	0.64 x V_{DBVDD1}	V/ns
		C_{LOAD} = 30 pF, SLIMDAT_DRV_STR = 0	SR_{DATA}	—	—	0.35 x V_{DBVDD1}	V/ns
		C_{LOAD} = 30pF, SLIMDAT_DRV_STR = 1	SR_{DATA}	—	—	0.46 x V_{DBVDD1}	V/ns
		C_{LOAD} = 70pF, SLIMDAT_DRV_STR = 0	SR_{DATA}	—	—	0.16 x V_{DBVDD1}	V/ns
		C_{LOAD} = 70pF, SLIMCLK_DRV_STR = 1	SR_{DATA}	—	—	0.21 x V_{DBVDD1}	V/ns
Other parameters	Driver disable time		T_{DD}	—	—	6	ns
	Bus holder output impedance	0.1 x V_{DBVDD1} < V < 0.9 x V_{DBVDD1}	R_{DATAS}	18	—	50	kΩ

Notes:

- The signal timing information describes the timing requirements of the SLIMbus interface as a whole, not just the CS47L35 device.
- T_{DV} is the propagation delay from the rising SLIMCLK edge (at CS47L35 input) to the SLIMDAT output being achieved at the input to all devices across the bus.
- T_{SETUP} is the set-up time for SLIMDAT input (at CS47L35), relative to the falling SLIMCLK edge (at CS47L35).
- T_H is the hold time for SLIMDAT input (at CS47L35) relative to the falling SLIMCLK edge (at CS47L35).
- For more details of the interface timing, refer to the *MIPI Alliance Specification for Serial Low-power Inter-Chip Media Bus (SLIMbus)*

1.SLIMbus interface timing.



V_{IL}, V_{IH} are the 35%/65% levels of the respective inputs.
V_{OL}, V_{OH} are the 20%/80% levels of the respective outputs.
The SLIMDAT output delay (T_{DV}) is with respect to the input pads of all receiving devices

Table 3-22. JTAG Interface Timing

Test conditions (unless specified otherwise): C_{LOAD} = 25 pF (output pins); TCK slew (20%–80%) = 5 ns; with the exception of the conditions noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

Parameter [1]	Symbol	Minimum	Typical	Maximum	Units
TCK cycle time	T_{CCY}	50	—	—	ns
TCK pulse width high	T_{CCH}	20	—	—	ns
TCK pulse width low	T_{CCL}	20	—	—	ns
TMS setup time to TCK rising edge	T_{MSU}	1	—	—	ns
TMS hold time from TCK rising edge	T_{MH}	2	—	—	ns
TDI setup time to TCK rising edge	T_{DSU}	1	—	—	ns
TDI hold time from TCK rising edge	T_{DH}	2	—	—	ns
TDO propagation delay from TCK falling edge	T_{DD}	0	—	17	ns
TRST setup time to TCK rising edge	T_{RSU}	3	—	—	ns
TRST hold time from TCK rising edge	T_{RH}	3	—	—	ns
TRST pulse width low	—	20	—	—	ns

1.JTAG Interface timing

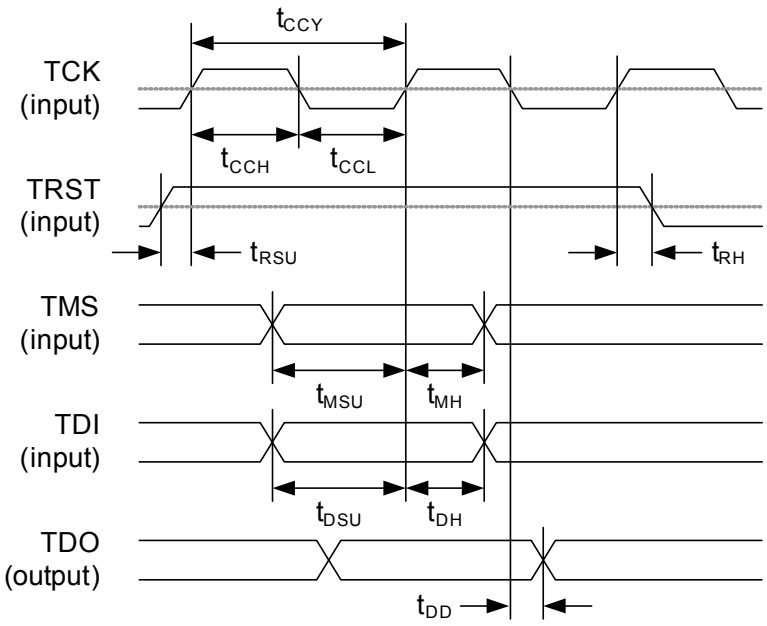


Table 3-23. Typical Power Consumption

Test conditions (unless specified otherwise): DBVDD1 = DBVDD2 = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = Off (CP2 and LDO2 disabled); SPKVDD = 4.2 V; T_A = +25ºC; Fs = 48 kHz; 24-bit audio data, I²S Slave Mode; SYSCLK = 24.576 MHz (direct MCLK1 input).

Operating Configuration			Typical $I_{1.2V}$ (mA)	Typical $I_{1.8V}$ (mA)	Typical $I_{4.2V}$ (mA)	P_{TOT} (mW)
Headphone playback	AIF1 to DAC to HPOUT (stereo), 32-Ω load.	Quiescent	1.00	0.75	0.00	2.54
		1-kHz sine wave, P_O = 10 mW	1.06	36.5	0.00	67.0
Earpiece playback	AIF1 to DAC to EPOUT, 32-Ω load (BTL).	Quiescent	0.86	0.75	0.00	2.38
		1-kHz sine wave, P_O = 30 mW	0.86	61.8	0.00	112
Speaker playback	AIF1 to DAC to SPKOUT, 8-Ω, 22-µH load.	Quiescent	0.76	1.03	0.10	3.19
		1-kHz sine wave, P_O = 700 mW	0.79	1.10	180	759
Stereo line record	Analog line to ADC to AIF1, MICVDD = 1.8V (CP2 and LDO2 bypass enabled).	1-kHz sine wave, -1 dBFS output	1.23	2.52	0.00	6.01
Sleep Mode	Accessory detect enabled (JD1_ENA = 1)		0.000	0.013	0.000	0.023

Table 3-24. Typical Signal Latency

Test conditions (unless specified otherwise): DBVDD1 = DBVDD2 = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = Off (CP2 and LDO2 disabled); SPKVDD = 4.2 V; T_A = +25ºC; Fs = 48 kHz; 24-bit audio data, I²S Slave Mode; SYSCLK = 24.576 MHz (direct MCLK1 input).

Operating Configuration			Latency (µs)
AIF to DAC path	Digital input (AIFn) to analog output (HPOUT). Signal is routed via the ISRC function in the isochronous cases only.	48 kHz input, 48 kHz output, Synchronous	344
		44.1 kHz input, 44.1 kHz output, Synchronous	371
		16 kHz input, 16 kHz output, Synchronous	665
		8 kHz input, 8 kHz output, Synchronous	1105
		8 kHz input, 48 kHz output, Isochronous	1660
		16 kHz input, 48 kHz output, Isochronous	1170
ADC to AIF path	Analog input (INn) to digital output (AIFn). Digital core high-pass filter is included in the signal path. Signal is routed via the ISRC function in the isochronous cases only.	48 kHz input, 48 kHz output, Synchronous	210
		44.1 kHz input, 44.1 kHz output, Synchronous	225
		16 kHz input, 16 kHz output, Synchronous	620
		8 kHz input, 8 kHz output, Synchronous	1210
		8 kHz input, 48 kHz output, Isochronous	1765
		16 kHz input, 48 kHz output, Isochronous	965