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$\pm 2.5\text{ V} / 5\text{ V}$, 50 kSps, 24-bit, High-throughput $\Delta\Sigma$ ADC

Features

- ❑ Differential Analog Input
- ❑ On-chip Buffers for High Input Impedance
- ❑ Conversion Time = 20 μs
- ❑ Settles in One Conversion
- ❑ Linearity Error = 0.0005%
- ❑ Signal-to-Noise = 110 dB
- ❑ 24 Bits, No Missing Codes
- ❑ Simple three/four-wire serial interface
- ❑ Power Supply Configurations:
 - Analog: +5 V / GND; IO: +1.8 V to +3.3 V
 - Analog: $\pm 2.5\text{ V}$; IO: +1.8 V to +3.3 V
- ❑ Power Consumption:
 - ADC Input Buffers On: 90 mW
 - ADC Input Buffers Off: 60 mW

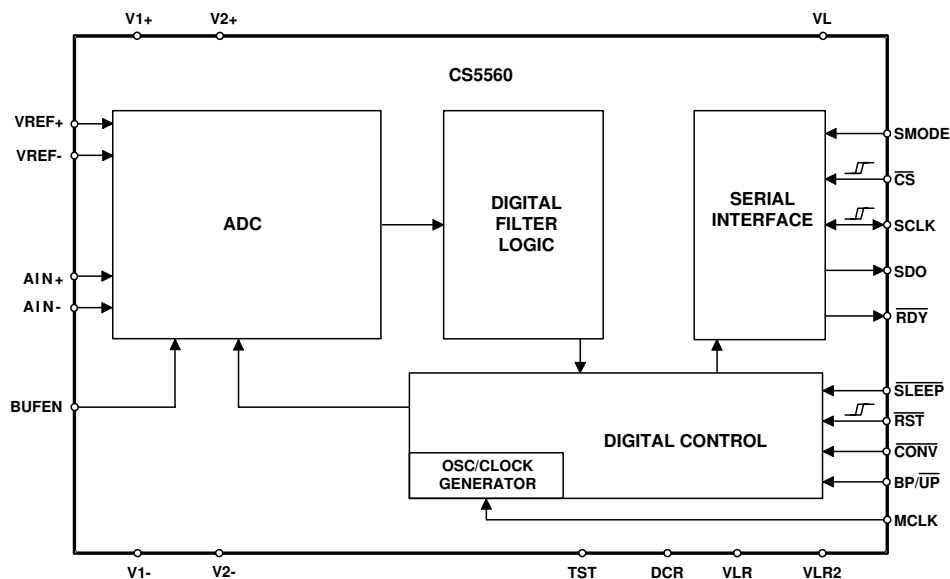
General Description

The CS5560 is a single-channel, 24-bit analog-to-digital converter capable of 50 kSps conversion rate. The input accepts a fully differential analog input signal. On-chip buffers provide high input impedance for both the AIN inputs and the VREF+ input. This significantly reduces the drive requirements of signal sources and reduces errors due to source impedances. The CS5560 is a delta-sigma converter capable of switching multiple input channels at a high rate with no loss in throughput. The ADC uses a low-latency digital filter architecture. The filter is designed for fast settling and settles to full accuracy in one conversion. The converter's 24-bit data output is in serial form, with the serial port acting as either a master or a slave. The converter is designed to support bipolar, ground-referenced signals when operated from $\pm 2.5\text{V}$ analog supplies.

The converter can operate from an analog supply of 0-5V or from $\pm 2.5\text{V}$. The digital interface supports standard logic operating from 1.8, 2.5, or 3.3 V.

ORDERING INFORMATION:

See [Ordering Information](#) on page 32.



Preliminary Product Information

This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS AND SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over the specified operating conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and $T_A = 25^\circ\text{C}$.
- VLR = 0 V. All voltages with respect to 0 V.

ANALOG CHARACTERISTICS $T_A = -40$ to $+85^\circ\text{C}$; $V_{1+} = V_{2+} = +2.5$ V, $\pm 5\%$; $V_{1-} = V_{2-} = -2.5$ V, $\pm 5\%$; $V_L - V_{LR} = 3.3$ V, $\pm 5\%$; $V_{REF} = (V_{REF+}) - (V_{REF-}) = 4.096$ V; $MCLK = 16$ MHz; $SMODE = V_L$. $BUFEN = V_{1+}$ unless otherwise stated. Connected per [Figure 6](#). Bipolar mode unless otherwise stated.

Parameter	Min	Typ	Max	Unit	
Accuracy					
Linearity Error	-	0.0005	-	$\pm\%$ FS	
Differential Linearity Error (Note 1, 2)	-	± 0.1	-	LSB_{24}	
Positive Full-scale Error	-	1.0	-	$\%$ FS	
Negative Full-scale Error	-	1.0	-	$\%$ FS	
Full-scale Drift (Note 2)	-	1	-	ppm / $^\circ\text{C}$	
Unipolar Offset (Note 2)	-	+2000	-	LSB_{24}	
Unipolar Offset Drift (Note 2)	-	2	-	$LSB / ^\circ\text{C}$	
Bipolar Offset (Note 2)	-	± 1000	-	LSB_{24}	
Bipolar Offset Drift (Note 2)	-	1	-	$LSB / ^\circ\text{C}$	
Noise	-	9.5	-	μV_{rms}	
Dynamic Performance					
Peak Harmonic or Spurious Noise	997 Hz, -0.5 dB Input	-	-111	-	dB
Total Harmonic Distortion	997 Hz, -0.5 dB Input	-	-108	-95	dB
Signal-to-Noise		108	110	-	dB
S/(N + D) Ratio	-0.5 dB Input, 997 Hz	95	109	-	dB
	-60 dB Input, 997 Hz	-	50	-	dB
-3 dB Input Bandwidth (Note 3)		-	42	-	kHz

1. No missing codes is guaranteed at 24 bits resolution over the specified temperature range.
2. One LSB is equivalent to $(2 \times V_{REF}) \div 2^{24}$ or $(2 \times 4.096) \div 16,777,216 = 488$ nV.
3. Scales with MCLK.

ANALOG CHARACTERISTICS (CONTINUED) $T_A = -40$ to $+85$ °C; $V_{1+} = V_{2+} = +2.5$ V, $\pm 5\%$; $V_{1-} = V_{2-} = -2.5$ V, $\pm 5\%$; $V_L - V_{LR} = 3.3$ V, $\pm 5\%$; $V_{REF} = (V_{REF+}) - (V_{REF-}) = 4.096$ V; $MCLK = 16$ MHz; $SMODE = V_L$.; $BUFEN = V_{1+}$ unless otherwise stated. Connected per [Figure 6](#).

Parameter		Min	Typ	Max	Unit
Analog Input					
Analog Input Range	Unipolar Bipolar	0 to +VREF $\pm V_{REF}$			V V
Input Capacitance		-	10	-	pF
CVF Current (Note 4)	AIN Buffer On ($BUFEN = V_+$)	-	600	-	nA
	AIN Buffer Off ($BUFEN = V_-$)	-	130	-	μ A
Common Mode Rejection Ratio (CMRR)		116	130	-	dB
Voltage Reference Input					
Voltage Reference Input Range (V_{REF+}) – (V_{REF-})	(Note 5)	2.4	4.096	4.2	V
Input Capacitance		-	10	-	pF
CVF Current	V_{REF+} Buffer On ($BUFEN = V_+$)	-	3	-	μ A
	V_{REF+} Buffer Off ($BUFEN = V_-$)	-	1	-	mA
	V_{REF-}	-	1	-	mA
Power Supplies					
DC Power Supply Currents	I_{V1}	-	-	19	mA
	I_{V2}	-	-	1.8	mA
	I_{V_L}	-	-	0.6	mA
Power Consumption	Normal Operation Buffers On	-	90	106	mW
	Buffers Off	-	60	90	mW
Power Supply Rejection	(Note 6) V_{1+} , V_{2+} Supplies	60	70	-	dB
	V_{1-} , V_{2-} Supplies	60	70	-	dB

4. Measured using an input signal of 1 V DC.

5. For optimum performance, V_{REF+} should always be less than $(V_+) - 0.2$ volts to prevent saturation of the V_{REF+} input buffer.

6. Tested with 100 mVP-P on any supply up to 2 kHz. V_{1+} and V_{2+} supplies at the same voltage potential, V_{1-} and V_{2-} supplies at the same voltage potential.

SWITCHING CHARACTERISTICS

$T_A = -40$ to $+85$ °C; $V_{1+} = V_{2+} = +2.5$ V, $\pm 5\%$; $V_{1-} = V_{2-} = -2.5$ V, $\pm 5\%$;

$V_L - V_{LR} = 3.3$ V, $\pm 5\%$, 2.5 V, $\pm 5\%$, or 1.8 V, $\pm 5\%$

Input levels: Logic 0 = 0V = Low; Logic 1 = V_{D+} = High; $C_L = 15$ pF.

Parameter	Symbol	Min	Typ	Max	Unit	
Master Clock Frequency	Internal Oscillator	XIN	12	14	16	MHz
	External Clock	f_{clk}	0.5	16	16.2	MHz
Master Clock Duty Cycle		40	-	60	%	
Reset						
RST Low Time	t_{res}	1	-	-	μs	
RST rising to RDY falling	Internal Oscillator External Clock	t_{wup}	-	120	-	μs
			-	1536	-	MCLKs
Conversion						
CONV Pulse Width	t_{cpw}	4	-	-	MCLKs	
BP/UP setup to CONV falling	(Note 7)	t_{scn}	0	-	ns	
CONV low to start of conversion	t_{scn}	-	-	2	MCLKs	
Perform Single Conversion (CONV high before RDY falling)	t_{bus}	20	-	-	MCLKs	
Conversion Time	(Note 8) Start of Conversion to RDY falling	t_{buh}	-	-	324	MCLKs
Sleep Mode	SLEEP low to low-power state	t_{con}	-	50	-	μs
	SLEEP high to device active (Note 9)	t_{con}	-	3083	-	MCLKs

7. BP/UP can be changed coincident CONV falling. BP/UP must remain stable until RDY falls.
8. If CONV is held low continuously, conversions occur every 320 MCLK cycles.
If RDY is tied to CONV, conversions will occur every 322 MCLKs.
If CONV is operated asynchronously to MCLK, a conversion may take up to 324 MCLKs.
RDY falls at the end of conversion.
9. RDY will fall when the device is fully operational when coming out of sleep mode.

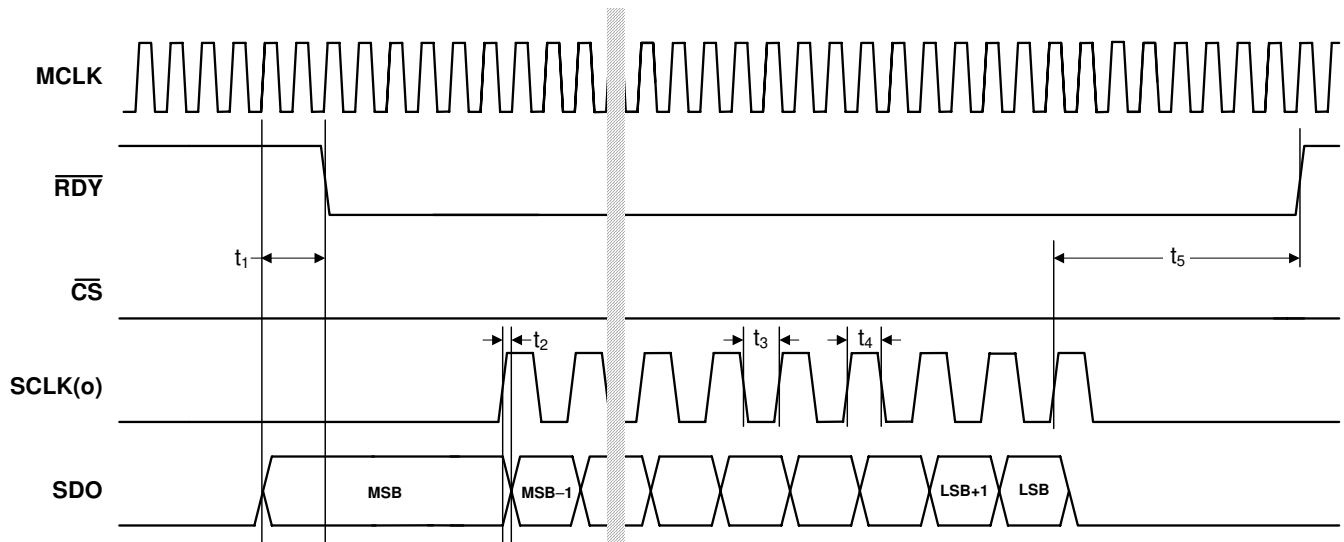
SWITCHING CHARACTERISTICS (CONTINUED)
 $T_A = -40$ to $+85$ °C; $V_{1+} = V_{2+} = +2.5$ V, $\pm 5\%$; $V_{1-} = V_{2-} = -2.5$ V, $\pm 5\%$;

 $V_L - V_{LR} = 3.3$ V, $\pm 5\%$, 2.5 V, $\pm 5\%$, or 1.8 V, $\pm 5\%$

 Input levels: Logic 0 = 0V = Low; Logic 1 = V_{D+} = High; $C_L = 15$ pF.

Parameter	Symbol	Min	Typ	Max	Unit
Serial Port Timing in SSC Mode (SMODE = VL)					
\overline{RDY} falling to MSB stable	t_1	-	-2	-	MCLKs
Data hold time after SCLK rising	t_2	-	10	-	ns
Serial Clock (Out) (Note 10, 11)	Pulse Width (low)	50	-	-	ns
	Pulse Width (high)	50	-	-	ns
\overline{RDY} rising after last SCLK rising	t_5	-	8	-	MCLKs

10. SDO and SCLK will be high impedance when \overline{CS} is high. In some systems SCLK and SDO may require pull-down resistors.
11. $SCLK = MCLK/2$.


Figure 1. SSC Mode - Read Timing, \overline{CS} remaining low (Not to Scale)

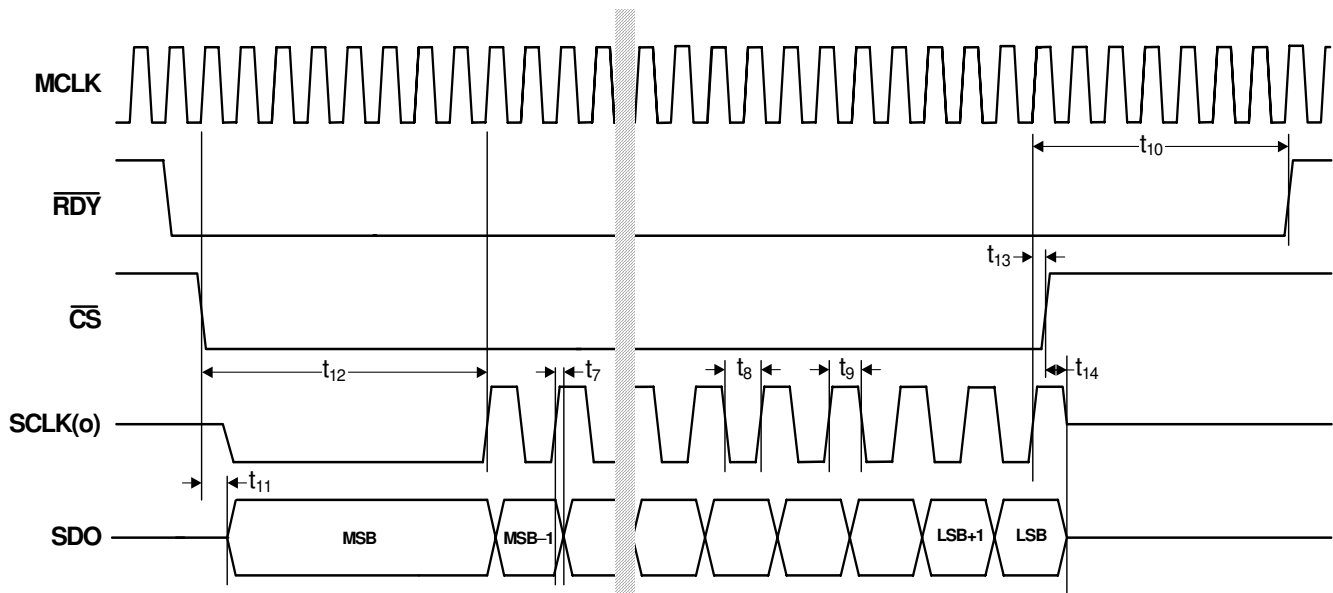
SWITCHING CHARACTERISTICS (CONTINUED)
 $T_A = -40$ to $+85$ °C; $V_{1+} = V_{2+} = +2.5$ V, $\pm 5\%$; $V_{1-} = V_{2-} = -2.5$ V, $\pm 5\%$;

 $V_L - V_{LR} = 3.3$ V, $\pm 5\%$, 2.5 V, $\pm 5\%$, or 1.8 V, $\pm 5\%$

 Input levels: Logic 0 = 0V = Low; Logic 1 = V_{D+} = High; $C_L = 15$ pF.

Parameter	Symbol	Min	Typ	Max	Unit
Serial Port Timing in SSC Mode (SMODE = VL)					
Data hold time after SCLK rising	t_7	-	10	-	ns
Serial Clock (Out) (Note 12, 13)	Pulse Width (low)	50	-	-	ns
	Pulse Width (high)	50	-	-	ns
\overline{RDY} rising after last SCLK rising	t_{10}	-	8	-	MCLKs
\overline{CS} falling to MSB stable	t_{11}	-	10	-	ns
First SCLK rising after \overline{CS} falling	t_{12}	-	8	-	MCLKs
\overline{CS} hold time (low) after SCLK rising	t_{13}	10	-	-	ns
SCLK, SDO tristate after \overline{CS} rising	t_{14}	-	5	-	ns

12. SDO and SCLK will be high impedance when \overline{CS} is high. In some systems it may require a pull-down resistor.
13. $SCLK = MCLK/2$.

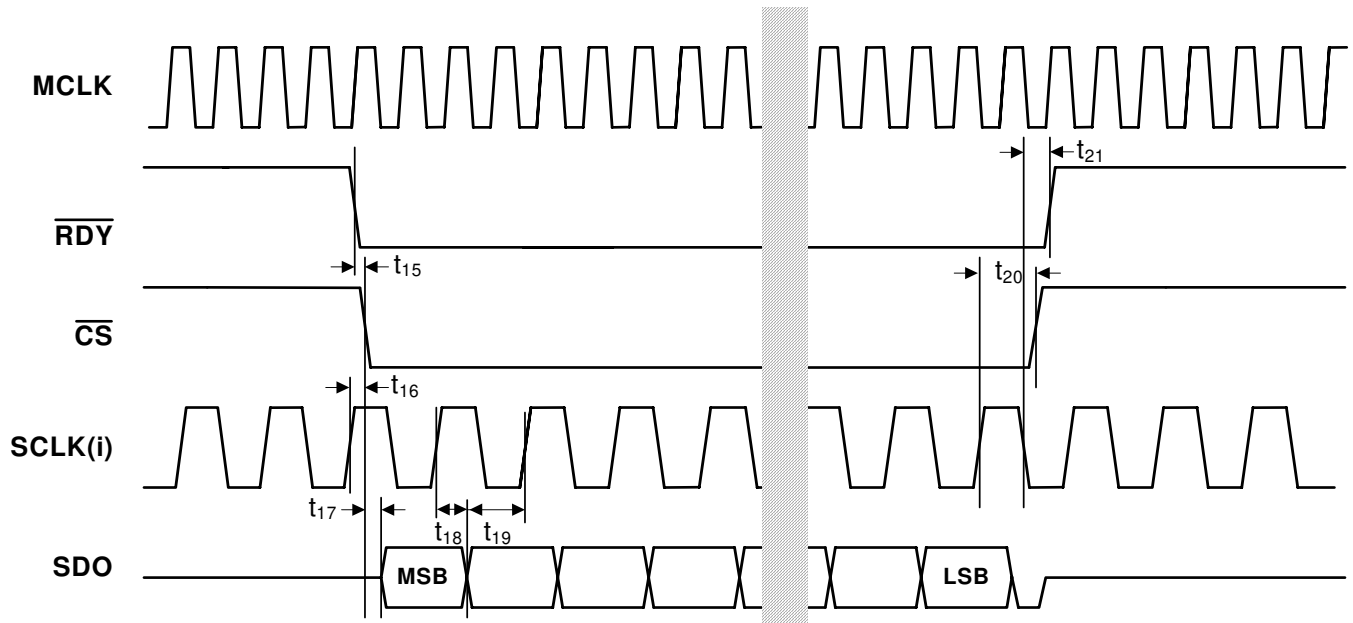

Figure 2. SSC Mode - Read Timing, \overline{CS} falling after \overline{RDY} falls (Not to Scale)

SWITCHING CHARACTERISTICS (CONTINUED)
 $T_A = -40$ to $+85$ °C; $V_{1+} = V_{2+} = +2.5$ V, $\pm 5\%$; $V_{1-} = V_{2-} = -2.5$ V, $\pm 5\%$;

 $V_L - V_{LR} = 3.3$ V, $\pm 5\%$, 2.5 V, $\pm 5\%$, or 1.8 V, $\pm 5\%$

 Input levels: Logic 0 = 0V = Low; Logic 1 = V_{D+} = High; $C_L = 15$ pF.

Parameter	Symbol	Min	Typ	Max	Unit
Serial Port Timing in SEC Mode (SMODE = VLR)					
SCLK(in) Pulse Width (High)	-	30	-	-	ns
SCLK(in) Pulse Width (Low)	-	30	-	-	ns
\overline{CS} hold time (high) after \overline{RDY} falling	t_{15}	10	-	-	ns
\overline{CS} hold time (high) after SCLK rising	t_{16}	10	-	-	ns
\overline{CS} low to SDO out of Hi-Z (Note 14)	t_{17}	-	10	-	ns
Data hold time after SCLK rising	t_{18}	-	10	-	ns
Data setup time before SCLK rising	t_{19}	10	-	-	ns
\overline{CS} hold time (low) after SCLK rising	t_{20}	10	-	$\frac{1}{SCLK} - 10$	ns
\overline{RDY} rising after SCLK falling	t_{21}	-	10	-	ns

 14. SDO will be high impedance when \overline{CS} is high. In some systems it may require a pull-down resistor.

Figure 3. SEC Mode - Continuous SCLK Read Timing (Not to Scale)

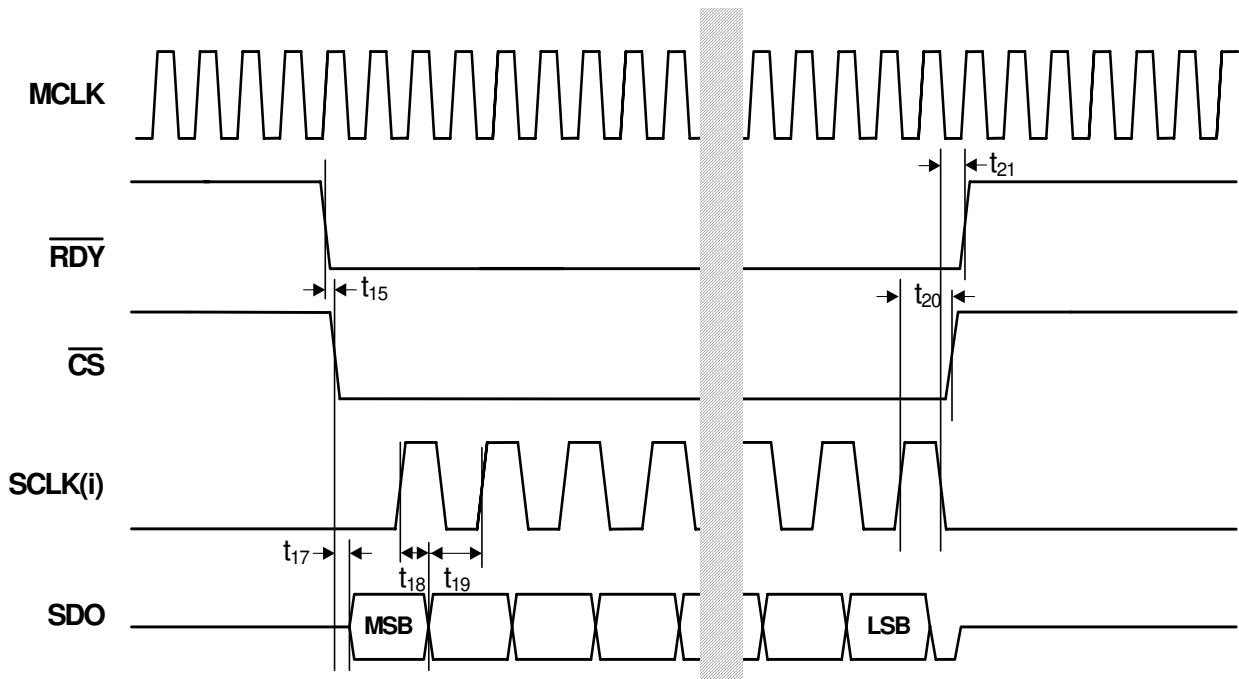


Figure 4. SEC Mode - Discontinuous SCLK Read Timing (Not to Scale)

DIGITAL CHARACTERISTICS

$T_A = T_{MIN}$ to T_{MAX} ; $V_L = 3.3V, \pm 5\%$ or $V_L = 2.5V, \pm 5\%$ or $1.8V, \pm 5\%$; $V_{LR} = 0V$

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current	I_{in}	-	-	2	μA
Digital Input Pin Capacitance	C_{in}	-	3	-	pF
Digital Output Pin Capacitance	C_{out}	-	3	-	pF

DIGITAL FILTER CHARACTERISTICS

$T_A = T_{MIN}$ to T_{MAX} ; $V_L = 3.3V, \pm 5\%$ or $V_L = 2.5V, \pm 5\%$ or $1.8V, \pm 5\%$; $V_{LR} = 0V$

Parameter	Symbol	Min	Typ	Max	Unit
Group Delay	-	-	160	-	MCLKs

GUARANTEED LOGIC LEVELS

$T_A = -40$ to $+85$ °C; $V_{1+} = V_{2+} = +2.5$ V, $\pm 5\%$; $V_{1-} = V_{2-} = -2.5$ V, $\pm 5\%$;

VL - VLR = 3.3 V, $\pm 5\%$, 2.5 V, $\pm 5\%$, or 1.8 V, $\pm 5\%$

Input levels: Logic 0 = 0V = Low; Logic 1 = V_{D+} = High; $C_L = 15$ pF.

Parameter	Sym	VL	Guaranteed Limits			Unit	Conditions
			Min	Typ	Max		
Logic Inputs							
Minimum High-level Input Voltage:	V_{IH}	3.3	1.9			V	
		2.5	1.6				
		1.8	1.2				
Maximum Low-level Input Voltage:	V_{IL}	3.3			1.1	V	
		2.5			0.95		
		1.8			0.6		
Logic Outputs							
Minimum High-level Output Voltage:	V_{OH}	3.3	2.9			V	$I_{OH} = -2$ mA
		2.5	2.1				
		1.8	1.65				
Maximum Low-level Output Voltage:	V_{OL}	3.3			0.36	V	$I_{OH} = -2$ mA
		2.5			0.36		
		1.8			0.44		

RECOMMENDED OPERATING CONDITIONS

(VLR = 0V, see Note 15)

Parameter	Symbol	Min	Typ	Max	Unit	
Single Analog Supply						
DC Power Supplies:	(Note 15)					
V1+	V1+	4.75	5.0	5.25	V	
V2+	V2-	4.75	5.0	5.25	V	
V1-	V1+	-	0	-	V	
V2-	V2-	-	0	-	V	
Dual Analog Supplies						
DC Power Supplies:	(Note 15)					
V1+	V1+	+2.375	+2.5	+2.625	V	
V2+	V2-	+2.375	+2.5	+2.625	V	
V1-	V1+	-2.375	-2.5	-2.625	V	
V2-	V2-	-2.375	-2.5	-2.625	V	
Analog Reference Voltage	(Note 16) [VREF+] – [VREF-]	VREF	2.4	4.096	4.2	V

15. The logic supply can be any value VL – VLR = +1.71 to +3.465 volts as long as VLR ≥ V2- and VL ≤ 3.465 V.

16. The differential voltage reference magnitude is constrained by the V1+ or V1- supply magnitude.

ABSOLUTE MAXIMUM RATINGS

(VLR = 0V)

Parameter	Symbol	Min	Typ	Max	Unit	
DC Power Supplies:						
[V1+] – [V1-] (Note 17)	-	0	-	5.5	V	
VL + [V1-] (Note 18)	-	0	-	6.1	V	
Input Current, Any Pin Except Supplies	(Note 19)	I _{IN}	-	±10	mA	
Analog Input Voltage	(AIN and VREF pins)	V _{INA}	(V1-) – 0.3	-	(V1+) + 0.3	V
Digital Input Voltage		V _{IND}	VLR – 0.3	-	VL + 0.3	V
Storage Temperature		T _{stg}	-65	-	150	°C

Notes: 17. V1+ = V2+; V1- = V2-

18. V1- = V2-

19. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING:

Recommended Operating Conditions indicate limits to which the device is functionally operational. Absolute Maximum Ratings indicate limits beyond which permanent damage to the device may occur. The Absolute Maximum Ratings are stress ratings only and the device should not be operated at these limits. Operation at conditions beyond the Recommended Operating Conditions may affect device reliability, and functional operation beyond Recommended Operating Conditions is not implied. Performance specifications are intended for the conditions specified for each table in the Characteristics and Specifications section.

2. OVERVIEW

The CS5560 is a 24-bit analog-to-digital converter capable of 50 kSps conversion rate. The device is capable of switching multiple input channels at a high rate with no loss in throughput. The ADC uses a low-latency digital filter architecture. The filter is designed for fast settling and settles to full accuracy in one conversion.

The converter is a serial output device. The serial port can be configured to function as either a master or a slave.

The converter can operate from an analog supply of 5V or from $\pm 2.5V$. The digital interface supports standard logic operating from 1.8, 2.5, or 3.3 V.

The CS5560 converts at 50 kSps when operating from a 16 MHz input clock.

3. THEORY OF OPERATION

The converter should be reset after the power supplies and voltage reference are stable.

The CS5560 converter provides high-performance measurement of DC or AC signals. The converter can be used to perform single conversions or continuous conversions upon command. Each conversion is independent of previous conversions and can settle to full specified accuracy, even with a full-scale input voltage step. This is due to the converter architecture which uses a combination of a high-speed delta-sigma modulator and a low-latency filter architecture.

Once power is established to the converter, a reset must be performed. A reset initializes the internal converter logic.

If $\overline{\text{CONV}}$ is held low, the converter will convert continuously with $\overline{\text{RDY}}$ falling every 320 MCLKs. This is equivalent to 50 kSps if $\text{MCLK} = 16.0 \text{ MHz}$. If $\overline{\text{CONV}}$ is tied to $\overline{\text{RDY}}$, a conversion will occur every 322 MCLKs. If $\overline{\text{CONV}}$ is operated asynchronously to MCLK, it may take up to 324 MCLKs from $\overline{\text{CONV}}$ falling to $\overline{\text{RDY}}$ falling.

Multiple converters can operate synchronously if they are driven by the same MCLK source and $\overline{\text{CONV}}$ to each converter falls on the same MCLK falling edge. Alternately, $\overline{\text{CONV}}$ can be held low and all devices can be synchronized if they are reset with $\overline{\text{RST}}$ rising on the same falling edge of MCLK.

The output coding of the conversion word is a function of the BP/ $\overline{\text{UP}}$ pin.

The active-low $\overline{\text{SLEEP}}$ signal causes the device to enter a low-power state. When exiting sleep, the converter will take 3083 MCLK cycles before conversions can be performed. $\overline{\text{RST}}$ should remain inactive (high) when $\overline{\text{SLEEP}}$ is asserted (low).

3.1 Converter Operation

The CS5560 converts at 50 kSps when synchronously operated ($\overline{\text{CONV}} = \text{VLR}$) from a 16.0 MHz master clock. Conversion is initiated by taking $\overline{\text{CONV}}$ low. A conversion lasts 320 master clock cycles, but if $\overline{\text{CONV}}$ is asynchronous to MCLK there may be an uncertainty of 0-4 MCLK cycles after $\overline{\text{CONV}}$ falls to when a conversion actually begins. This may extend the throughput to 324 MCLKs

When the conversion is completed, the output word is placed into the serial port and $\overline{\text{RDY}}$ goes low. To convert continuously, $\overline{\text{CONV}}$ should be held low. In continuous conversion mode with $\overline{\text{CONV}}$ held low, a conversion is performed in 320 MCLK cycles. Alternately $\overline{\text{RDY}}$ can be tied to $\overline{\text{CONV}}$ and a conversion will occur every 322 MCLK cycles.

To perform only one conversion, $\overline{\text{CONV}}$ should return high at least 20 master clock cycles before $\overline{\text{RDY}}$ falls.

Once a conversion is completed and $\overline{\text{RDY}}$ falls, $\overline{\text{RDY}}$ will return high when all the bits of the data word are emptied from the serial port or if the conversion data is not read and $\overline{\text{CS}}$ is held low, $\overline{\text{RDY}}$ will go high two MCLK cycles before the end of conversion. $\overline{\text{RDY}}$ will fall at the end of the next conversion when new data is put into the port register.

See [Serial Port](#) on page 24 for information about reading conversion data.

Conversion performance can be affected by several factors. These include the choice of clock source for the chip, the timing of $\overline{\text{CONV}}$, and the choice of the serial port mode.

The converter can be operated from an internal oscillator. This clock source has greater jitter than an external crystal-based clock. Jitter may not be an issue when measuring DC signals, or very-low-frequency AC signals, but can become an issue for higher frequency AC signals. For maximum performance when digitizing AC signals, a low-jitter MCLK should be used.

To maximize performance, the $\overline{\text{CONV}}$ pin should be held low in the continuous conversion state to perform multiple conversions, or $\overline{\text{CONV}}$ should occur synchronous to MCLK, falling when MCLK falls.

If the converter is operated at maximum throughput, the SSC serial port mode is less likely to cause interference to measurements as the SCLK output is synchronized to the MCLK. Alternately, any interference due to serial port clocking can also be minimized if data is read in the SEC serial port mode when a conversion is not in progress.

3.2 Clock

The CS5560 can be operated from its internal oscillator or from an external master clock. The state of MCLK determines which clock source will be used. If MCLK is tied low, the internal oscillator will start and be used as the clock source for the converter. If an external CMOS-compatible clock is input into MCLK the converter will power down the internal oscillator and use the external clock. If the MCLK pin is held high, the internal oscillator will be held in the stopped state. The MCLK input can be held high to delete clock cycles to aid in synchronizing multiple converters in different phase relationships.

The internal oscillator can be used if the signals to be measured are essentially DC. The internal oscillator exhibits jitter at about 500 picoseconds rms. If the CS5560 is used to digitize AC signals, an external low-jitter clock source should be used.

If the internal oscillator is used as the clock for the CS5560, the maximum conversion rate will be dictated by the oscillator frequency.

If driven from an external MCLK source, the fast rise and fall times of the MCLK signal can result in clock coupling from the internal bond wire of the IC to the analog input. Adding a 50 ohm resistor on the external MCLK source significantly reduces this effect.

3.3 Voltage Reference

The voltage reference for the CS5560 can range from 2.4 volts to 4.2 volts. A 4.096 volt reference is required to achieve the specified performance. [Figure 6](#) and [Figure 7](#) illustrate the connection of the voltage reference with either a single +5 V analog supply or with ± 2.5 V.

For optimum performance, the voltage reference device should be one that provides a capacitor connection to provide a means of noise filtering, or the output should include some type of bandwidth-limiting filter. Some 4.096 volt reference devices need only 5 volts total supply for operation and can be connected as shown in [Figure 6](#) or [Figure 7](#). The reference should have a local bypass capacitor and an appropriate output capacitor.

Some older 4.096 volt reference designs require more headroom and must operate from an input voltage of 5.5 to 6.5 volts. If this type of voltage reference is used ensure that when power is applied to the system, the voltage reference rise time is slower than the rise time of the V1+ and V1- power supply voltage to the converter. An example circuit to slow the output startup time of the reference is illustrated in [Figure 5](#).

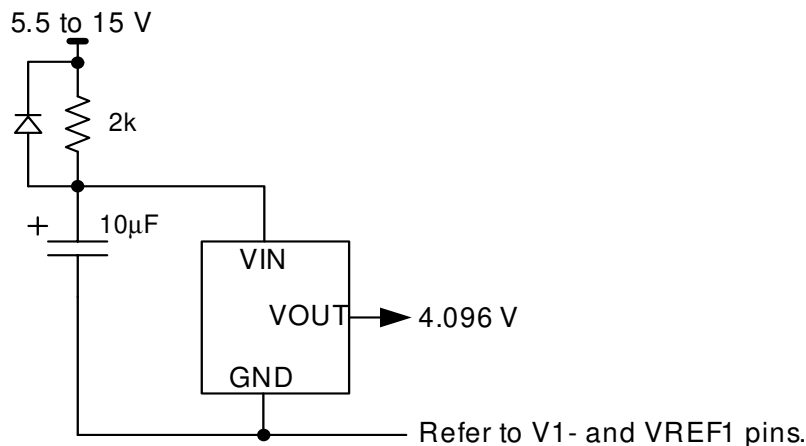


Figure 5. Voltage Reference Circuit

3.4 Analog Input

The analog input of the converter is fully differential with a peak-to-peak input of 4.096 volts on each input. Therefore, the differential, peak-to-peak input is 8.192 volts. This is illustrated in [Figure 6](#) and [Figure 7](#). These diagrams also illustrate a differential buffer amplifier configuration for driving the CS5560.

The capacitors at the outputs of the amplifiers provide a charge reservoir for the dynamic current from the A/D inputs while the resistors isolate the dynamic current from the amplifier. The amplifiers can be powered from higher supplies than those used by the A/D but precautions should be taken to ensure that the op amp output voltage remains within the power supply limits of the A/D, especially under start-up conditions.

3.5 Output Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/UP low), the first code transition occurs 0.5 LSB above zero, and the final code transition occurs 1.5 LSBs below VREF. In the bipolar configuration (BP/UP high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSBs below +VREF. See [Table 1](#) for the output coding of the converter.

Table 1. Output Coding, Two's Complement

Bipolar Input Voltage	Two's Complement
>(VREF-1.5 LSB)	7F FF FF
VREF-1.5 LSB	7F FF FF 7F FF FE
-0.5 LSB	00 00 00 FF FF FF
-VREF+0.5 LSB	80 00 01 80 00 00
<(-VREF+0.5 LSB)	80 00 00

NOTE: VREF = (VREF+) - (VREF-)

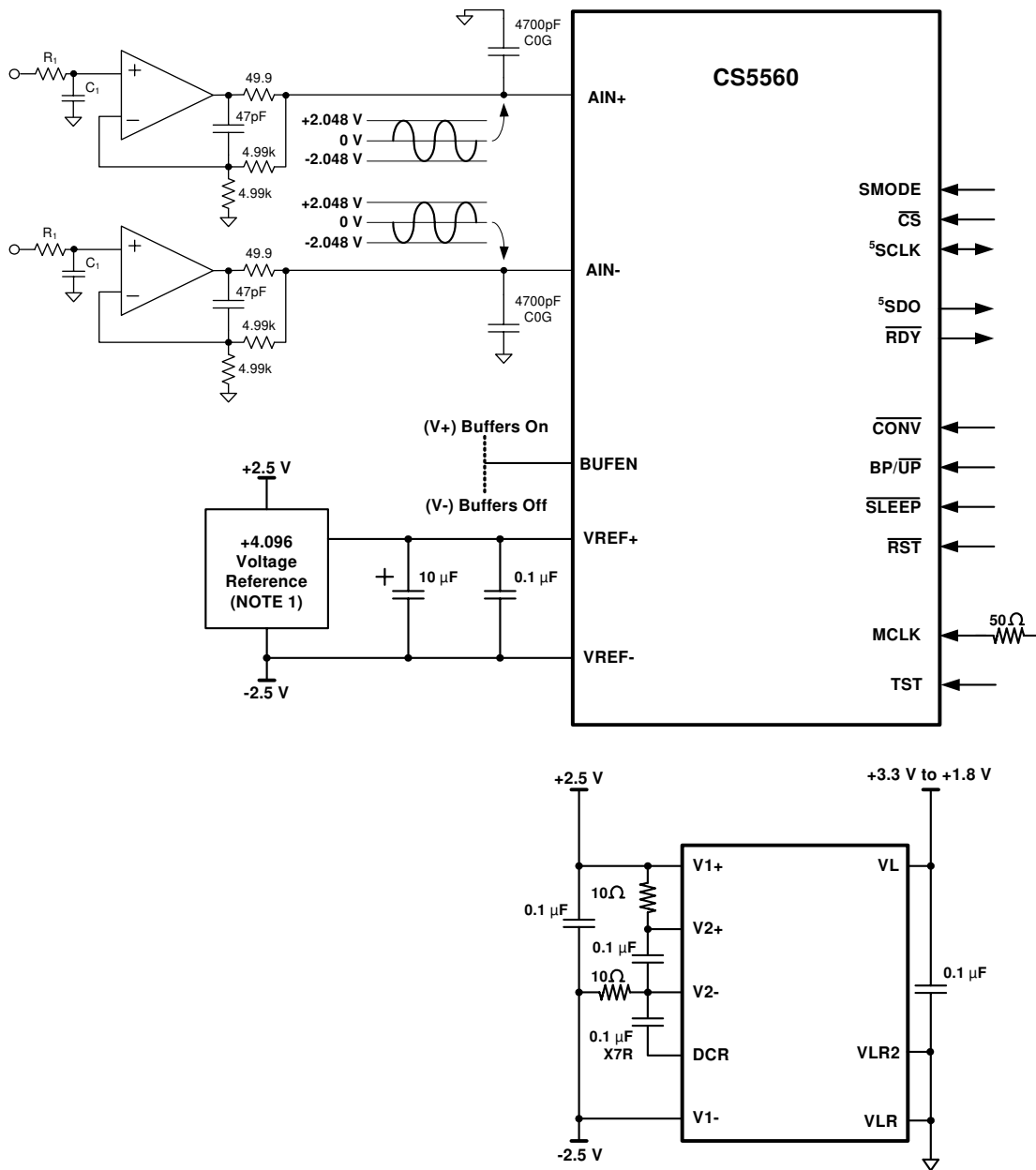
Table 2. Output Coding, Offset Binary

Unipolar Input Voltage	Offset Binary
>(VREF-1.5 LSB)	FF FF FF
VREF-1.5 LSB	FF FF FF FF FF FE
(VREF/2)-0.5 LSB	80 00 00 7F FF FF
+0.5 LSB	00 00 01 00 00 00
<(+0.5 LSB)	00 00 00

NOTE: VREF = (VREF+) - (VREF-)

3.6 Typical Connection Diagrams

The following figure depicts the CS5560 powered from bipolar analog supplies, +2.5 V and -2.5 V.

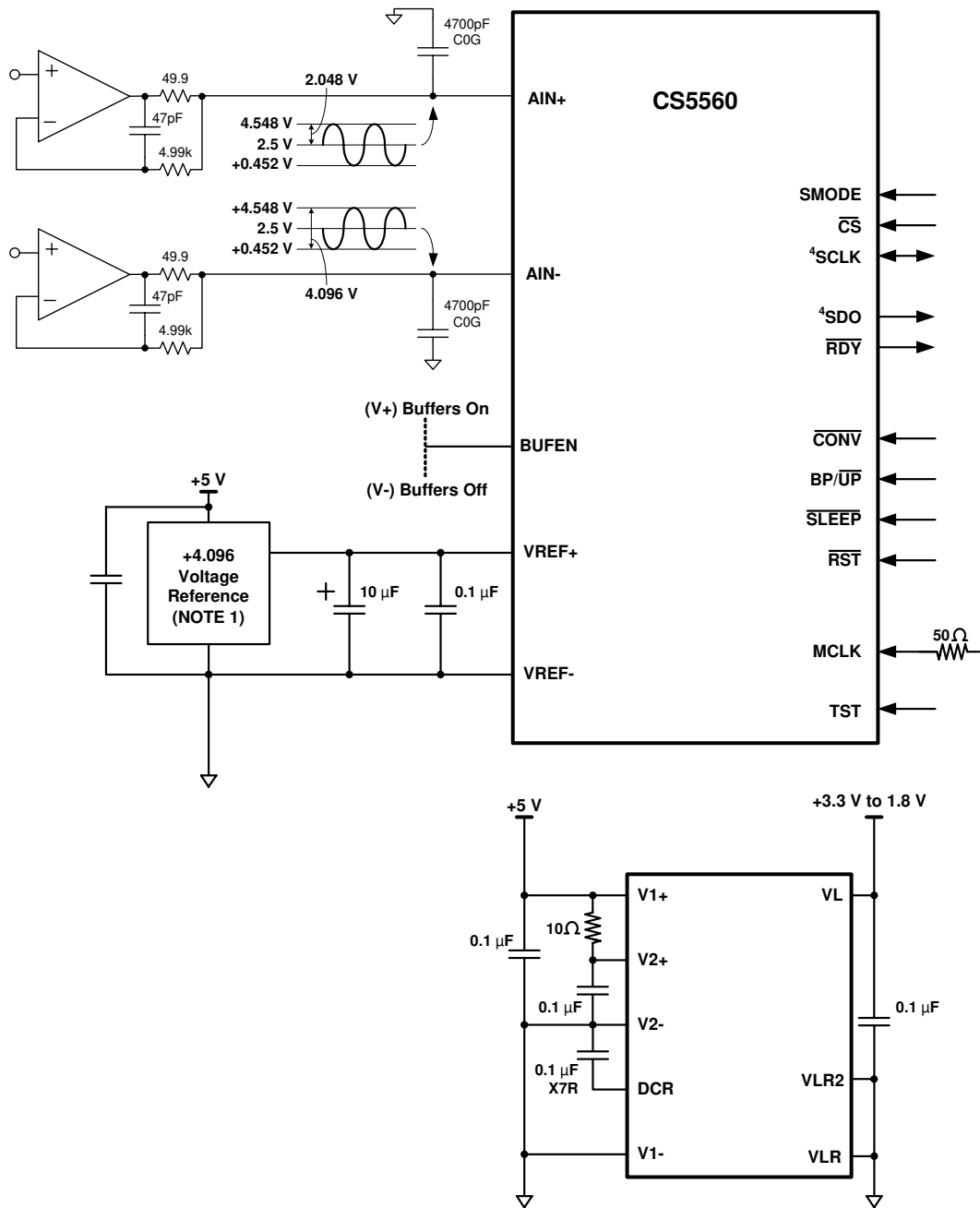


NOTES

1. See Section 3.3 Voltage Reference for information on required voltage reference performance criteria.
2. Locate capacitors so as to minimize loop length.
3. The ± 2.5 V supplies should also be bypassed to ground at the converter.
4. VLR and the power supply ground for the ± 2.5 V should be connected to the same ground plane under the chip.
5. SCLK and SDO may require pull-down resistors in some applications.
6. An RC input filter can be used to band limit the input to reduce noise. Select R to be equal to the parallel combination of the feedback of the feedback resistors $4.99k \parallel 4.99k = 2.5k \leftrightarrow$

Figure 6. CS5560 Configured Using ± 2.5 V Analog Supplies

The following figure depicts the CS5560 device powered from a single 5V analog supply.



NOTES

1. See Section 3.3 Voltage Reference for information on required voltage reference performance criteria.
2. Locate capacitors so as to minimize loop length.
3. V1-, V2-, and VLR should be connected to the same ground plane under the chip.
4. SCLK and SDO may require pull-down resistors in some applications.

Figure 7. CS5560 Configured Using a Single 5V Analog Supply

3.7 AIN & VREF Sampling Structures

The CS5560 uses on-chip buffers on the AIN+, AIN-, and the VREF+ inputs. Buffers provide much higher input impedance and therefore reduce the amount of drive current required from an external source. This helps minimize errors.

The Buffer Enable (BUFEN) pin determines if the on-chip buffers are used or not. If the BUFEN pin is connected to the V1+ supply, the buffers will be enabled. If the BUFEN pin is connected to the V1- pin, the buffers are off. The converter will consume about 30 mW less power when the buffers are off, but the input impedances of AIN+, AIN- and VREF+ will be significantly less than with the buffers enabled.

3.8 Converter Performance

The CS5560 achieves excellent differential nonlinearity (DNL) as shown in Figure 8. Figure 8 illustrates the code widths on the typical scale of ± 1 LSB and on a zoomed scale of ± 0.2 LSB.

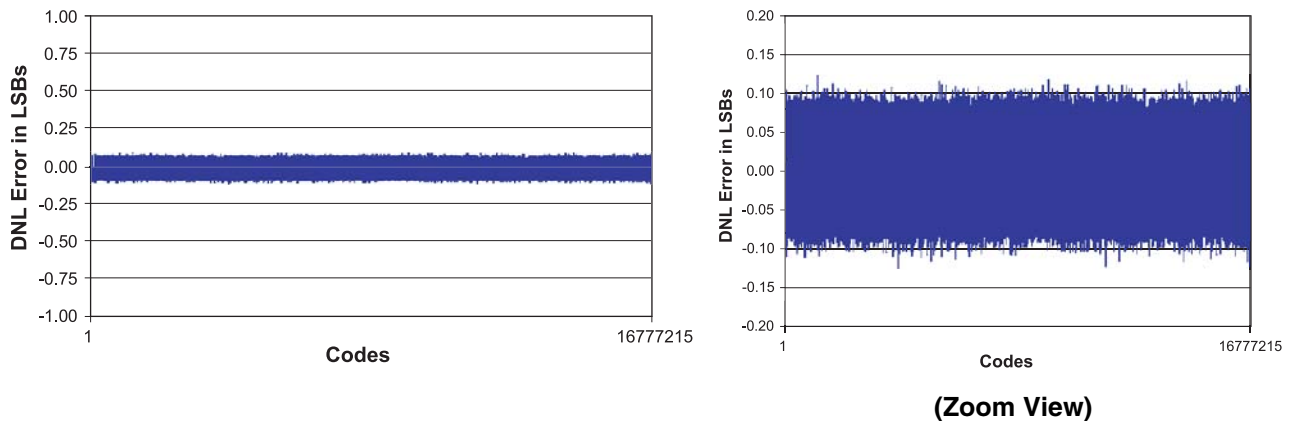


Figure 8. CS5560 DNL Plot

Figure 9 through Figure 16 illustrate the performance of the converter with various input signal magnitudes.

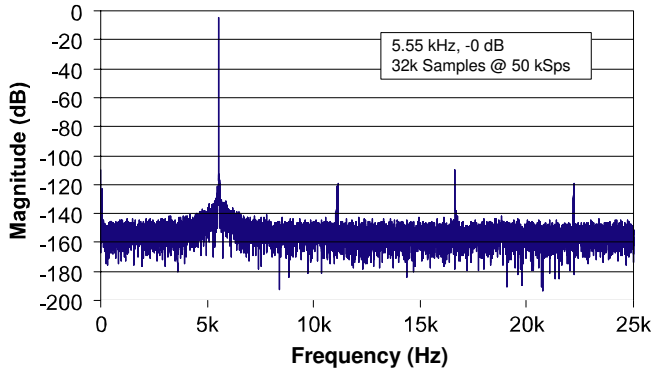


Figure 9. Spectral Performance, 0 dB

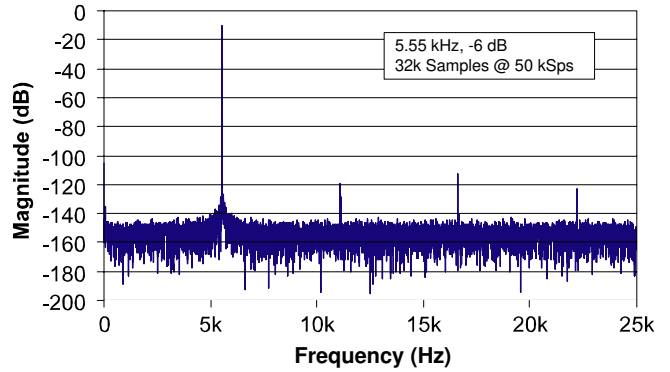


Figure 10. Spectral Performance, -6 dB

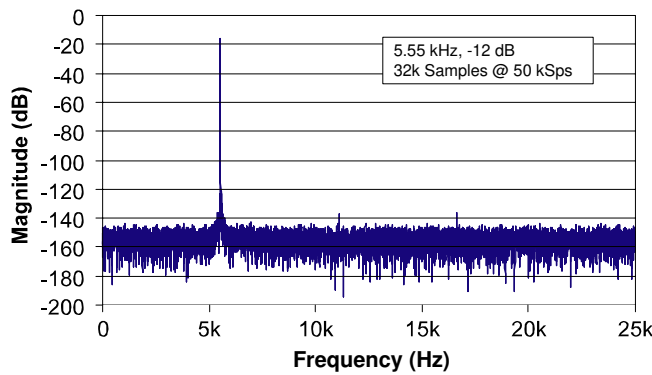


Figure 11. Spectral Performance, -12 dB

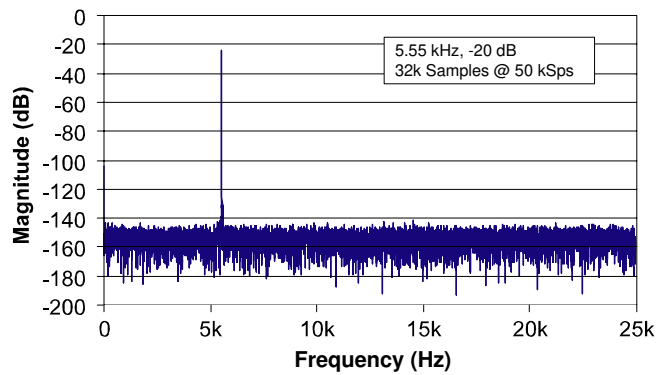


Figure 12. Spectral Performance, -20 dB

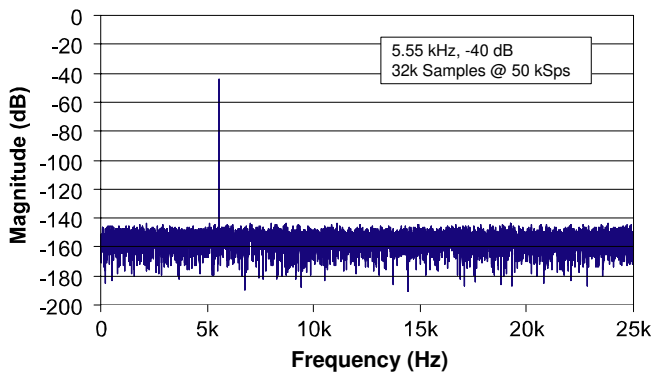


Figure 13. Spectral Performance, -40 dB

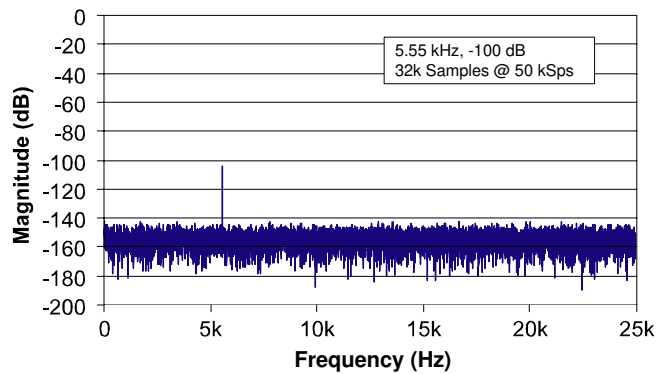


Figure 14. Spectral Performance, -100 dB

Figure 15 illustrates the device with a small signal 1/1,000,000 of full scale. The signal input for figure 14 is about 8.2 microvolts peak to peak, or about 17 codes peak to peak. Figure 16 illustrates the converter with a signal at about 2.6 microvolts peak to peak, or about 5 codes peak to peak. The CS5560 achieves superb performance with this small signal. And the noise floor exhibits no spurious components due to digital interference from the on chip logic.

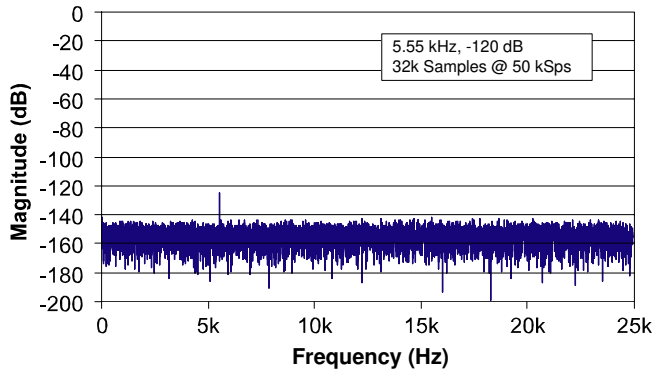


Figure 15. Spectral Performance, -120 dB

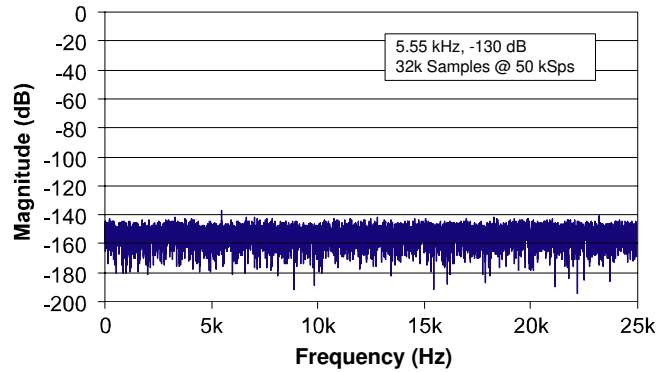


Figure 16. Spectral Performance, -130 dB

Figure 17 illustrates the noise floor of the converter from 0.1 Hz to 25 kHz. While the plot does exhibit some 1/f noise at lower frequencies, the noise floor is entirely free of spurious frequency content due to digital activity inside the chip.

Figure 16 illustrates a noise histogram of 32,768 samples.

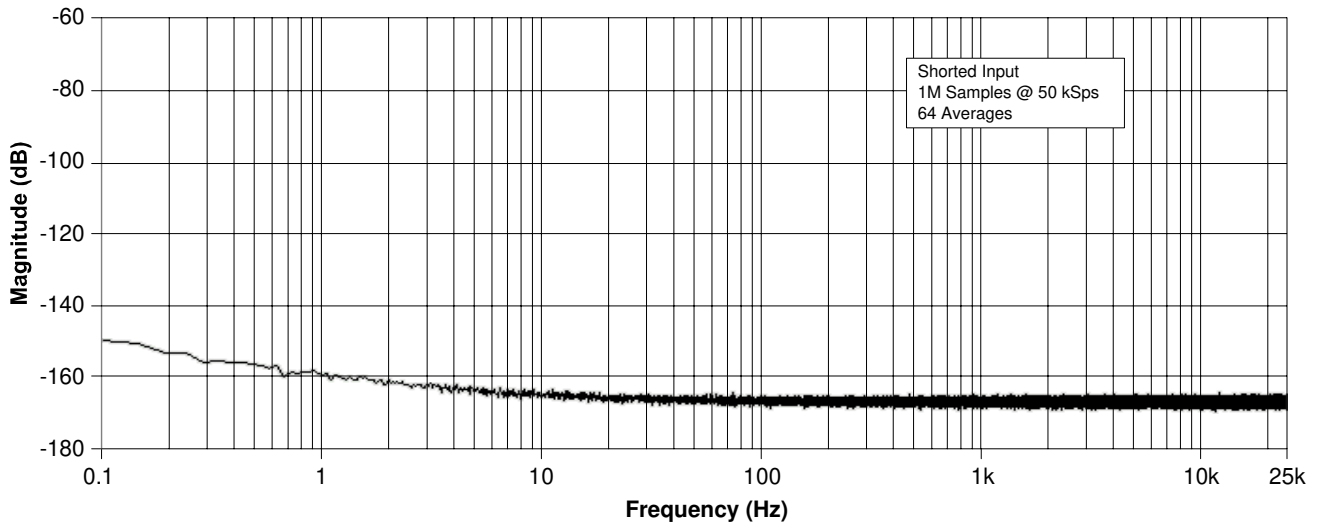


Figure 17. Spectral Plot of Noise with Shorted Input

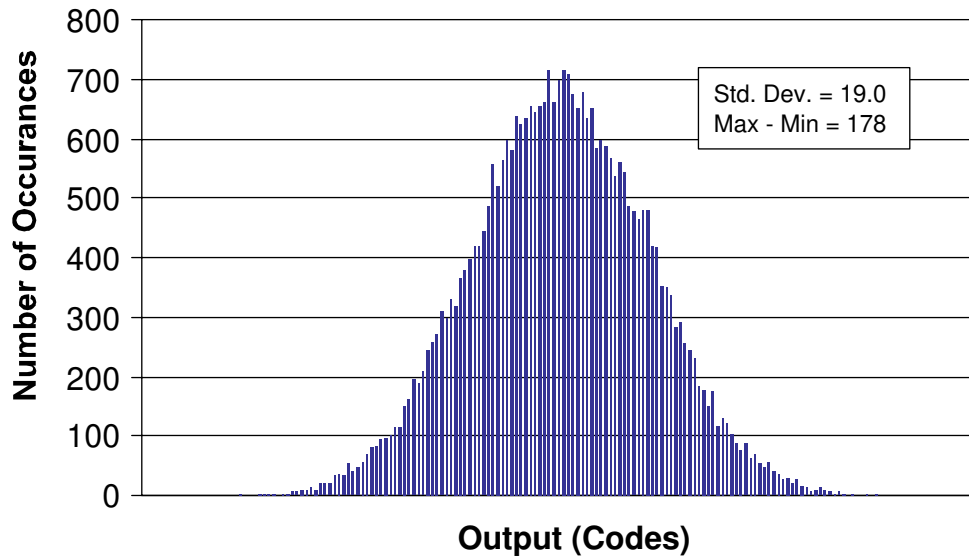


Figure 18. Noise Histogram (32k Samples)

3.9 Digital Filter Characteristics

The digital filter is designed for fast settling, therefore it exhibits very little in-band attenuation. The filter attenuation is 1.040 dB at 25 kHz when sampling at 50 kSps.

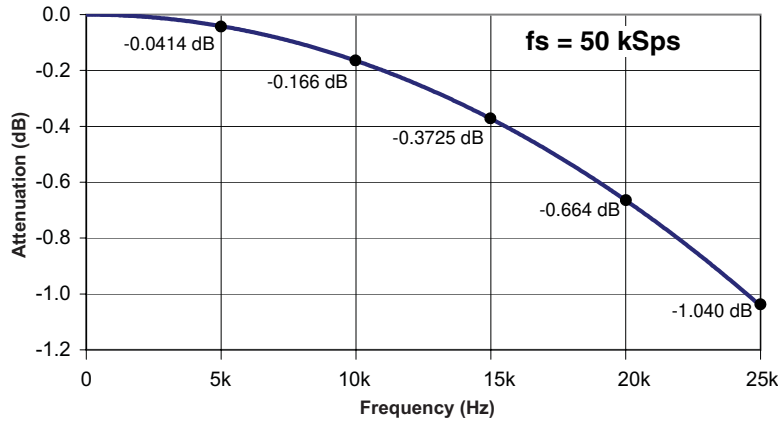


Figure 19. CS5560 Digital Filter Response (DC to fs/2)

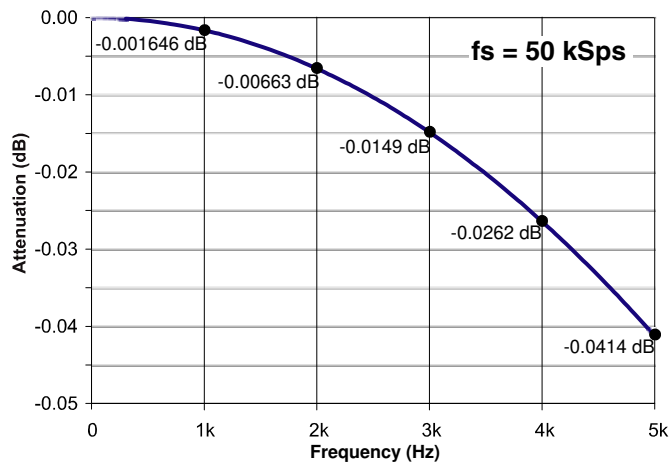


Figure 20. CS5560 Digital Filter Response (DC to 5 kHz)

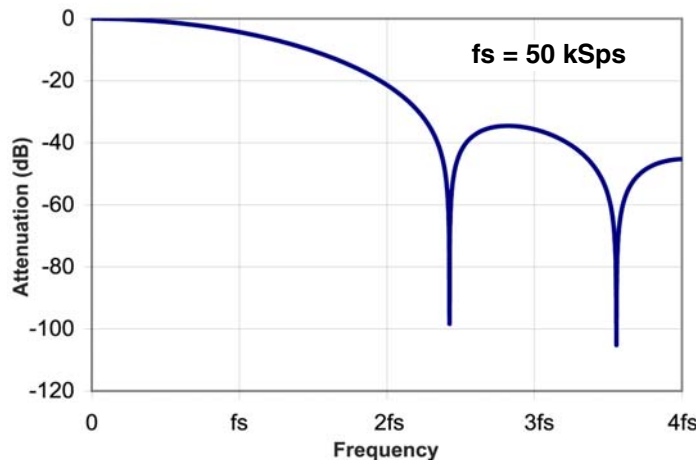


Figure 21. CS5560 Digital Filter Response (DC to 4fs)

3.10 Serial Port

The serial port on the CS5560 can operate in two different modes: synchronous self clock (SSC) mode & synchronous external clock (SEC) mode.

3.10.1 SSC Mode

If the SMODE pin is high (SMODE = VL), the serial port operates in the SSC (Synchronous Self Clock) mode. In the SSC mode the port shifts out conversion data words with SCLK as an output. SCLK is generated inside the converter from MCLK. Data is output from the SDO (Serial Data Output) pin. If \overline{CS} is high, the SDO and SCLK pins will stay in a high-impedance state. If \overline{CS} is low when \overline{RDY} falls, the conversion data word will be output from SDO MSB first. Data is output on the rising edge of SCLK and should be latched into the external logic on the subsequent rising edge of SCLK. When all bits of the conversion word are output from the port the \overline{RDY} signal will return to high.

3.10.2 SEC Mode

If the SMODE pin is low (SMODE = VLR), the serial port operates in the SEC (Synchronous External Clock mode). In this mode, the user usually monitors \overline{RDY} . When \overline{RDY} falls at the end of a conversion, the conversion data word is placed into the output data register in the serial port. \overline{CS} is then activated low to enable data output. Note that \overline{CS} can be held low continuously if it is not necessary to have the SDO output operate in the high impedance state. When \overline{CS} is taken low (after \overline{RDY} falls) the conversion data word is then shifted out of the SDO pin by driving the SCLK pin from system logic external to the converter.

If \overline{CS} is held low continuously, the \overline{RDY} signal will fall at the end of a conversion and the conversion data will be placed into the serial port. If the user starts a read, the user will maintain control over the serial port until the port is empty. However, if SCLK is not toggled, the converter will overwrite the conversion data at the completion of the next conversion. If \overline{CS} is held low and no read is performed, \overline{RDY} will rise just prior to the end of the next conversion and then fall to signal that new data has been written into the serial port.

3.11 Power Supplies & Grounding

The CS5560 can be configured to operate with its analog supply operating from 5V, or with its analog supplies operating from $\pm 2.5\text{V}$. The digital interface supports digital logic operating from either 1.8V, 2.5V, or 3.3V.

[Figure 6](#) on page 17 illustrates the device configured to operate from $\pm 2.5\text{V}$ analog. [Figure 7](#) on page 18 illustrates the device configured to operate from 5V analog.

To maximize converter performance, the analog ground and the logic ground for the converter should be connected at the converter. In the dual analog supply configuration, the analog ground for the $\pm 2.5\text{V}$ supplies should be connected to the VLR pin at the converter with the converter placed entirely over the analog ground plane.

In the single analog supply configuration (+5V), the ground for the +5V supply should be directly tied to the VLR pin of the converter with the converter placed entirely over the analog ground plane. Refer to [Figure 7](#) on page 18.