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$\pm 2.5\text{ V} / 5\text{ V}$, 100 kSps, 16-bit, High-throughput $\Delta\Sigma$ ADC

Features

- ❑ Single-ended Analog Input
- ❑ On-chip Buffers for High Input Impedance
- ❑ Conversion Time = 10 μs
- ❑ Settles in One Conversion
- ❑ Linearity Error = 0.0008%
- ❑ Signal-to-Noise = 92 dB
- ❑ S/(N + D) = 91 dB
- ❑ DNL = ± 0.1 LSB Max.
- ❑ Simple three/four-wire serial interface
- ❑ Power Supply Configurations:
 - Analog: +5V/GND; IO: +1.8V to +3.3V
 - Analog: $\pm 2.5\text{V}$; IO: +1.8V to +3.3V
- ❑ Power Consumption:
 - ADC Input Buffers On: 85 mW
 - ADC Input Buffers Off: 60 mW

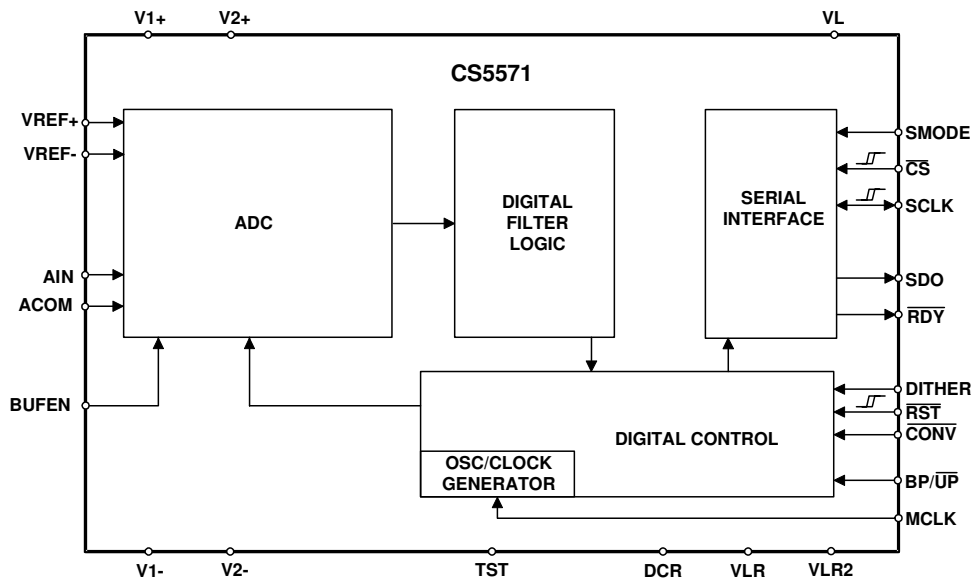
General Description

The CS5571 is a single-channel, 16-bit analog-to-digital converter capable of 100 kSps conversion rate. The input accepts a single-ended analog input signal. On-chip buffers provide high input impedance for both the AIN input and the VREF+ input. This significantly reduces the drive requirements of signal sources and reduces errors due to source impedances. The CS5571 is a delta-sigma converter capable of switching multiple input channels at a high rate with no loss in throughput. The ADC uses a low-latency digital filter architecture. The filter is designed for fast settling and settles to full accuracy in one conversion. The converter's 16-bit data output is in serial format, with the serial port acting as either a master or a slave. The converter is designed to support bipolar, ground-referenced signals when operated from $\pm 2.5\text{V}$ analog supplies.

The converter can operate from an analog supply of 0-5V or from $\pm 2.5\text{V}$. The digital interface supports standard logic operating from 1.8, 2.5, or 3.3 V.

ORDERING INFORMATION:

See [Ordering Information](#) on page 34.



Preliminary Product Information

This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS AND SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over the specified operating conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and $T_A = 25^\circ\text{C}$.
- $V_{LR} = 0\text{ V}$. All voltages measured with respect to 0 V.

ANALOG CHARACTERISTICS $T_A = -40$ to $+85^\circ\text{C}$; $V_{1+} = V_{2+} = +2.5\text{ V}$, $\pm 5\%$; $V_{1-} = V_{2-} = -2.5\text{ V}$, $\pm 5\%$; $V_L - V_{LR} = 3.3\text{ V}$, $\pm 5\%$; $V_{REF} = (V_{REF+}) - (V_{REF-}) = 4.096\text{V}$; $MCLK = 16\text{ MHz}$; $S_{MODE} = V_L$. $DITHER = V_L$ unless otherwise stated; $BUFEN = V_{1+}$ unless otherwise stated. Connected per [Figure 6](#). Bipolar mode unless otherwise stated.

Parameter	Min	Typ	Max	Unit	
Accuracy					
Linearity Error	-	0.0008	-	$\pm\%FS$	
Differential Linearity Error (Note 1)	-	-	± 0.1	LSB_{16}	
Positive Full-scale Error	-	1.0	-	$\%FS$	
Negative Full-scale Error	-	1.0	-	$\%FS$	
Full-scale Drift (Note 2, 3)	-	± 1	-	LSB_{16}	
Bipolar Offset (Note 2)	-	± 15	-	LSB_{16}	
Bipolar Offset Drift (Note 2, 3)	-	± 1	-	LSB_{16}	
Noise (Note 4)	-	36	-	μV_{rms}	
Dynamic Performance					
Peak Harmonic or Spurious Noise	1 kHz, -0.5 dB Input	-	-96	-	dB
	12 kHz, -0.5 dB Input	-	-96	-	dB
Total Harmonic Distortion	1 kHz, -0.5 dB Input	-	-94	-82	dB
Signal-to-Noise		91	92	-	dB
S/(N + D) Ratio	-0.5 dB Input, 1 kHz	-	91	-	dB
	-60 dB Input, 1 kHz	-	32	-	dB
-3 dB Input Bandwidth (Note 5)	-	84	-	kHz	

1. No missing codes is guaranteed at 16 bits resolution over the specified temperature range.
2. One LSB is equivalent to $V_{REF} \div 2^{16}$ or $4.096 \div 65536 = 62.5\ \mu\text{V}$.
3. Total drift over specified temperature range after [reset](#) at power-up, at 25°C .
4. With $DITHER$ off the output will be dominated by quantization.
5. Scales with $MCLK$.

ANALOG CHARACTERISTICS (CONTINUED) $T_A = -40$ to $+85$ °C; $V_{1+} = V_{2+} = +2.5$ V, $\pm 5\%$; $V_{1-} = V_{2-} = -2.5$ V, $\pm 5\%$; $V_L - V_{LR} = 3.3$ V, $\pm 5\%$; $V_{REF} = (V_{REF+}) - (V_{REF-}) = 4.096$ V; $MCLK = 16$ MHz; $SMODE = V_L$. $DITHER = V_L$ unless otherwise stated; $BUFEN = V_{1+}$ unless otherwise stated. Connected per [Figure 6](#).

Parameter		Min	Typ	Max	Unit
Analog Input					
Analog Input Range	Unipolar Bipolar		0 to $+V_{REF} / 2$ $\pm V_{REF} / 2$		V V
Input Capacitance		-	10	-	pF
CVF Current (Note 6)	AIN Buffer On ($BUFEN = V_{+}$)	-	600	-	nA
	AIN Buffer Off ($BUFEN = V_{-}$)	-	130	-	μ A
	ACOM	-	130	-	μ A
Voltage Reference Input					
Voltage Reference Input Range (V_{REF+}) – (V_{REF-})	(Note 7)	2.4	4.096	4.2	V
Input Capacitance		-	10	-	pF
CVF Current	V_{REF+} Buffer On ($BUFEN = V_{+}$)	-	3	-	μ A
	V_{REF+} Buffer Off ($BUFEN = V_{-}$)	-	1	-	mA
	V_{REF-}	-	1	-	mA
Power Supplies					
DC Power Supply Currents	I_{V1}	-	-	18	mA
	I_{V2}	-	-	1.8	mA
	I_{VL}	-	-	0.6	mA
Power Consumption	Normal Operation Buffers On	-	85	101	mW
	Normal Operation Buffers Off	-	60	80	mW
Power Supply Rejection	(Note 8) V_{1+} , V_{2+} Supplies	-	80	-	dB
	V_{1-} , V_{2-} Supplies	-	80	-	dB

6. Measured using an input signal of 1 V DC.

7. For optimum performance, V_{REF+} should always be less than $(V_{+}) - 0.2$ volts to prevent saturation of the V_{REF+} input buffer.

8. Tested with 100 mVp-p on any supply up to 1 kHz. V_{1+} and V_{2+} supplies at the same voltage potential, V_{1-} and V_{2-} supplies at the same voltage potential.

SWITCHING CHARACTERISTICS

$T_A = -40$ to $+85$ °C; $V_{1+} = V_{2+} = +2.5$ V, $\pm 5\%$; $V_{1-} = V_{2-} = -2.5$ V, $\pm 5\%$;

$V_L - V_{LR} = 3.3$ V, $\pm 5\%$, 2.5 V, $\pm 5\%$, or 1.8 V, $\pm 5\%$

Input levels: Logic 0 = 0V = Low; Logic 1 = V_{D+} = High; $C_L = 15$ pF.

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	Internal Oscillator	XIN	12	14	16	MHz
	External Clock	f_{clk}	0.5	16	16.2	MHz
Master Clock Duty Cycle			40	-	60	%
Reset						
RST Low Time	(Note 9)	t_{res}	1	-	-	μ s
RST rising to RDY falling	Internal Oscillator	t_{wup}	-	120	-	μ s
	External Clock		-	1536	-	MCLKs
Conversion						
CONV Pulse Width		t_{cpw}	4	-	-	MCLKs
BP/UP setup to CONV falling	(Note 10)	t_{scn}	0	-	-	ns
CONV low to start of conversion		t_{scn}	-	-	2	MCLKs
Perform Single Conversion (CONV high before RDY falling)		t_{bus}	20	-	-	MCLKs
Conversion Time	(Note 11) Start of Conversion to RDY falling	t_{buh}	-	-	164	MCLKs

9. Reset must not be released until the power supplies and the voltage reference are within specification.

10. BP/UP can be changed coincident to CONV falling. BP/UP must remain stable until RDY falls.

11. If CONV is held low continuously, conversions occur every 160 MCLK cycles.

If RDY is tied to CONV, conversions will occur every 162 MCLKs.

If CONV is operated asynchronously to MCLK, a conversion may take up to 164 MCLKs.

RDY falls at the end of conversion.

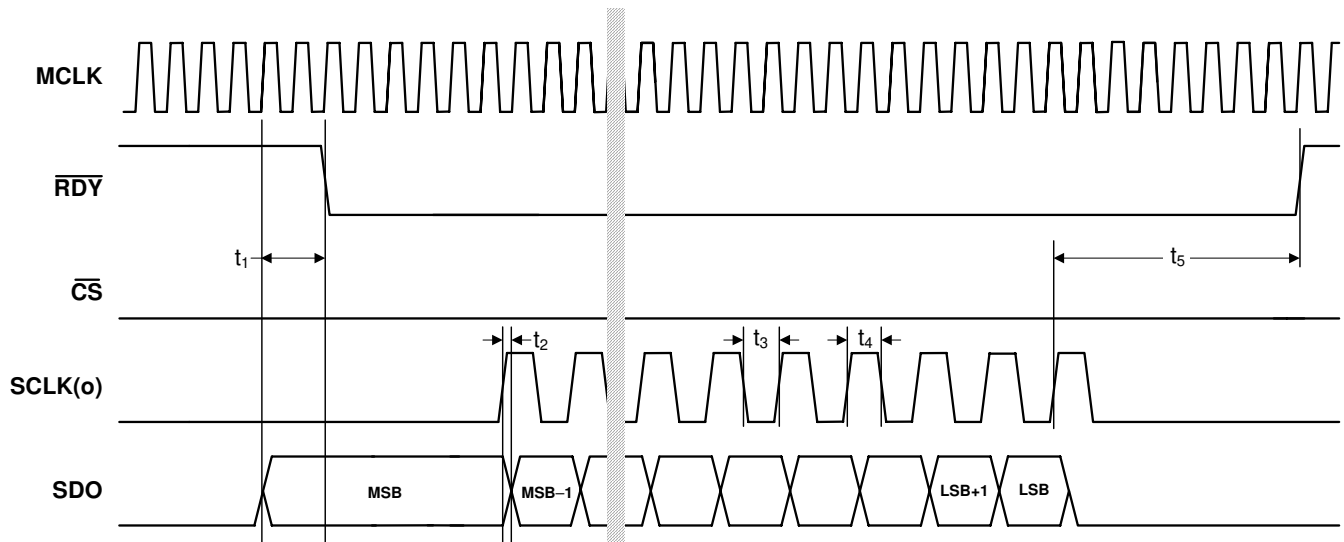
SWITCHING CHARACTERISTICS (CONTINUED)
 $T_A = -40$ to $+85$ °C; $V_{1+} = V_{2+} = +2.5$ V, $\pm 5\%$; $V_{1-} = V_{2-} = -2.5$ V, $\pm 5\%$;

 $V_L - V_{LR} = 3.3$ V, $\pm 5\%$, 2.5 V, $\pm 5\%$, or 1.8 V, $\pm 5\%$

 Input levels: Logic 0 = 0V = Low; Logic 1 = V_{D+} = High; $C_L = 15$ pF.

Parameter	Symbol	Min	Typ	Max	Unit
Serial Port Timing in SSC Mode (SMODE = VL)					
\overline{RDY} falling to MSB stable	t_1	-	-2	-	MCLKs
Data hold time after SCLK rising	t_2	-	10	-	ns
Serial Clock (Out) (Note 12, 13)	Pulse Width (low)	50	-	-	ns
	Pulse Width (high)	50	-	-	ns
\overline{RDY} rising after last SCLK rising	t_5	-	8	-	MCLKs

12. SDO and SCLK will be high impedance when \overline{CS} is high. In some systems SCLK and SDO may require pull-down resistors.
13. $SCLK = MCLK/2$.


Figure 1. SSC Mode - Read Timing, \overline{CS} remaining low (Not to Scale)

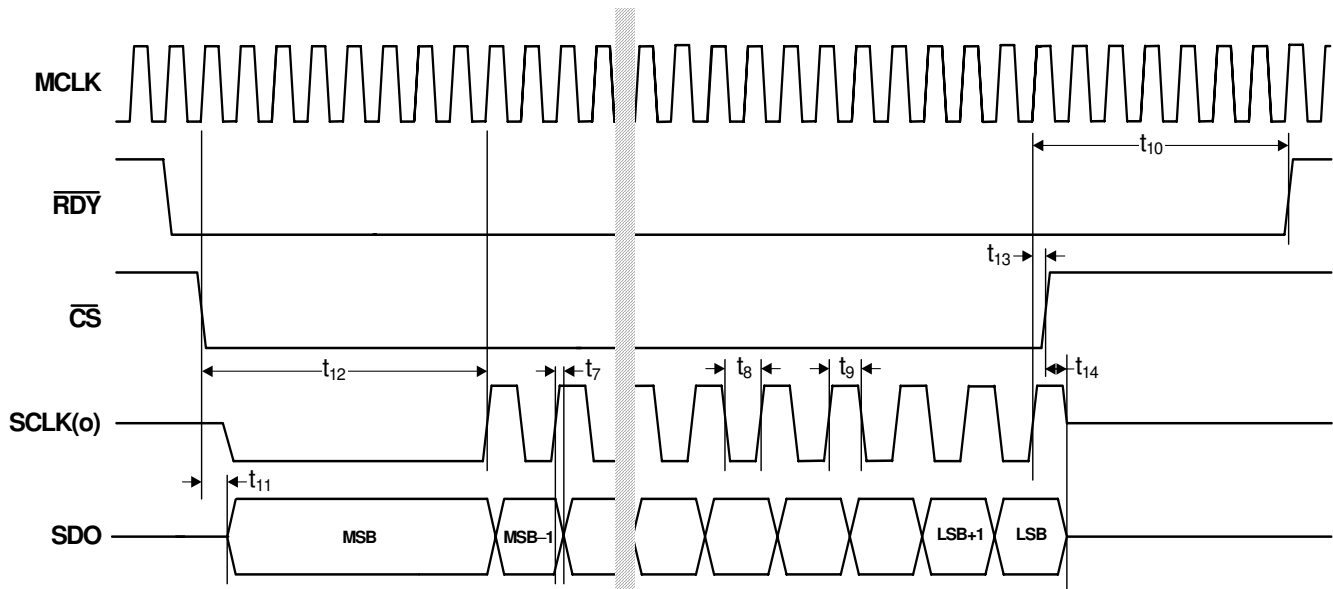
SWITCHING CHARACTERISTICS (CONTINUED)
 $T_A = -40$ to $+85$ °C; $V_{1+} = V_{2+} = +2.5$ V, $\pm 5\%$; $V_{1-} = V_{2-} = -2.5$ V, $\pm 5\%$;

 $V_L - V_{LR} = 3.3$ V, $\pm 5\%$, 2.5 V, $\pm 5\%$, or 1.8 V, $\pm 5\%$

 Input levels: Logic 0 = 0V = Low; Logic 1 = V_{D+} = High; $C_L = 15$ pF.

Parameter	Symbol	Min	Typ	Max	Unit
Serial Port Timing in SSC Mode (SMODE = VL)					
Data hold time after SCLK rising	t_7	-	10	-	ns
Serial Clock (Out) (Note 14, 15)	Pulse Width (low)	50	-	-	ns
	Pulse Width (high)	50	-	-	ns
\overline{RDY} rising after last SCLK rising	t_{10}	-	8	-	MCLKs
\overline{CS} falling to MSB stable	t_{11}	-	10	-	ns
First SCLK rising after \overline{CS} falling	t_{12}	-	8	-	MCLKs
\overline{CS} hold time (low) after SCLK rising	t_{13}	10	-	-	ns
SCLK, SDO tri-state after \overline{CS} rising	t_{14}	-	5	-	ns

14. SDO and SCLK will be high impedance when \overline{CS} is high. In some systems SCLK and SDO may require pull-down resistors.
15. $SCLK = MCLK/2$.

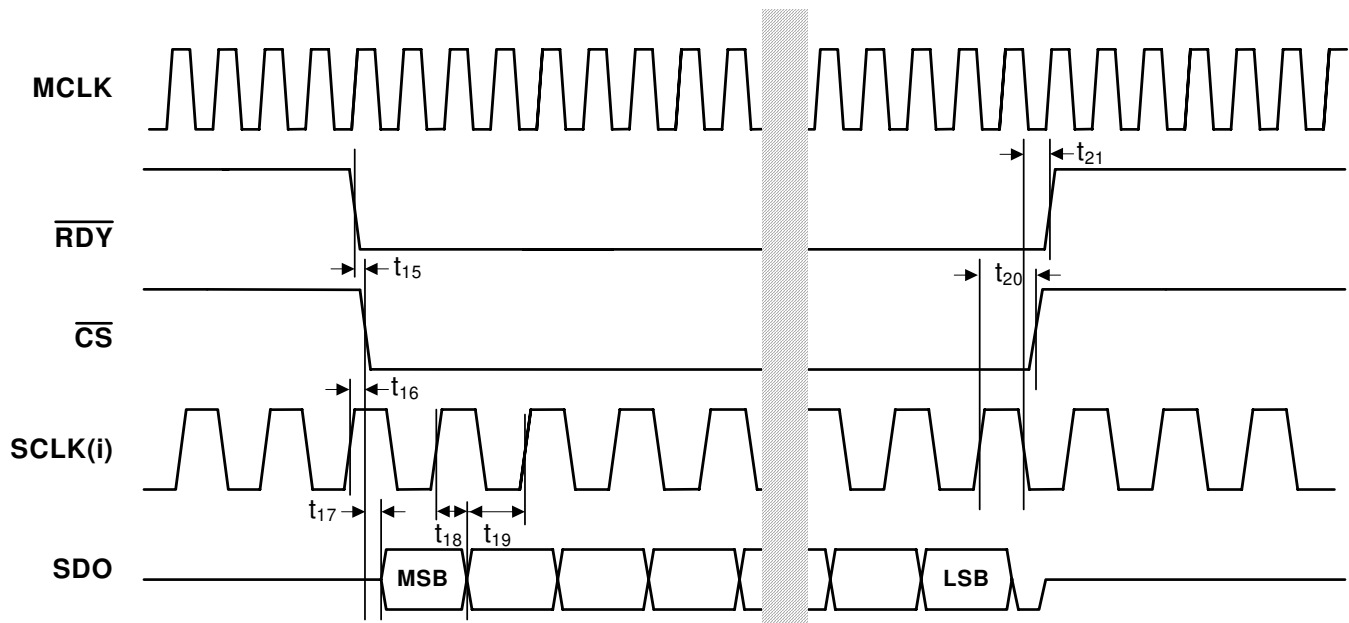

Figure 2. SSC Mode - Read Timing, \overline{CS} falling after \overline{RDY} falls (Not to Scale)

SWITCHING CHARACTERISTICS (CONTINUED)
 $T_A = -40$ to $+85$ °C; $V_{1+} = V_{2+} = +2.5$ V, $\pm 5\%$; $V_{1-} = V_{2-} = -2.5$ V, $\pm 5\%$;

 $V_L - V_{LR} = 3.3$ V, $\pm 5\%$, 2.5 V, $\pm 5\%$, or 1.8 V, $\pm 5\%$

 Input levels: Logic 0 = 0V = Low; Logic 1 = V_{D+} = High; CL = 15 pF.

Parameter	Symbol	Min	Typ	Max	Unit
Serial Port Timing in SEC Mode (SMODE = VLR)					
SCLK(in) Pulse Width (High)	-	30	-	-	ns
SCLK(in) Pulse Width (Low)	-	30	-	-	ns
\overline{CS} hold time (high) after \overline{RDY} falling	t_{15}	10	-	-	ns
\overline{CS} hold time (high) after SCLK rising	t_{16}	10	-	-	ns
\overline{CS} low to SDO out of Hi-Z (Note 16)	t_{17}	-	10	-	ns
Data hold time after SCLK rising	t_{18}	-	10	-	ns
Data setup time before SCLK rising	t_{19}	10	-	-	ns
\overline{CS} hold time (low) after SCLK rising	t_{20}	10	-	$\frac{1}{SCLK} - 10$	ns
\overline{RDY} rising after SCLK falling	t_{21}	-	10	-	ns

 16. SDO will be high impedance when \overline{CS} is high. In some systems SDO may require a pull-down resistor.

Figure 3. SEC Mode - Continuous SCLK Read Timing (Not to Scale)

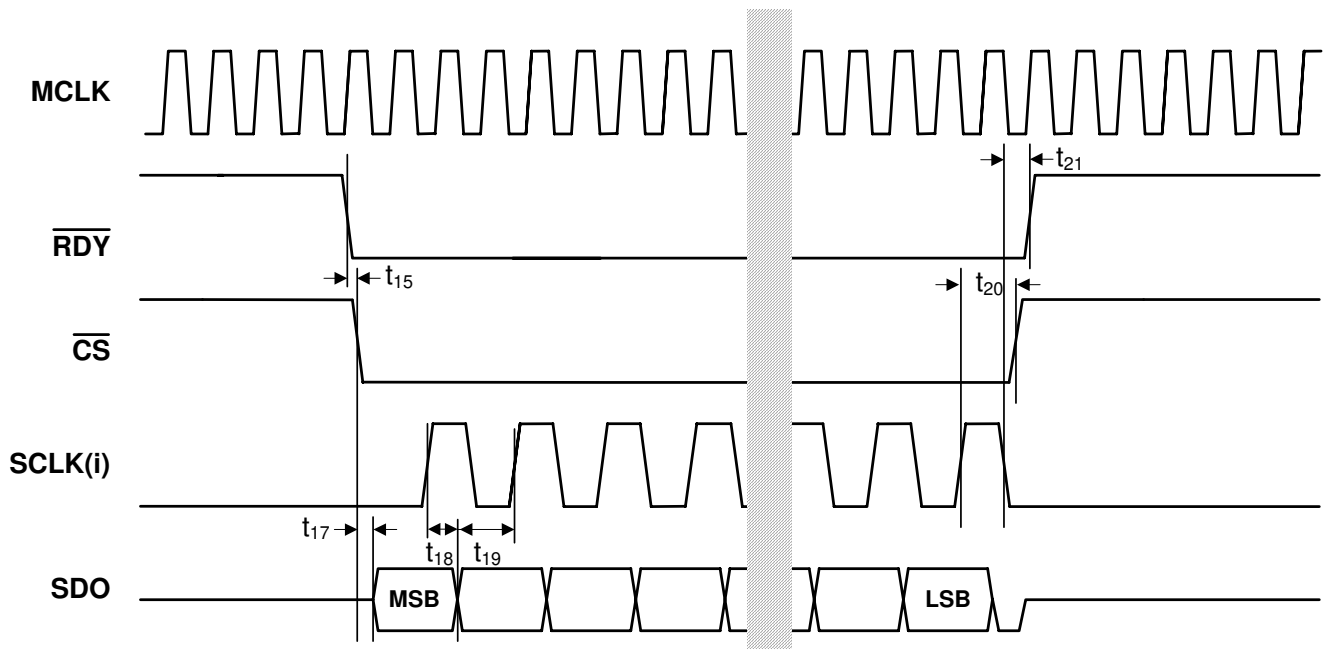


Figure 4. SEC Mode - Discontinuous SCLK Read Timing (Not to Scale)

DIGITAL CHARACTERISTICS

T_A = TMIN to TMAX; V_L = 3.3V, $\pm 5\%$ or V_L = 2.5V, $\pm 5\%$ or 1.8V, $\pm 5\%$; V_{LR} = 0V

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current	I_{in}	-	-	2	μA
Digital Input Pin Capacitance	C_{in}	-	3	-	pF
Digital Output Pin Capacitance	C_{out}	-	3	-	pF

GUARANTEED LOGIC LEVELS

$T_A = -40$ to $+85$ °C; $V_{1+} = V_{2+} = +2.5$ V, $\pm 5\%$; $V_{1-} = V_{2-} = -2.5$ V, $\pm 5\%$;

VL - VLR = 3.3 V, $\pm 5\%$, 2.5 V, $\pm 5\%$, or 1.8 V, $\pm 5\%$

Input levels: Logic 0 = 0V = Low; Logic 1 = V_{D+} = High; $C_L = 15$ pF.

Parameter	Sym	VL	Guaranteed Limits			Unit	Conditions
			Min	Typ	Max		
Logic Inputs							
Minimum High-level Input Voltage:	V_{IH}	3.3	1.9			V	
		2.5	1.6				
		1.8	1.2				
Maximum Low-level Input Voltage:	V_{IL}	3.3			1.1	V	
		2.5			0.95		
		1.8			0.6		
Logic Outputs							
Minimum High-level Output Voltage:	V_{OH}	3.3	2.9			V	$I_{OH} = -2$ mA
		2.5	2.1				
		1.8	1.65				
Maximum Low-level Output Voltage:	V_{OL}	3.3			0.36	V	$I_{OH} = -2$ mA
		2.5			0.36		
		1.8			0.44		

RECOMMENDED OPERATING CONDITIONS

(VLR = 0V, see Note 17)

Parameter	Symbol	Min	Typ	Max	Unit	
Single Analog Supply						
DC Power Supplies:	(Note 17)					
V1+	V1+	4.75	5.0	5.25	V	
V2+	V2-	4.75	5.0	5.25	V	
V1-	V1+	-	0	-	V	
V2-	V2-	-	0	-	V	
Dual Analog Supplies						
DC Power Supplies:	(Note 17)					
V1+	V1+	+2.375	+2.5	+2.625	V	
V2+	V2-	+2.375	+2.5	+2.625	V	
V1-	V1+	-2.375	-2.5	-2.625	V	
V2-	V2-	-2.375	-2.5	-2.625	V	
Analog Reference Voltage	(Note 18) [VREF+] – [VREF-]	VREF	2.4	4.096	4.2	V

17. The logic supply can be any value VL – VLR = +1.71 to +3.465 volts as long as VLR ≥ V2- and VL ≤ 3.465 V.

18. The differential voltage reference magnitude is constrained by the V1+ or V1- supply magnitude.

ABSOLUTE MAXIMUM RATINGS

(VLR = 0V)

Parameter	Symbol	Min	Typ	Max	Unit	
DC Power Supplies:						
[V1+] – [V1-] (Note 19)	-	0	-	5.5	V	
VL + [V1-] (Note 20)	-	0	-	6.1	V	
Input Current, Any Pin Except Supplies	(Note 21)	I _{IN}	-	-	±10	mA
Analog Input Voltage	(AIN and VREF pins)	V _{INA}	(V1-) – 0.3	-	(V1+) + 0.3	V
Digital Input Voltage		V _{IND}	VLR – 0.3	-	VL + 0.3	V
Storage Temperature		T _{stg}	-65	-	150	°C

Notes: 19. V1+ = V2+; V1- = V2-

20. V1- = V2-

21. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING:

Recommended Operating Conditions indicate limits to which the device is functionally operational. Absolute Maximum Ratings indicate limits beyond which permanent damage to the device may occur. The Absolute Maximum Ratings are stress ratings only and the device should not be operated at these limits. Operation at conditions beyond the Recommended Operating Conditions may affect device reliability, and functional operation beyond Recommended Operating Conditions is not implied. Performance specifications are intended for the conditions specified for each table in the Characteristics and Specifications section.

2. OVERVIEW

The CS5571 is a 16-bit analog-to-digital converter capable of 100 kSps conversion rate. The analog input accepts a single-ended input with a magnitude of $\pm V_{REF} / 2$ volts. The device is capable of switching multiple input channels at a high rate with no loss in throughput. The ADC uses a low-latency digital filter architecture. The filter is designed for fast settling and settles to full accuracy in one conversion.

The converter is a serial output device. The serial port can be configured to function as either a master or a slave.

The converter can operate from an analog supply of 5V or from $\pm 2.5V$. The digital interface supports standard logic operating from 1.8, 2.5, or 3.3 V.

The CS5571 may convert at rates up to 100 kSps when operating from a 16 MHz input clock.

3. THEORY OF OPERATION

The CS5571 converter provides high-performance measurement of DC or AC signals. The converter can be used to perform single conversions or continuous conversions upon command. Each conversion is independent of previous conversions and settles to full specified accuracy, even with a full-scale input voltage step. This is due to the converter architecture which uses a combination of a high-speed delta-sigma modulator and a low-latency filter architecture.

Once power is established to the converter, a reset must be performed. A reset initializes the internal converter logic.

If \overline{CONV} is held low, the converter will convert continuously with \overline{RDY} falling every 160 MCLKs. This is equivalent to 100 kSps if $MCLK = 16.0$ MHz. If \overline{CONV} is tied to \overline{RDY} , a conversion will occur every 162 MCLKs. If \overline{CONV} is operated asynchronously to MCLK, it may take up to 164 MCLKs from \overline{CONV} falling to \overline{RDY} falling.

Multiple converters can operate synchronously if they are driven by the same MCLK source and \overline{CONV} to each converter falls on the same MCLK falling edge. Alternately, \overline{CONV} can be held low and all devices can be synchronized if they are reset with \overline{RST} rising on the same falling edge of MCLK.

The output coding of the conversion word is a function of the BP/\overline{UP} pin.

3.1 Converter Operation

The converter should be reset after the power supplies and voltage reference are stable.

The CS5571 converts at 100 kSps when synchronously operated ($\overline{CONV} = \overline{VLR}$) from a 16.0 MHz master clock. Conversion is initiated by taking \overline{CONV} low. A conversion lasts 160 master clock cycles, but if \overline{CONV} is asynchronous to MCLK there may be an uncertainty of 0-4 MCLK cycles after \overline{CONV} falls to when a conversion actually begins. This may extend the throughput to 164 MCLKs per conversion.

When the conversion is completed, the output word is placed into the serial port and \overline{RDY} goes low. To convert continuously, \overline{CONV} should be held low. In continuous conversion mode with \overline{CONV} held low, a conversion is performed in 160 MCLK cycles. Alternately \overline{RDY} can be tied to \overline{CONV} and a conversion will occur every 162 MCLK cycles.

To perform only one conversion, \overline{CONV} should return high at least 20 master clock cycles before \overline{RDY} falls.

Once a conversion is completed and $\overline{\text{RDY}}$ falls, $\overline{\text{RDY}}$ will return high when all the bits of the data word are emptied from the serial port or if the conversion data is not read and $\overline{\text{CS}}$ is held low, $\overline{\text{RDY}}$ will go high two MCLK cycles before the end of conversion. $\overline{\text{RDY}}$ will fall at the end of the next conversion when new data is put into the port register.

See [Serial Port](#) on page 26 for information about reading conversion data.

Conversion performance can be affected by several factors. These include the choice of clock source for the chip, the timing of $\overline{\text{CONV}}$, the setting of the DITHER function, and the choice of the serial port mode.

The converter can be operated from an internal oscillator. This clock source has greater jitter than an external crystal-based clock. Jitter may not be an issue when measuring DC signals, or very-low-frequency AC signals, but can become an issue for higher frequency AC signals. For maximum performance when digitizing AC signals, a low-jitter MCLK should be used.

To achieve the highest resolution when measuring a DC signal with a single conversion the DITHER function should be off. If averaging is to be performed with multiple conversions of a DC signal, DITHER should be on. To maximize performance, the $\overline{\text{CONV}}$ pin should be held low in the continuous conversion state to perform multiple conversions, or $\overline{\text{CONV}}$ should occur synchronous to MCLK, falling when MCLK falls.

If the converter is operated at maximum throughput, the SSC serial port mode is less likely to cause interference to measurements as the SCLK output is synchronized to the MCLK. Alternately, any interference due to serial port clocking can also be minimized if data is read in the SEC serial port mode when a conversion is not in progress.

3.2 Clock

The CS5571 can be operated from its internal oscillator or from an external master clock. The state of MCLK determines which clock source will be used. If MCLK is tied low, the internal oscillator will start and be used as the clock source for the converter. If an external CMOS-compatible clock is input into MCLK, the converter will power down the internal oscillator and use the external clock. If the MCLK pin is held high, the internal oscillator will be held in the stopped state. The MCLK input can be held high to delete clock cycles to aid in synchronizing multiple converters in different phase relationships.

The internal oscillator can be used if the signals to be measured are essentially DC. The internal oscillator exhibits jitter at about 500 picoseconds rms. If the CS5571 is used to digitize AC signals, an external low-jitter clock source should be used.

If the internal oscillator is used as the clock for the CS5571, the maximum conversion rate will be dictated by the oscillator frequency.

If driven from an external MCLK source, the fast rise and fall times of the MCLK signal can result in clock coupling from the internal bond wire of the IC to the analog input. Adding a 50 ohm resistor on the external MCLK source significantly reduces this effect.

3.3 Voltage Reference

The voltage reference for the CS5571 can range from 2.4 volt to 4.2 volts. A 4.096 volt reference is required to achieve the specified signal-to-noise performance. [Figure 6](#) and [Figure 7](#) illustrate the connection of the voltage reference with either a single +5 V analog supply or with ± 2.5 V.

For optimum performance, the voltage reference device should be one that provides a capacitor connection to provide a means of noise filtering, or the output should include some type of bandwidth-limiting filter.

Some 4.096 volt reference devices need only 5 volts total supply for operation and can be connected as shown in [Figure 6](#) or [Figure 7](#). The reference should have a local bypass capacitor and an appropriate output capacitor.

Some older 4.096 voltage reference designs require more headroom and must operate from an input voltage of 5.5 to 6.5 volts. If this type of voltage reference is used ensure that when power is applied to the system, the voltage reference rise time is slower than the rise time of the V1+ and V1- power supply voltage to the converter. An example circuit to slow the output startup time of the reference is illustrated in [Figure 5](#).

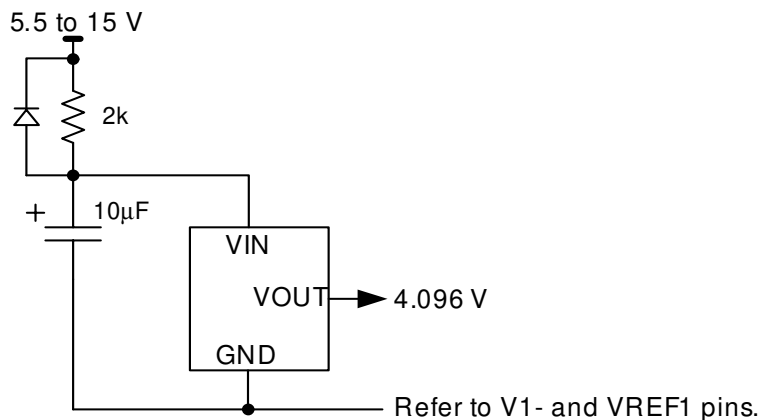


Figure 5. Voltage Reference Circuit

3.4 Analog Input

The analog input of the converter is single-ended with a full-scale input of ± 2.048 volts, relative to the ACOM pin.. This is illustrated in [Figure 6](#) and [Figure 7](#). These diagrams also illustrate a differential buffer amplifier configuration for driving the CS5571.

The capacitors at the outputs of the amplifiers provide a charge reservoir for the dynamic current from the A/D inputs while the resistors isolate the dynamic current from the amplifier. The amplifiers can be powered from higher supplies than those used by the A/D but precautions should be taken to ensure that the op-amp output voltage remains within the power supply limits of the A/D, especially under start-up conditions.

3.5 Output Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/ \overline{UP} low), the first code transition occurs 0.5 LSB above zero, and the final code transition occurs 1.5 LSBs below VREF. In the bipolar configuration (BP/ \overline{UP} high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSBs below +VREF. See [Table 1](#) for the output coding of the converter.

Table 1. Output Coding, Two's Complement

Bipolar Input Voltage	Two's Complement
$>(VREF-1.5 \text{ LSB})$	7F FF
$VREF-1.5 \text{ LSB}$	7F FF 7F FE
-0.5 LSB	00 00 FF FF
$-VREF+0.5 \text{ LSB}$	80 01 80 00
$<(-VREF+0.5 \text{ LSB})$	80 00

NOTE: $VREF = [(VREF+) - (VREF-)] / 2$

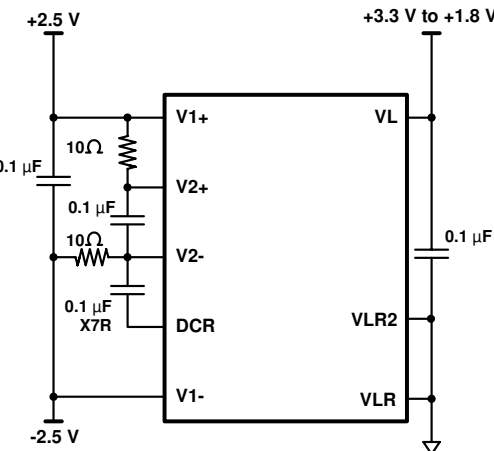
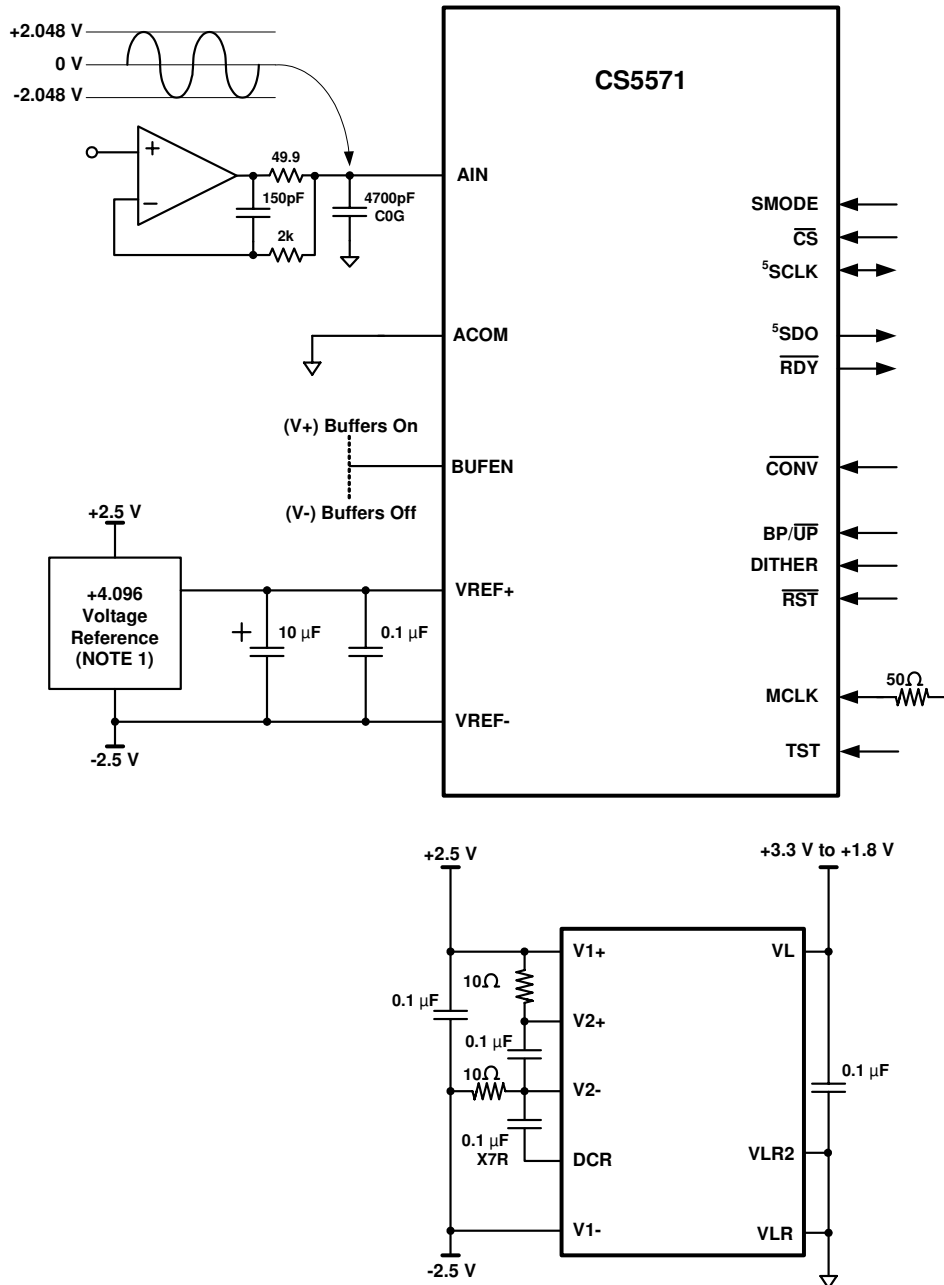
Table 2. Output Coding, Offset Binary

Unipolar Input Voltage	Offset Binary
$>(VREF-1.5 \text{ LSB})$	FF FF
$VREF-1.5 \text{ LSB}$	FF FF FF FE
$(VREF/2)-0.5 \text{ LSB}$	80 00 7F FF
$+0.5 \text{ LSB}$	00 01 00 00
$<(+0.5 \text{ LSB})$	00 00

NOTE: $VREF = [(VREF+) - (VREF-)] / 2$

3.6 Typical Connection Diagrams

The following figure depicts the CS5571 powered from bipolar analog supplies, +2.5 V and - 2.5 V.

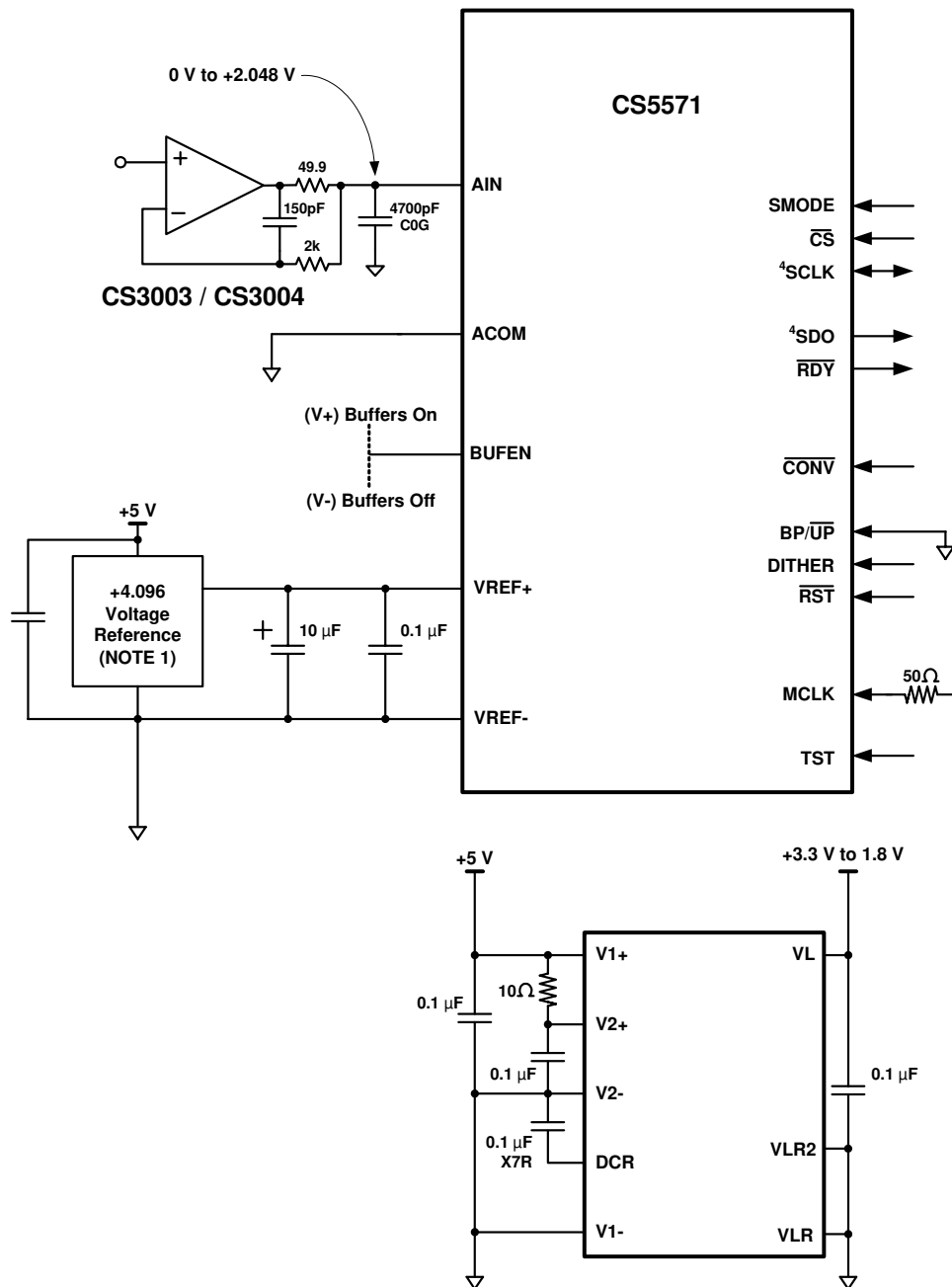


NOTES

1. See Section 3.3 Voltage Reference for information on required voltage reference performance criteria.
2. Locate capacitors so as to minimize loop length.
3. The ±2.5 V supplies should also be bypassed to ground at the converter.
4. VLR and the power supply ground for the ±2.5 V should be connected to the same ground plane under the chip.
5. SCLK and SDO may require pull-down resistors in some applications.

Figure 6. CS5571 Configured Using ±2.5V Analog Supplies

The following figure depicts the CS5571 part powered from a single 5V analog supply and configured for unipolar measurement.

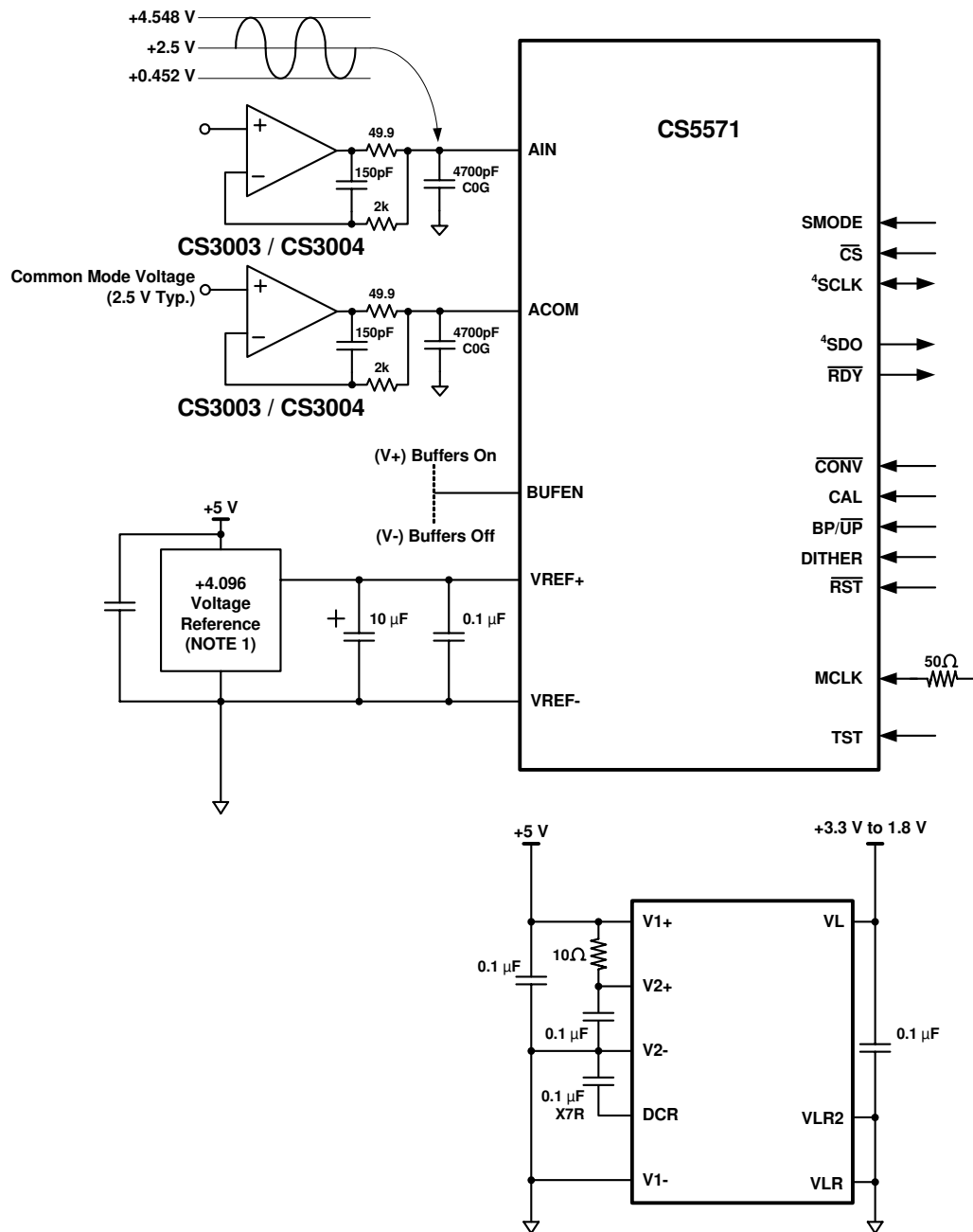


NOTES

1. See Section 3.3 Voltage Reference for information on required voltage reference performance criteria.
2. Locate capacitors so as to minimize loop length.
3. V1-, V2-, and VLR should be connected to the same ground plane under the chip.
4. SCLK and SDO may require pull-down resistors in some applications.

Figure 7. CS5571 Configured for Unipolar Measurement Using a Single 5V Analog Supply

The following figure depicts the CS5571 part powered from a single 5V analog supply and configured for bipolar measurement, referenced to a common mode voltage of 2.5 V.


NOTES

1. See Section 3.3 Voltage Reference for information on required voltage reference performance criteria.
2. Locate capacitors so as to minimize loop length.
3. V1-, V2-, and VLR should be connected to the same ground plane under the chip.
4. SCLK and SDO may require pull-down resistors in some applications.

Figure 8. CS5571 Configured for Bipolar Measurement Using a Single 5V Analog Supply

3.7 AIN & VREF Sampling Structures

The CS5571 uses on-chip buffers on the AIN and VREF+ inputs. Buffers provide much higher input impedance and therefore reduce the amount of drive current required from an external source. This helps minimize errors.

The Buffer Enable (BUFEN) pin determines if the on-chip buffers are used or not. If the BUFEN pin is connected to the V1+ supply, the buffers will be enabled. If the BUFEN pin is connected to the V1- pin, the buffers are off. The converter will consume about 30 mW less power when the buffers are off, but the input impedances of AIN, ACOM and VREF+ will be significantly less than with the buffers enabled.

3.8 Converter Performance

The CS5571 achieves excellent differential nonlinearity (DNL) as shown in figures 9 and 10. Figure 9 illustrates the code widths on a typical scale of ± 1 LSB. Figure 10 illustrates a zoom view of figure 9 on a scale of ± 0.1 LSB. Figure 10 also includes a DNL error histogram that indicates that the errors are equally distributed about the perfect code size; and most codes are accurate within ± 0.01 LSB.

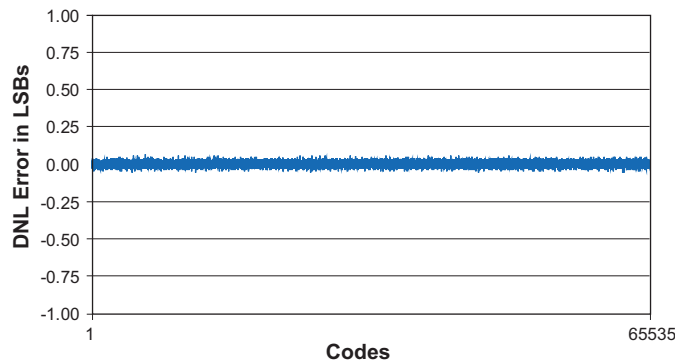


Figure 9. CS5571 DNL Plot

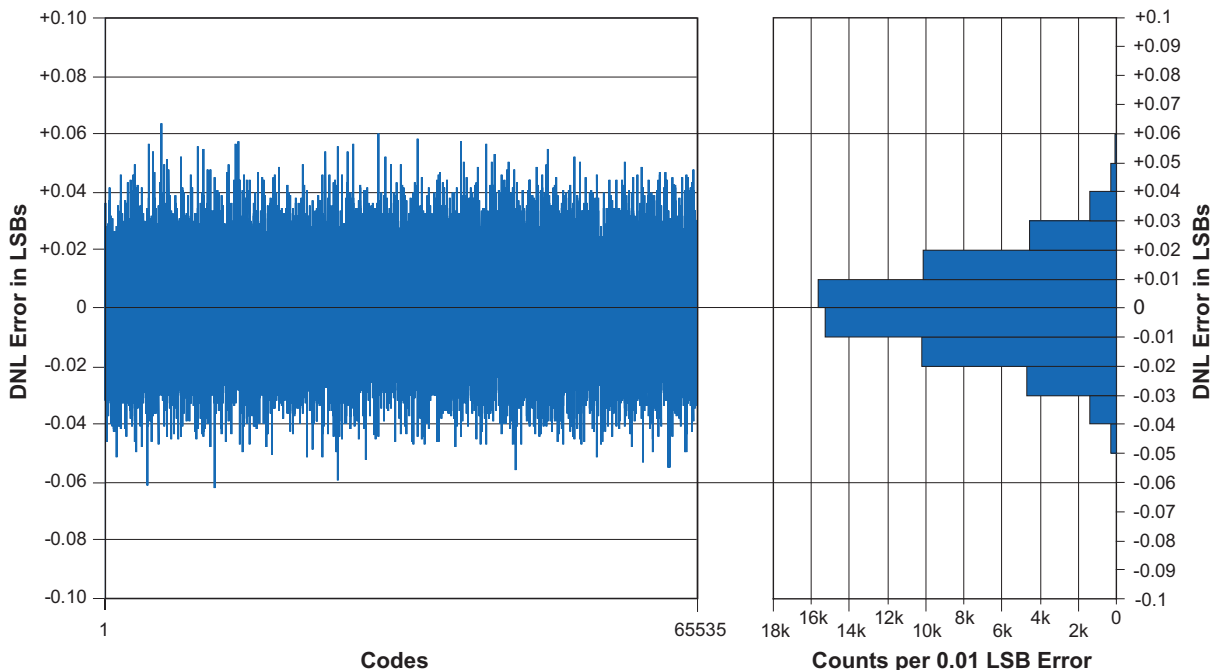


Figure 10. CS5581 DNL Error Plot with DNL Histogram

Figures 11, 12, and 13 indicate the spectral performance of the CS5571 with a 0 dB, -6 dB and -12 dB 5.55 kHz input signal. In each case, the captured data was windowed with a seven-term window function that exhibits 4.3 dB of attenuation before being processed by the FFT.

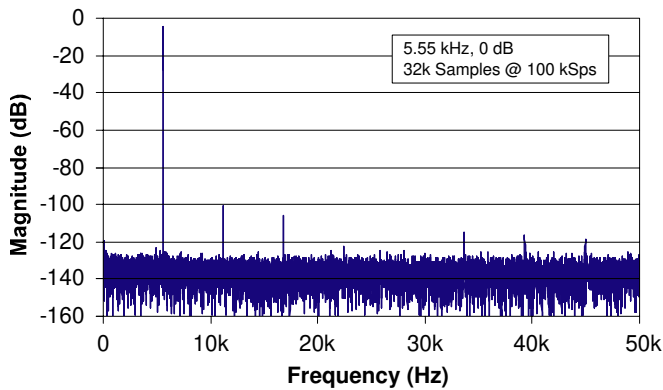


Figure 11. Spectral Performance, 0 dB

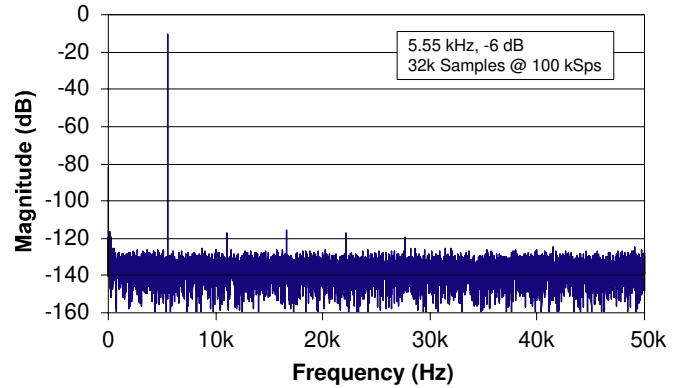


Figure 12. Spectral Performance, -6 dB

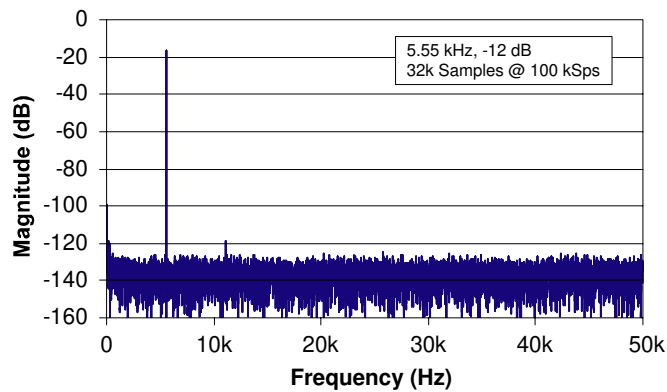
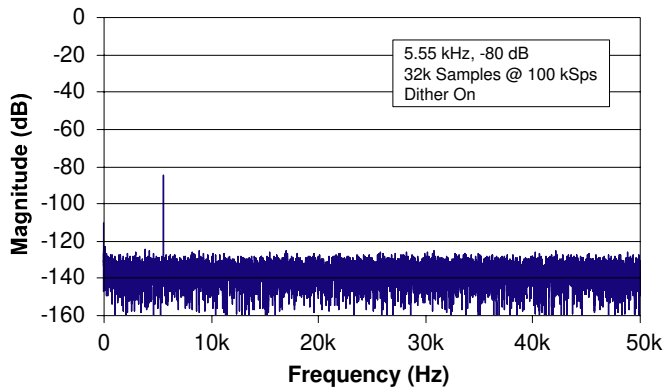
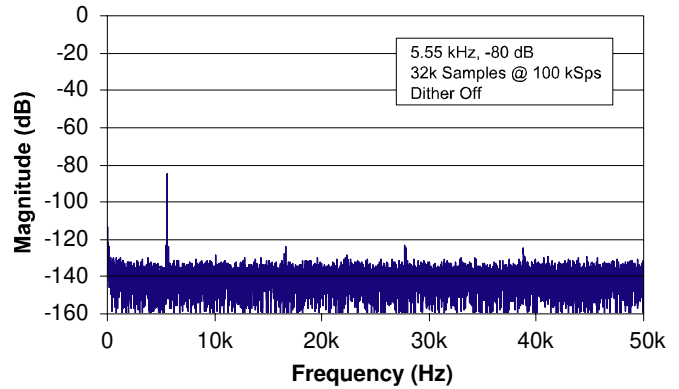


Figure 13. Spectral Performance, -12 dB

Figures 14 and 15 illustrate the small signal performance of the CS5571 with a 5.55 kHz signal at -80 dB down. Figure 14 is with DITHER on and Figure 15 is with DITHER off. At -80 dB the signal is 1/10,000 of full scale, having a peak-to-peak magnitude of only a few codes. For small signals, DNL errors and quantization errors can introduce distortion because the error in the code size, or the quantization error without adequate dither, are a much greater percentage of the signal than with a full-scale input. Figure 15, with DITHER off, illustrates that distortion components can be introduced when there is not adequate dither to randomize the quantization error.

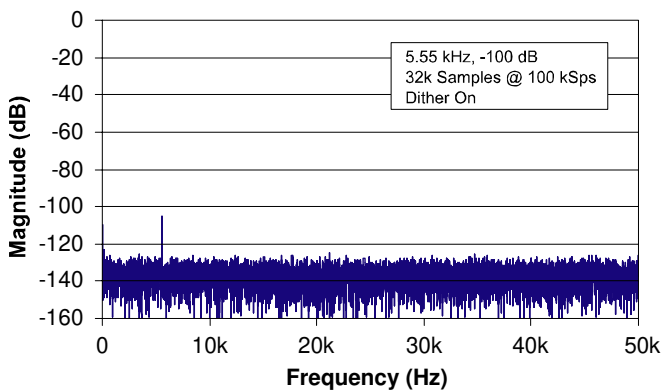


**Figure 14. Spectral Performance, -80 dB
Dither On**

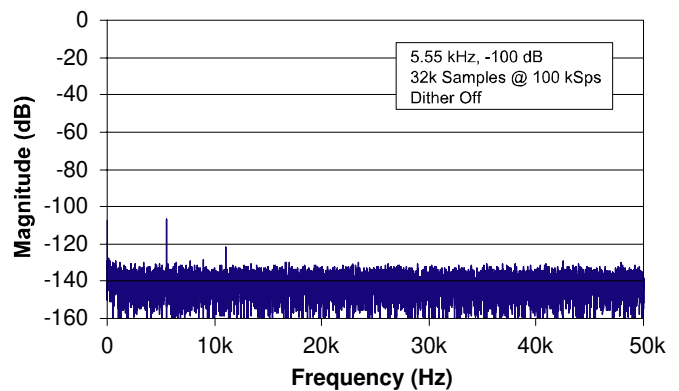


**Figure 15. Spectral Performance, -80 dB
Dither Off**

Figures 16 and 17 illustrate DITHER on and DITHER off with a 5.55 kHz input at -100 dB. At -100 dB the signal is only about 41 microvolts peak to peak. This is less than the one code width which is about 62.5 microvolts.

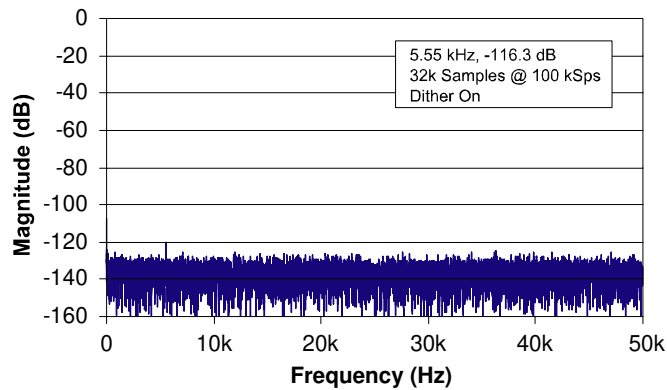


**Figure 16. Spectral Performance, -100 dB
Dither On**



**Figure 17. Spectral Performance, -100 dB
Dither Off**

Figure 18 illustrates a test signal of 5.55 kHz, 116.3 dB down, which is only 6.3 microvolts peak to peak, or about 1/10 of a code width. The converter can reliably digitize this signal because of its excellent DNL and proper dither.



**Figure 18. Spectral Performance, -116.3 dB
Dither On**

Figure 19 is a spectral plot of the converter with its input grounded. The spectral information is on a logarithmic frequency axis as this illustrates the very low frequency behavior of the converter. Figure 19 was produced from averaging the results of 16 FFT outputs using 2 million samples each. This plot also illustrates that the converter noise floor is free of spurious components that may be present in other converters due to on-chip digital interference.

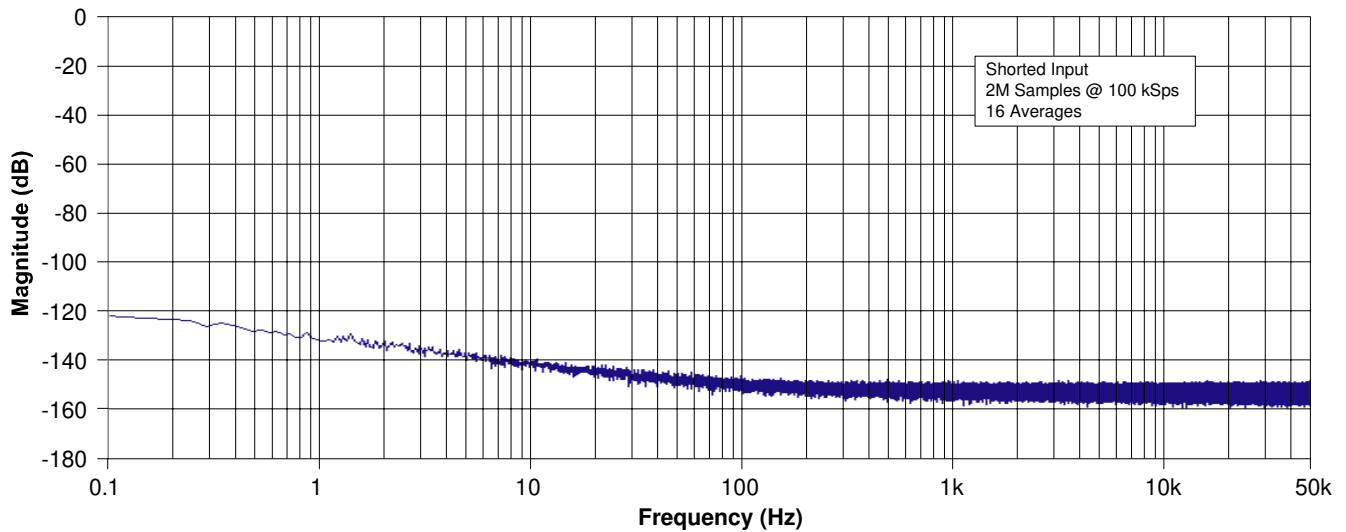


Figure 19. Spectral Plot of Noise with Shorted Input

Figure 20 illustrates a noise histogram of 4096 samples with the input signal adjusted to almost the exact center of a code with DITHER on. Figure 21 illustrates a noise histogram of 4096 samples with the input signal at the center of a code with DITHER off.

Notice that with a signal at the center of a code that the converter outputs the same code over 96% of the time. Figures 22 and 23 illustrate the noise histogram, DITHER on and then DITHER off with the input signal at a code boundary. Notice that in the DITHER off case the converter only exhibits two codes of noise.

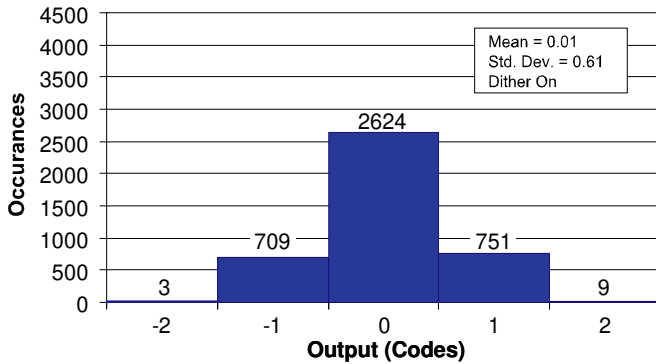


Figure 20. Noise Histogram, 4096 Samples Dither On, Code Center

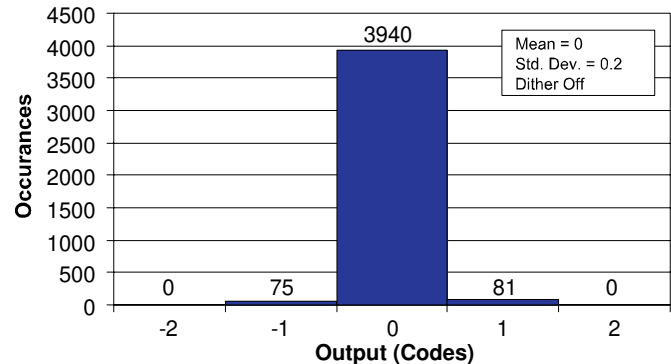


Figure 21. Noise Histogram, 4096 Samples Dither Off, Code Center

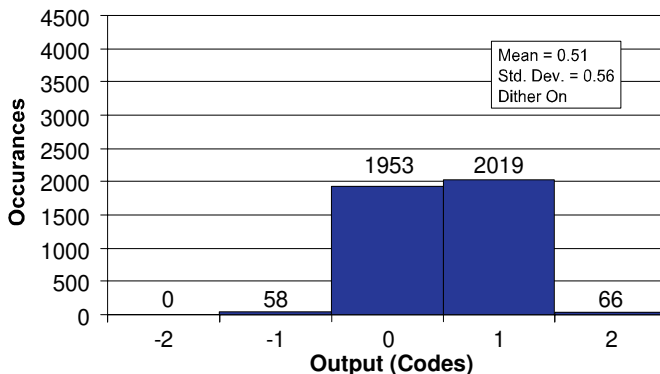


Figure 22. Noise Histogram, 4096 Samples Dither On, Input at Code Boundary

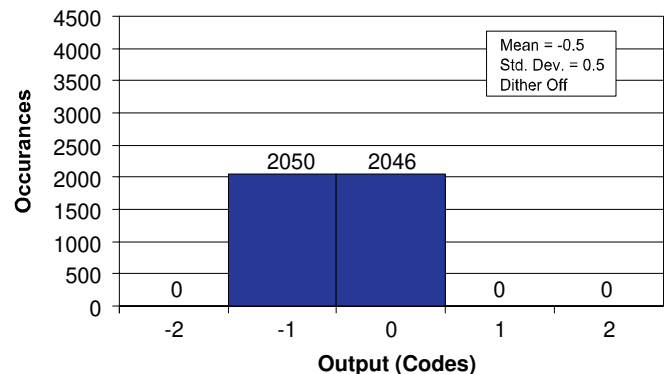


Figure 23. Noise Histogram, 4096 Samples Dither Off, Input at Code Boundary

3.9 DITHER

From the performance plots, one should conclude that the best AC performance for small signals occurs with DITHER on. For capturing multiple samples and performing averaging, DITHER should also be on because the dither will randomize the quantization noise of the converter and provide improved accuracy. However, if only one conversion is to be taken on a DC input, DITHER should be set to off. With DITHER off, the converter exhibits only two codes of noise if the signal is at any point other than the exact center of a code. This means that with DITHER off the converter will nominally yield over 32,000 noise-free counts.

3.10 Digital Filter Characteristics

The digital filter is designed for fast settling, therefore it exhibits very little in-band attenuation. The filter attenuation is 1.040 dB at 50 kHz when sampling at 100 kSps.

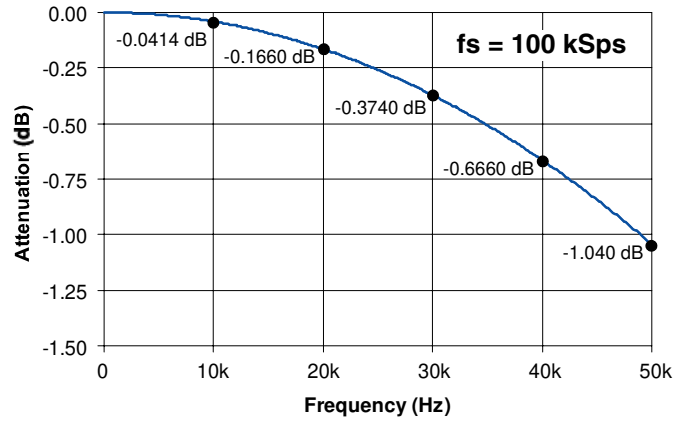


Figure 24. CS5571 Digital Filter Response (DC to fs/2)

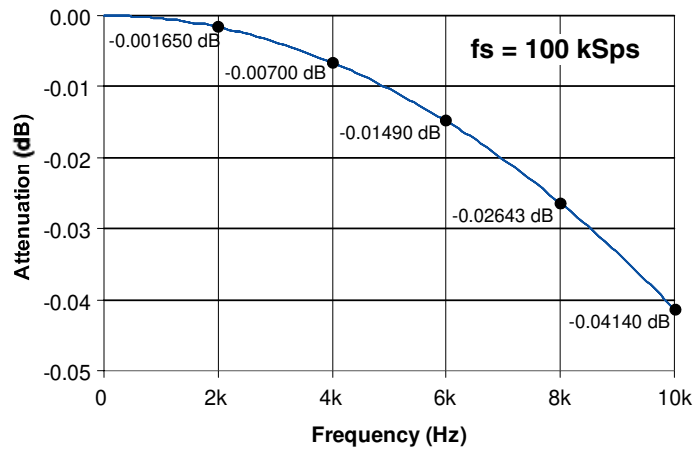


Figure 25. CS5571 Digital Filter Response (DC to 10 kHz)

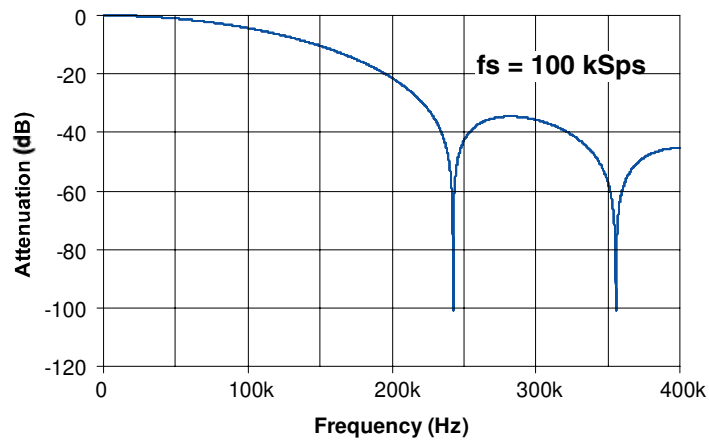


Figure 26. CS5571 Digital Filter Response (DC to 4fs)