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CEC1702

Cryptographic Embedded Controller

- 3.3V and 1.8V Operation
- ACPI Compliant
- VTR (standby) and VBAT Power Planes
  - Low Standby Current in Sleep Mode
- ARM® Cortex®-M4 Processor Core
  - 32-Bit ARM v7-M Instruction Set Architecture
  - Hardware Floating Point Unit (FPU)
  - Single 4GByte Addressing Space (Von Neumann Model)
  - Little-Endian Byte Ordering
  - Bit-Banding Feature Included
  - NVIC Nested Vectored Interrupt Controller
    - Up to 240 Individually-Vectored Interrupt Sources Supported
    - 8 Levels of Priority, Individually Assignable By Vector
    - Chip-Level Interrupt Aggregator supported, to expand number of interrupt sources or reduce number of vectors
  - System Tick Timer
  - Complete ARM-Standard Debug Support
    - JTAG-Based DAP Port, Comprised of SWJ-DP and AHB-AP Debugger Access Functions
    - Full DWT Hardware Functionality: 4 Data Watchpoints and Execution Monitoring
    - Full FPB Hardware Breakpoint Functionality: 6 Execution Breakpoints and 2 Literal (Data) Breakpoints
  - Comprehensive ARM-Standard Trace Support
    - Full DWT Hardware Trace Functionality for Watchpoint and Performance Monitoring
    - Full ITM Hardware Trace Functionality for Instrumented Firmware Support and Profiling
    - Full TPIU Functionality for Trace Output Communication
  - MPU Feature
  - 1µS Delay Register
- Internal Memory
  - 64k Boot ROM
  - Two blocks of SRAM, totaling 480KB
    - Each block can be used for either program or data
  - 128 Bytes Battery Powered SRAM
- Battery Backed Resources
  - Power-Fail Status Register
  - 32 KHz Clock Generator
  - Week Alarm Timer Interface
  - Real Time Clock
  - VBAT-Powered Control Interface
    - Two Wake-up Input Signals
    - Optional Latching of Wake-up Inputs
  - VBAT-Backed 128 Byte Memory
- Four I^2C Host Controllers
  - Allows Master or Dual Slave Operation
  - Fully Operational on Standby Power
  - DMA-driven I^2C Network Layer Hardware
  - I^2C Datalink Compatibility Mode
  - Multi-Master Capable
  - Supports Clock Stretching
  - Programmable Bus Speed up to 1MHz
  - Hardware Bus Access “Fairness” Interface
  - SMBus Time-outs Interface
  - All Ports Assignable to Any Controller
  - All ports 1.8V-capable
- General Purpose Serial Peripheral Interface Controller
  - One 4-pin Full Duplex Serial Communication Interface
  - Flexible Clock Rates
  - SPI Burst Capable
- One Quad Serial Peripheral Interface (SPI) Controller
  - Master Only SPI Controller
  - Mappable to two ports (only 1 port active at a time)
  - Dual and Quad I/O Support
  - Flexible Clock Rates
  - SPI Burst Capable
  - SPI Controller Operates with Internal DMA Controller with CRC Generation
- 13 x 8 Interrupt Capable Multiplexed Keyboard Scan Matrix
  - Optional Push-Pull Drive for Fast Signal Switching
- Two Breathing/Blinking LED Interfaces
  - Supports three modes of operation:
    - Blinking Mode with Programmable Blink Rates
    - Breathing LED Output
    - 8-bit PWM
  - Breathing LED Supports Piecewise-linear Brightness Curves, Symmetric or Asymmetric
  - Supports Low Power Operation in Blinking and Breathing Modes
    - Operates on Standby Power
    - Operates in Chip's System Deepest Sleep State on 32kHz standby clock
    - Operational in EC Sleep State
  - Pin buffers capable of sinking up to 12 mA
- Two Resistor/Capacitor Identification Detection (RC_ID) ports
  - Single Pin Interface to External Inexpensive RC Circuit
  - Replacement for Multiple GPIO’s
  - Provides 8 Quantized States on One Pin
- General Purpose I/O Pins
  - Up to 65 GPIOs

  - Glitch protection on most GPIO pins
  - 1 Battery-powered General Purpose Outputs
  - All GPIOs can be powered by 1.8V
  - Programmable Drive Strength and Slew Rate on all GPIOs
- Programmable 16-bit Counter/Timer Interface
  - Four 16-bit Auto-reloading Counter/Timer Instances
  - Four Operating Modes per Instance: Timer, One-shot, Event and Measurement
    - 3 External Inputs
    - 2 External Outputs
- Hibernation Timer Interface
  - Two 32.768 KHz Driven 16-bit Timers
    - Programmable Wake-up from 0.5ms to 128 Minutes
  - One 32.768 KHz Driven 32-bit RTOS Timer
    - Programmable Wake-up from 30µS to 35 Hours
    - Auto Reload Option
- System Watch Dog Timer (WDT)
- Input Capture Timer
  - 32-bit Free-running timer
  - Four 32-bit Capture Registers
  - One Compare Timer with Optional Toggling Output
  - Capture Interrupts with Programmable Edge Detection
  - Compare Timer and Counter Overflow Interrupts
- Week Timer
  - Power-up Event Output
  - Week Alarm Interrupt with 1 Second to 8.5 Year Time-out
  - Sub-Week Alarm Interrupt with 0.50 Seconds - 72.67 hours time-out
  - 1 Second and Sub-second Interrupts
- Real Time Clock (RTC)
  - VBAT Powered
  - 32KHz Crystal Oscillator
  - Time-of-Day and Calendar Registers
  - Programmable Alarms
  - Supports Leap Year and Daylight Savings Time
- Pulse-Width Modulator Support
  - Seven Programmable PWM Outputs
    - Multiple Clock Rates
    - 16-Bit 'On' and 16-Bit 'Off' Counters
  - Optional Inverted Output
- FAN Support
  - Two Fan Tachometer Inputs
  - Two RPM-Based Fan Speed Controllers
    - Each includes one Tach input and one PWM output
    - 3% accurate from 500 RPM to 16k RPM
    - Automatic Tachometer feedback
    - Aging Fan or Invalid Drive Detection
    - Spin Up Routine
    - Ramp Rate Control
    - RPM-based Fan Speed Control Algorithm
- ADC Interface
  - 10-bit Conversion in 1µs
  - 5 Channels
  - Integral Non-Linearity of ±1.5 LSB; Differential Non-Linearity of ±1.0 LSB
- Two Standard 16C550 UARTs
  - Both UARTs with 4-pin Interface
  - Programmable Input/output Pin Polarity Inversion
  - Programmable Main Power or Standby Power Functionality
- Trace FIFO Debug Port (TFDP)
- Integrated Standby Power Reset Generator
  - Reset Input Pin
- Clock Generator
  - 32.768KHz Clock Source
    - Low power 32KHz crystal oscillator
    - Optional use of a crystal-free silicon oscillator with ±2% Accuracy
    - Optional use of 32.768 KHz input Clock
    - Operational on Suspend Power
  - Programmable Clock Power Management Control and Distribution
  - 48 MHz PLL
- Multi-purpose AES Cryptographic Engine
  - Hardware support for ECB, CTR, CBC and OFB AES modes
  - Support for 128-bit, 192-bit and 256-bit key length
  - DMA interface to SRAM, shared with Hash engine
- Cryptographic Hash Engine
  - Support for SHA-1, SHA-256, SHA-512
  - DMA interface to SRAM, shared with AES engine
- Public Key Cryptographic Engine
  - Hardware support for RSA and Elliptic Curve public key algorithms
  - RSA keys length from 1024 to 4096 bits
  - ECC Prime Field and Binary Field keys up to 640 bits
  - Microcoded support for standard public key algorithms
- Cryptographic Features
  - True Random Number Generator
    - 1K bit FIFO
  - Monotonic Counter
- Package
  - 84 Pin WFBGA RoHS Compliant package

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Table of Contents

1.0 GENERAL DESCRIPTION

The CEC1702 is a family of embedded controller designs with strong cryptographic support, customized for Internet of Things (IOT) platforms. The family is a highly-configurable, mixed signal, advanced I/O controller architecture. The device incorporates a 32-bit ARM Cortex M4F Microcontroller core with a closely-coupled SRAM for code and data. A secure boot-loader is used to download the custom firmware image from the system's shared SPI Flash device, thereby allowing system designers to customize the device's behavior.

The CEC1702 is directly powered by a minimum of two separate suspend supply planes (VBAT and VTR). There are three voltage supply regions for all GPIO pins. Two regions may be either 3.3V or 1.8V.

The CEC1702 family of devices offer a software development system interface that includes a Trace FIFO Debug port and a JTAG/SWD debug interface.

1.1 Family Features

TABLE 1-1: CEC1702 FEATURE LIST BY PACKAGE

CEC1702 Product Family	CEC1702
Package	84 WFBGA
Device ID	31h
Boundary Scan JTAG ID	021F2445h
SRAM Block (Primary use: code)	416KB
SRAM Block (Primary use: data)	64KB
Battery Backed SRAM	128 bytes
Trace FIFO Debug Port	Yes
Internal DMA Channels	14
16-bit Counter/Timer	4
Capture Timer	4
Compare Timer	1
Watchdog Timer (WDT)	1
Hibernation Timer	2
Week Timer	1
RTC	1
Battery-Powered General Purpose Output (BGPO)	1
Active Low VBAT-Powered Control Interface (VCI)	2
Keyboard Matrix Scan Support	13x8
I2C Host Controllers	4
I2C Ports	6
GPIOs	65
Pass-through GPIOs	2
Blinking/Breathing PWM	2
General Purpose SPI Master Controller	1
Quad SPI Master Controller	1
10-bit ADC Channels	5
16-bit PWMs	7
16-bit TACHs	2
UARTs	2
AES Hardware Support	128-256 bit
SHA Hashing Support	SHA-1 to SHA-512
Public Key Cryptography Support	RSA: 4K bit ECC: 640 bit
True Random Number Generator	1K bit

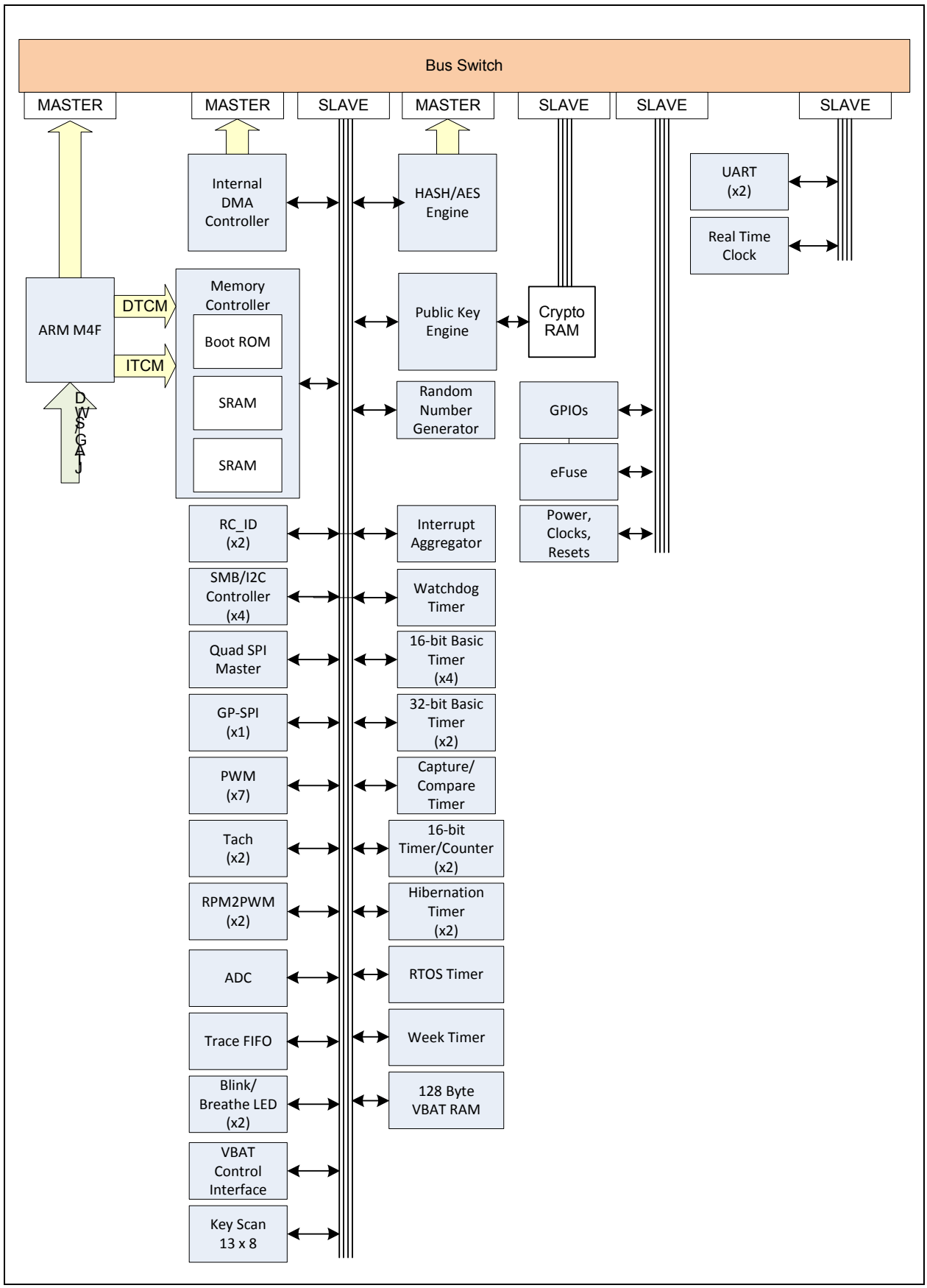
1.2 Boot ROM

Following the release of the RESET_EC signal, the processor will start executing code in the Boot ROM. The Boot ROM executes the SPI Flash Loader, which downloads User Code from an external SPI Flash and stores it in the internal Code RAM. Upon completion, the Boot ROM jumps into the User Code and starts executing as defined in the CEC1702 ROM Description Addendum.

The Boot ROM loads code from an external SPI Flash device. The interface supports SPI devices with dual and quad data rates, in addition to standard SPI devices. The downloaded code must configure the device's pins according to the platform's needs. After loading code, the Boot ROM leaves all pins in their default initial state.

1.3 CEC1702 Block Diagram

Note:	Not all features shown are available on all devices. Refer to Table 1-1, "CEC1702 Feature List by Package" for a list of the features by device.


Bus Switch
MASTER
MASTER
SLAVE
MASTER
SLAVE
SLAVE
SLAVE
ARM M4F
DTCM
ITCM
SWJ/SWD
Memory Controller
Boot ROM
SRAM
SRAM
Internal DMA Controller
HASH/AES Engine
Public Key Engine
Crypto RAM
Random Number Generator
GPIOs
eFuse
Power, Clocks, Resets
UART (x2)
Real Time Clock
RC_ID (x2)
Interrupt Aggregator
SMB/I2C Controller (x4)
Watchdog Timer
Quad SPI Master
16-bit Basic Timer (x4)
GP-SPI (x1)
32-bit Basic Timer (x2)
PWM (x7)
Capture/ Compare Timer
Tach (x2)
16-bit Timer/Counter (x2)
RPM2PWM (x2)
Hibernation Timer (x2)
ADC
RTOS Timer
Trace FIFO
Week Timer
Blink/ Breathe LED (x2)
128 Byte VBAT RAM
VBAT Control Interface
Key Scan 13 x 8

2.0 PIN CONFIGURATION

2.1 Description

The Pin Configuration chapter includes Pin List By Pin Name, Signal Description by Signal, Notes for Tables in this Chapter, Pin Default State Through Power Transitions, and Package.

2.2 Terminology and Symbols for Pins/Buffers

2.2.1 BUFFER TERMINOLOGY

Term	Definition
#	The '#' sign at the end of a signal name indicates an active-low signal
n	The lowercase 'n' preceding a signal name indicates an active-low signal
PWR	Power
PIO	Programmable as Input, Output, Open Drain Output, Bi-directional or Bi-directional with Open Drain Output. Configurable drive strength from 2ma to12ma. **Note:** All GPIOs have programmable drive strength options of 2ma, 4ma, 8ma and 12ma. GPIO pin drive strength is determined by the DRIVE_STRENGTH field in the Pin Control 2 Register.
In	Input only - I Type Input Buffer.
O2ma	O-2 mA Type Buffer.

2.2.2 PIN NAMING CONVENTIONS

1. Pin Name is composed of the multiplexed options separated by '/'. E.g., GPIOxxxx/SignalA/SignalB.
2. Parenthesis '()' are used to list aliases or alternate functionality for a single mux option. E.g. GPIOxxx(Alias)/SignalA/SignalB. The Alias is the intended usage for a specific GPIO. E.g., GPIOxxx(ICSP_DATA) is intended to indicate that ICSP_DATA signal may come out on this pin when the Mux Control is set for GPIOxxx. In this case, enabling the test mode takes precedence over the Mux Control selection.
3. Signal Names appended with a numeric value indicates the Instance Number. E.g., PWM0, PWM1, etc. indicates that PWM0 is the PWM output for PWM Instance 0, PWM1 is the PWM output for PWM Instance 1, etc. Note that this same instance number is shown in the Register Base Address tables linking the specific PWM block instance to a specific signal on the pinout. The instance number may be omitted if there in only one instance of the IP block implemented.

2.3 Notes for Tables in this Chapter

Note	Description
Note 1	When the JTAG_RST# pin is not asserted (logic'1'), the pins for the signal functions in the JTAG/SWD interface are unconditionally routed to the interface; the Pin Control register for these pins has no effect. When the JTAG_RST# pin is asserted (logic'0'), the signal functions in the JTAG/SWD interface are not routed to the interface and the Pin Control Register for these pins controls the muxing. The pin control registers can not route the JTAG interface to the pins. System Board Designer should terminate this pin in all functional state using jumpers and pull-up or pull down resistors, etc.
Note 2	I2C/SMBus Port pins can be mapped to any I2C/SMB Controller. The number in the I2C/SMBus signal names (I2Cxx_DATA) indicates the port value. E.g. I2C01_DATA represents I2C/SMBus Data Port 1
Note 3	VCI_IN# function works even when configured as GPIO.
Note 4	The Voltage Regulator Capacitor (VR_CAP) pin requires an external 1uF capacitor and a voltage range of 1.08V (min) to 1.32V (max).

2.4 Pin List By Pin Name

2.4.1 DEFAULT STATE

The default state for analog pins is Input. The default state for all pins that default to a GPIO function is also input, with pull-up and pull-down resistors disabled. The default state for pins that differ is shown in the following table. Entries for the Default State column are

- O2ma-Low: Push-Pull output, Slow slew rate, 2ma drive strength, grounded
- O2ma-High Push-Pull output, Slow slew rate, 2ma drive strength, high output
- In-PU Input, with pull-up resistor enabled

CEC1702-84	Signal	Default (if not GPIO)	Default State (if not In)
B1	BGPO0	BGPO0	O2ma-Low
J6	GPIO001/PWM4		
J5	GPIO002/PWM5		
A3	GPIO003/I2C00_SDA/SPI0_CS#		
B2	GPIO004/I2C00_SCL/SPI0_MOSI		
B5	GPIO007/I2C03_SDA		
A8	GPIO010/I2C03_SCL		
K1	GPIO012/I2C07_SDA/TOUT3		
J2	GPIO013/I2C07_SCL/TOUT2		
K2	GPIO016/GPTP-IN7/QSPI0_IO3/ICT3		
J7	GPIO017/GPTP-IN5/KSI0		
J3	GPIO020/KSI1		
J4	GPIO021/KSI2		
K9	GPIO026/TIN1/KSI3		
J10	GPIO027/TIN2/KSI4		
G7	GPIO030/TIN3/KSI5		
J8	GPIO031/KSI6		
H5	GPIO032/KSI7		
G4	GPIO034/RC_ID1/SPI0_CLK		
F10	GPIO036/RC_ID2/SPI0_MISO		
K8	GPIO040/KSO00		
C5	GPIO045/KSO01		
C9	GPIO046/KSO02		
B8	GPIO047/KSO03		
F3	GPIO050/FAN_TACH0/GTACH0		
E2	GPIO051/FAN_TACH1/GTACH1		
K10	GPIO053/PWM0/GPWM0		
J9	GPIO054/PWM1/GPWM1		
K7	GPIO055/PWM2/QSPI0_CS#		
K6	GPIO056/PWM3/QSPI0_CLK		
D9	GPIO104/UART0_TX		
E9	GPIO105/UART0_RX		

CEC1702-84	Signal	Default (if not GPIO)	Default State (if not In)
H9	GPIO107/KSO04		
G9	GPIO112/KSO05		
G10	GPIO113/KSO06		
H10	GPIO120/KSO07		
D10	GPIO121/QSPI1_IO0/KSO08		
B10	GPIO122/QSPI1_IO1/KSO09		
C10	GPIO124/QSPI1_CS#/KSO11		
A10	GPIO125/GPTP-OUT5/QSPI1_CLK/KSO12		
C6	GPIO127/UART0_CTS#		
E10	GPIO134/PWM10/UART1_RTS#		
E7	GPIO135/UART1_CTS#		
H6	GPIO140/ICT5		
C2	GPIO145/I2C09_SDA/JTAG_TDI		
B6	GPIO146/I2C09_SCL/JTAG_TDO		
A7	GPIO147/I2C08_SDA/JTAG_CLK		
B3	GPIO150/I2C08_SCL/JTAG_TMS		
A9	GPIO154/I2C02_SDA		
B7	GPIO155/I2C02_SCL		
D7	GPIO156/LED0		
B9	GPIO157/LED1		
A5	GPIO162/VCI_IN1#	VCI_IN1#	
B4	GPIO163/VCI_IN0#	VCI_IN0#	
A6	GPIO165/32KHZ_IN/CTOUT0		
F9	GPIO170/TFCLK/UART1_TX		
F8	GPIO171/TFDATA/UART1_RX/(JTAG_STRAP)		In-PU
F2	GPIO200/ADC00	ADC00	
G2	GPIO201/ADC01	ADC01	
H2	GPIO202/ADC02	ADC02	
G1	GPIO203/ADC03	ADC03	
H1	GPIO204/ADC04	ADC04	
K5	GPIO223/QSPI0_IO0		
K3	GPIO224/QSPI0_IO1		
D6	GPIO225/UART0_RTS#		
K4	GPIO227/QSPI0_IO2		
E8	JTAG_RST#	JTAG_RST#	
D2	RESETI#	RESETI#	
D5	VBAT	VBAT	
A1	VCI_OUT	VCI_OUT	O2ma-High
F1	VR_CAP	VR_CAP	
E3	VREF_ADC	VREF_ADC	
E4	VSS1	VSS1	

CEC1702-84	Signal	Default (if not GPIO)	Default State (if not In)
F7	VSS2	VSS2	
J1	VSS_ADC	VSS_ADC	
D4	VSS_ANALOG	VSS_ANALOG	
D1	VFLT_PLL	VFLT_PLL	
G6	VTR1	VTR1	
G5	VTR2	VTR2	
F4	VTR_ANALOG	VTR_ANALOG	
C1	VTR_PLL	VTR_PLL	
E1	VTR_REG	VTR_REG	
A4	XTAL1	XTAL1	
A2	XTAL2	XTAL2	

2.5 Pin List by Pin Number

2.5.1 POWER RAIL

The Power Rail column defines the power pin that provides I/O power for the signal pin.

2.5.2 PAD TYPES

The Pad Type column defines the type of pad associated with each signal. Some pins have signals with two different pad types sharing the pin; in this case, the pin is shown with the Pin Name but no pad type, followed by rows showing the pad type for each of the signals that share the pin. Pad Types are defined in the Section 38.0, "Electrical Specifications," on page 374.

- I/O Pad Types are defined in Section 38.2.4, "DC Electrical Characteristics for I/O Buffers," on page 376.
- The abbreviation “PWR” is used to denote power pins. The power supplies are defined in Section 38.2.1, "Power Supply Operational Characteristics," on page 374

2.5.3 GLITCH PROTECTION

Pins with glitch protection are glitch-free tristate pins and will not drive out while their associated power rail is rising. These glitch-free tristate pins require either an external pull-up or pull-down to set the state of the pin high or low.

Note:	If the pin needs to default low, a 1M ohm (max) external pull-down is required.

Pins without glitch protection may be susceptible to transitory changes as the power rail is rising.

Note:	The power rail must rise monotonically in order for glitch protection to operate.

BGPO GLITCH PROTECTION

All BGPO pins are glitch protected while VBAT power is applied.

The BGPO outputs are glitch protected on VBAT power as well as VTR power. As VBAT rises from ground, the BGPOx output are not driven until the VBAT power rail reaches approximately 1V. Once the VBAT power rail reaches approximately 1V, the BGPO outputs drive low.

Note:	It is recommended that a pull-down resistor be added to the BGPO pins.

2.5.4 OVER-VOLTAGE PROTECTION

For pins that have Over-voltage protection and the VTR*x* power rail that is supplying the pin is 3.3V, the pin can tolerate an input voltage of up to 5.5V without causing an error.

Note:	Pins with over-voltage protection may be pulled up externally to 5V supply. It is recommended to select strong pull-up resistor values (less than 10k ohms) that keep the pull-up voltage on the pin less than 3.8V and above 4.5V. If the voltage is 3.8V ≤ x ≤ 4.5V the pad current will be higher (65ua -nominal)

For pins with Over-voltage protection and the VTR*x* power rail that is supplying the pin is 1.8V, the pin can tolerate an input voltage of up to 3.6V without causing an error.

An input level that exceeds 105% of the power rail on a pin without Over-voltage protection may cause errors in the logic and may additionally damage internal circuitry.

2.5.5 UNDER-VOLTAGE PROTECTION

Pins that are identified as having Under-voltage PROTECTION may be configured so the will not sink excess current if powered by 3.3V and externally pulled up to 1.8V. The following configuration requirements must be met.

- If the pad is an output only pad type and it is configured as either open drain or the output is disabled.
- If the pin is a GPIO pin with a PIO pad type then is must be configured as open drain output with the input disabled. The input is disabled by setting the GPIO POWER_GATING bits to 11b.

2.5.6 BACKDRIVE PROTECTION

Assuming that the external voltage on the pin is within the parameters defined for the specific pad type, the backdrive protected pin will not sink excess current when it is at a lower potential than the external circuit. There are two cases where this occurs:

- The pad power is off and the external circuit is powered
- The pad power is on and the external circuitry is pulled to a higher potential than the pad power. This may occur on 3.3V powered pads that are 5V tolerant or on 1.8V powered pads that are 3.6V tolerant.

2.5.7 CEC1702 84 WFBGA

CEC1702-84	Pin Name	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
A1	VCI_OUT	VBAT	O2ma			X	X
A2	XTAL2	VBAT	I_AN				
A3	GPIO003/I2C00_SDA/SPI0_CS#	VTR1	PIO	X		X	X
A4	XTAL1	VBAT	I_AN				
A5	GPIO162/VCI_IN1#	VBAT	PIO	X		X	X
A6	GPIO165/32KHZ_IN/CTOUT0	VTR1	PIO	X		X	X
A7	GPIO147/I2C08_SDA/JTAG_CLK	VTR1	PIO	X		X	X
A8	GPIO010/I2C03_SCL	VTR1	PIO	X	X	X	X
A9	GPIO154/I2C02_SDA	VTR1	PIO	X	X	X	X
A10	GPIO125/GPTP-OUT5/QSPI1_CLK/KSO12	VTR1	PIO	X		X	X
B1	BGPO0	VBAT	O	X		X	X
B2	GPIO004/I2C00_SCL/SPI0_MOSI	VTR1	PIO	X		X	X
B3	GPIO150/I2C08_SCL/JTAG_TMS	VTR1	PIO	X		X	X
B4	GPIO163/VCI_IN0#	VBAT	PIO	X		X	X

CEC1702-84	Pin Name	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
B5	GPIO007/I2C03_SDA	VTR1	PIO	X	X	X	X
B6	GPIO146/I2C09_SCL/JTAG_TDO	VTR1	PIO	X		X	X
B7	GPIO155/I2C02_SCL	VTR1	PIO	X	X	X	X
B8	GPIO047/KSO03	VTR1	PIO	X		X	X
B9	GPIO157/LED1	VTR1	PIO	X	X	X	X
B10	GPIO122/QSPI1_IO1/KSO09	VTR1	PIO	X		X	X
C1	VTR_PLL		PWR				
C2	GPIO145/I2C09_SDA/JTAG_TDI	VTR1	PIO	X		X	X
C5	GPIO045/KSO01	VTR1	PIO	X		X	X
C6	GPIO127/UART0_CTS#	VTR1	PIO	X		X	X
C9	GPIO046/KSO02	VTR1	PIO	X		X	X
C10	GPIO124/QSPI1_CS#/KSO11	VTR1	PIO	X		X	X
D1	VFLT_PLL		PWR				
D2	RESETI#	VTR1	Om	X		X	X
D4	VSS_ANALOG		PWR				
D5	VBAT		PWR				
D6	GPIO225/UART0_RTS#	VTR1	PIO	X		X	X
D7	GPIO156/LED0	VTR1	PIO	X	X	X	X
D9	GPIO104/UART0_TX	VTR1	PIO	X		X	X
D10	GPIO121/QSPI1_IO0/KSO08	VTR1	PIO	X		X	X
E1	VTR_REG		PWR				
E2	GPIO051/FAN_TACH1/GTACH1	VTR1	PIO	X	X	X	X
E3	VREF_ADC		PWR			X	
E4	VSS1		PWR				
E7	GPIO135/UART1_CTS#	VTR1	PIO	X		X	X
E8	JTAG_RST#	VTR1	In	X		X	X
E9	GPIO105/UART0_RX	VTR1	PIO	X		X	X
E10	GPIO134/PWM10/UART1_RTS#	VTR1	PIO	X		X	X
F1	VR_CAP		PWR				
F2	GPIO200/ADC00	VTR1					
	GPIO200		PIO	X		X	
	ADC00		I_AN	X		X	
F3	GPIO050/FAN_TACH0/GTACH0	VTR1	PIO	X	X	X	X
F4	VTR_ANALOG		PWR				
F7	VSS2		PWR				
F8	GPIO171/TFDATA/UART1_RX/(JTAG_STRAP)	VTR1	PIO	X		X	X
F9	GPIO170/TFCLK/UART1_TX	VTR1	PIO	X		X	X

CEC1702-84	Pin Name	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
F10	GPIO036/RC_ID2/SPI0_MISO	VTR1					
	GPIO036/SPI0_MISO		PIO	X		X	
	RC_ID2		I_AN	X		X	
G1	GPIO203/ADC03	VTR1					
	GPIO203		PIO	X		X	
	ADC03		I_AN	X		X	
G2	GPIO201/ADC01	VTR1					
	GPIO201		PIO	X		X	
	ADC01		I_AN	X		X	
G4	GPIO034/RC_ID1/SPI0_CLK	VTR1					
	GPIO034/SPI0_CLK		PIO	X		X	
	RC_ID1		I_AN	X		X	
G5	VTR2		PWR				
G6	VTR1		PWR				
G7	GPIO030/TIN3/KSI5	VTR2	PIO	X		X	X
G9	GPIO112/KSO05	VTR2	PIO	X		X	X
G10	GPIO113/KSO06	VTR2	PIO	X		X	X
H1	GPIO204/ADC04	VTR1					
	GPIO204		PIO	X		X	
	ADC04		I_AN	X		X	
H2	GPIO202/ADC02	VTR1					
	GPIO202		PIO	X		X	
	ADC02		I_AN	X		X	
H5	GPIO032/KSI7	VTR2	PIO	X		X	X
H6	GPIO140/ICT5	VTR2	PIO	X		X	X
H9	GPIO107/KSO04	VTR2	PIO	X		X	X
H10	GPIO120/KSO07	VTR2	PIO	X		X	X
J1	VSS_ADC		PWR				
J2	GPIO013/I2C07_SCL/TOUT2	VTR2	PIO	X		X	X
J3	GPIO020/KSI1	VTR2	PIO	X		X	X
J4	GPIO021/KSI2	VTR2	PIO	X		X	X
J5	GPIO002/PWM5	VTR2	PIO	X		X	X
J6	GPIO001/PWM4	VTR2	PIO	X		X	X
J7	GPIO017/GPTP-IN5/KSI0	VTR2	PIO	X		X	X
J8	GPIO031/KSI6	VTR2	PIO	X		X	X
J9	GPIO054/PWM1/GPWM1	VTR2	PIO	X	X	X	X
J10	GPIO027/TIN2/KSI4	VTR2	PIO	X		X	X
K1	GPIO012/I2C07_SDA/TOUT3	VTR2	PIO	X		X	X
K2	GPIO016/GPTP-IN7/QSPI0_IO3/ICT3	VTR2	PIO	X		X	X

CEC1702-84	Pin Name	Power Rail	Pad Type	Glitch Prot	Over-voltage Prot	Under-voltage Prot	Backdrive Prot
K3	GPIO224/QSPI0_IO1	VTR2	PIO	X		X	X
K4	GPIO227/QSPI0_IO2	VTR2	PIO	X		X	X
K5	GPIO223/QSPI0_IO0	VTR2	PIO	X		X	X
K6	GPIO056/PWM3/QSPI0_CLK	VTR2	PIO	X		X	X
K7	GPIO055/PWM2/QSPI0_CS#	VTR2	PIO	X		X	X
K8	GPIO040/KSO00	VTR2	PIO	X		X	X
K9	GPIO026/TIN1/KSI3	VTR2	PIO	X		X	X
K10	GPIO053/PWM0/GPWM0	VTR2	PIO	X	X	X	X

2.6 Signal Description by Signal

EMULATED POWER WELL

Power well emulation for GPIOs and for signals that are multiplexed with GPIO signals is controlled by the POWER_-GATING field in the GPIO Pin Control Register. Power well emulation for signals that are not multiplexed with GPIO signals is defined by the entries in this column.

GATED STATE

This column defines the internal value of an input signal when either its emulated power well is inactive or it is not selected by the GPIO alternate function MUX. A value of “No Gate” means that the internal signal always follows the pin even when the emulated power well is inactive.

Note: Gated state is only meaningful to the operation of input signals. A gated state on an output pin defines the internal behavior of the GPIO MUX and does not imply pin behavior.

Signal	Emulated Power Rail	Gated State	Notes
ADC00	VTR	Low	
ADC01	VTR	Low	
ADC02	VTR	Low	
ADC03	VTR	Low	
ADC04	VTR	Low	
BGND		Low	
BGPO0	VTR	Low	
CTOUT0	VTR	Low	
FAN_TACH0	VTR	Low	
FAN_TACH1	VTR	Low	
GPIO001	VTR	No Gate	
GPIO002	VTR	No Gate	
GPIO003	VTR	No Gate	
GPIO004	VTR	No Gate	
GPIO007	VTR	No Gate	

Signal	Emulated Power Rail	Gated State	Notes
GPIO010	VTR	No Gate	
GPIO012	VTR	No Gate	
GPIO013	VTR	No Gate	
GPIO016	VTR	No Gate	
GPIO017	VTR	No Gate	
GPIO020	VTR	No Gate	
GPIO021	VTR	No Gate	
GPIO026	VTR	No Gate	
GPIO027	VTR	No Gate	
GPIO030	VTR	No Gate	
GPIO031	VTR	No Gate	
GPIO032	VTR	No Gate	
GPIO034	VTR	No Gate	
GPIO036	VTR	No Gate	
GPIO040	VTR	No Gate	
GPIO045	VTR	No Gate	
GPIO046	VTR	No Gate	
GPIO047	VTR	No Gate	
GPIO050	VTR	No Gate	
GPIO051	VTR	No Gate	
GPIO053	VTR	No Gate	
GPIO054	VTR	No Gate	
GPIO055	VTR	No Gate	
GPIO056	VTR	No Gate	
GPIO104	VTR	No Gate	
GPIO106	VTR	No Gate	
GPIO107	VTR	No Gate	
GPIO112	VTR	No Gate	
GPIO113	VTR	No Gate	
GPIO120	VTR	No Gate	
GPIO121	VTR	No Gate	
GPIO122	VTR	No Gate	
GPIO124	VTR	No Gate	
GPIO125	VTR	No Gate	
GPIO127	VTR	No Gate	
GPIO134	VTR	No Gate	
GPIO135	VTR	No Gate	
GPIO140	VTR	No Gate	
GPIO145	VTR	No Gate	
GPIO146	VTR	No Gate	
GPIO147	VTR	No Gate	
GPIO150	VTR	No Gate	
GPIO154	VTR	No Gate	

Signal	Emulated Power Rail	Gated State	Notes
GPIO155	VTR	No Gate	
GPIO156	VTR	No Gate	
GPIO157	VTR	No Gate	
GPIO162	VTR	No Gate	
GPIO163	VTR	No Gate	
GPIO165	VTR	No Gate	
GPIO170	VTR	No Gate	
GPIO171	VTR	No Gate	
GPIO200	VTR	No Gate	
GPIO201	VTR	No Gate	
GPIO202	VTR	No Gate	
GPIO203	VTR	No Gate	
GPIO204	VTR	No Gate	
GPIO223	VTR	No Gate	
GPIO224	VTR	No Gate	
GPIO225	VTR	No Gate	
GPIO227	VTR	No Gate	
GPTP-IN5	VTR	No Gate	
GPTP-OUT5	VTR	No Gate	
GPWM0	VTR	Low	
GPWM1	VTR	Low	
GTACH0	VTR	Low	
GTACH1	VTR	Low	
I2C00_SCL	VTR	High	Note 2
I2C00_SDA	VTR	High	Note 2
I2C02_SCL	VTR	High	Note 2
I2C02_SDA	VTR	High	Note 2
I2C03_SCL	VTR	High	Note 2
I2C03_SDA	VTR	High	Note 2
I2C07_SCL	VTR	High	Note 2
I2C07_SDA	VTR	High	Note 2
I2C08_SCL	VTR	High	Note 2
I2C08_SDA	VTR	High	Note 2
I2C09_SCL	VTR	High	Note 2
I2C09_SDA	VTR	High	Note 2
ICT3	VTR	Low	
ICT5	VTR	Low	
JTAG_CLK	VTR	Low	
JTAG_RST#	VTR	High	Note 1
JTAG_TDI	VTR	Low	
JTAG_TDO	VTR	Low	
JTAG_TMS	VTR	Low	
KSI0	VTR	Low	

Signal	Emulated Power Rail	Gated State	Notes
KSI1	VTR	Low	
KSI2	VTR	Low	
KSI3	VTR	Low	
KSI4	VTR	Low	
KSI5	VTR	Low	
KSI6	VTR	Low	
KSI7	VTR	Low	
KSO00	VTR	Low	
KSO01	VTR	Low	
KSO02	VTR	Low	
KSO03	VTR	Low	
KSO04	VTR	Low	
KSO05	VTR	Low	
KSO06	VTR	Low	
KSO07	VTR	Low	
KSO08	VTR	Low	
KSO09	VTR	Low	
KSO11	VTR	Low	
KSO12	VTR	Low	
LED0	VTR	Low	
LED1	VTR	Low	
PWM0	VTR	Low	
PWM1	VTR	Low	
PWM2	VTR	Low	
PWM3	VTR	Low	
PWM4	VTR	Low	
PWM5	VTR	Low	
PWM10	VTR	Low	
QSPI0_CLK	VTR	Low	
QSPI0_CS#	VTR	High	
QSPI0_IO0	VTR	Low	
QSPI0_IO1	VTR	Low	
QSPI0_IO2	VTR	Low	
QSPI0_IO3	VTR	Low	
QSPI1_CLK	VTR	Low	
QSPI1_CS#	VTR	High	
QSPI1_IO0	VTR	Low	
QSPI1_IO1	VTR	Low	
RC_ID1	VTR	Low	
RC_ID2	VTR	Low	
RESETI#	VTR	High	
SPI0_CLK	VTR	Low	
SPI0_CS#	VTR	High	

Signal	Emulated Power Rail	Gated State	Notes
SPI0_MISO	VTR	Low	
SPI0_MOSI	VTR	Low	
TFCLK	VTR	Low	
TFDATA	VTR	Low	
TIN1	VTR	Low	
TIN2	VTR	Low	
TIN3	VTR	Low	
UART0_CTS#	VTR	Low	
UART0_RTS#	VTR	Low	
UART0_RX	VTR	Low	
UART0_TX	VTR	Low	
UART1_CTS#	VTR	Low	
UART1_RTS#	VTR	Low	
UART1_RX	VTR	Low	
UART1_TX	VTR	Low	
VBAT			
VCI_IN0#	VTR	No Gate	Note 3
VCI_IN1#	VTR	No Gate	Note 3
VCI_OUT	VTR	Low	
VFLT_PLL			
VR_CAP			Note 4
VREF_ADC			
VSS_ADC			
VSS_ANALOG			
VSS_REG			
VSS1			
VSS2			
VTR_ANALOG			
VTR_PLL			
VTR_REG			
VTR1			
VTR2			
XTAL1			
XTAL2			

2.7 Signal Description by interface

CEC1702 84 WFBGA	Interface		Notes
16-Bit Counter/Timer Interface			
K9	TIN1	16-Bit Counter/Timer Input 2	
J10	TIN2	16-Bit Counter/Timer Input 3	
G7	TIN3	16-Bit Counter/Timer Input 4	
Analog Data Acquisition Interface			
F2	ADC00	ADC Channel 0	
G2	ADC01	ADC Channel 1	
H2	ADC02	ADC Channel 2	
G1	ADC03	ADC Channel 3	
H1	ADC04	ADC Channel 4	
E3	VREF_ADC	ADC Voltage Reference	
Capture Timer interface			
A6	CTOUT0	Compare Timer Output 0	
K2	ICT3	Input Capture Timer Input 3	
H6	ICT5	Input Capture Timer Input 5	
Fan PWM and Tachometer			
F3	FAN_TACH0	Fan Tachometer Input 0/Input Capture Timer Input 0	
E2	FAN_TACH1	Fan Tachometer Input 1/Input Capture Timer Input 1	
K10	GPWM0	PWM Output from RPM-based Fan Speed Control Algorithm, PWM 0	
J9	GPWM1	PWM Output from RPM-based Fan Speed Control Algorithm, PWM 1	
F3	GTACH0	Tach Input to RPM-based Fan Speed Control Algorithm, Tach 0	
E2	GTACH1	Tach Input to RPM-based Fan Speed Control Algorithm, Tach 1	
K10	PWM0	Pulse Width Modulator Output 0	
J9	PWM1	Pulse Width Modulator Output 1	
K7	PWM2	Pulse Width Modulator Output 2	
K6	PWM3	Pulse Width Modulator Output 3	
J6	PWM4	Pulse Width Modulator Output 4	
J5	PWM5	Pulse Width Modulator Output 5	
E10	PWM10	Pulse Width Modulator Output 10	
General Purpose Input/Outputs			
J6	GPIO001	General Purpose Input/Output Port	
J5	GPIO002	General Purpose Input/Output Port	
A3	GPIO003	General Purpose Input/Output Port	
B2	GPIO004	General Purpose Input/Output Port	
B5	GPIO007	General Purpose Input/Output Port	

CEC1702 84 WFBGA	Interface		Notes
A8	GPIO010	General Purpose Input/Output Port	
K1	GPIO012	General Purpose Input/Output Port	
J2	GPIO013	General Purpose Input/Output Port	
K2	GPIO016	General Purpose Input/Output Port	
J7	GPIO017	General Purpose Input/Output Port	
J3	GPIO020	General Purpose Input/Output Port	
J4	GPIO021	General Purpose Input/Output Port	
K9	GPIO026	General Purpose Input/Output Port	
J10	GPIO027	General Purpose Input/Output Port	
G7	GPIO030	General Purpose Input/Output Port	
J8	GPIO031	General Purpose Input/Output Port	
H5	GPIO032	General Purpose Input/Output Port	
G4	GPIO034	General Purpose Input/Output Port	
F10	GPIO036	General Purpose Input/Output Port	
K8	GPIO040	General Purpose Input/Output Port	
C5	GPIO045	General Purpose Input/Output Port	
C9	GPIO046	General Purpose Input/Output Port	
B8	GPIO047	General Purpose Input/Output Port	
F3	GPIO050	General Purpose Input/Output Port	
E2	GPIO051	General Purpose Input/Output Port	
K10	GPIO053	General Purpose Input/Output Port	
J9	GPIO054	General Purpose Input/Output Port	
K7	GPIO055	General Purpose Input/Output Port	
K6	GPIO056	General Purpose Input/Output Port	
D9	GPIO104	General Purpose Input/Output Port	
E9	GPIO105	General Purpose Input/Output Port	
H9	GPIO107	General Purpose Input/Output Port	
G9	GPIO112	General Purpose Input/Output Port	
G10	GPIO113	General Purpose Input/Output Port	
H10	GPIO120	General Purpose Input/Output Port	
D10	GPIO121	General Purpose Input/Output Port	
B10	GPIO122	General Purpose Input/Output Port	
C10	GPIO124	General Purpose Input/Output Port	
A10	GPIO125	General Purpose Input/Output Port	
C6	GPIO127	General Purpose Input/Output Port	
E10	GPIO134	General Purpose Input/Output Port	
E7	GPIO135	General Purpose Input/Output Port	
H6	GPIO140	General Purpose Input/Output Port	

CEC1702 84 WFBGA	Interface		Notes
C2	GPIO145	General Purpose Input/Output Port	
B6	GPIO146	General Purpose Input/Output Port	
A7	GPIO147	General Purpose Input/Output Port	
B3	GPIO150	General Purpose Input/Output Port	
A9	GPIO154	General Purpose Input/Output Port	
B7	GPIO155	General Purpose Input/Output Port	
D7	GPIO156	General Purpose Input/Output Port	
B9	GPIO157	General Purpose Input/Output Port	
A5	GPIO162	General Purpose Input/Output Port	
B4	GPIO163	General Purpose Input/Output Port	
A6	GPIO165	General Purpose Input/Output Port	
F9	GPIO170	General Purpose Input/Output Port	
F8	GPIO171	General Purpose Input/Output Port	
F2	GPIO200	General Purpose Input/Output Port	
G2	GPIO201	General Purpose Input/Output Port	
H2	GPIO202	General Purpose Input/Output Port	
G1	GPIO203	General Purpose Input/Output Port	
H1	GPIO204	General Purpose Input/Output Port	
K5	GPIO223	General Purpose Input/Output Port	
K3	GPIO224	General Purpose Input/Output Port	
D6	GPIO225	General Purpose Input/Output Port	
K4	GPIO227	General Purpose Input/Output Port	
General Purpose Pass-Through Ports			
J7	GPTP-IN5	General Purpose Pass Through Port Input 5	
A10	GPTP-OUT5	General Purpose Pass Through Port Output 5	
I2C Interface			
B2	I2C00_SCL	I2C Controller Port 0 Clock	Note 2
A4	I2C00_SDA	I2C Controller Port 0 Data	Note 2
B7	I2C02_SCL	I2C Controller Port 2 Clock	Note 2
A9	I2C02_SDA	I2C Controller Port 2 Data	Note 2
A8	I2C03_SCL	I2C Controller Port 3 Clock	Note 2
B5	I2C03_SDA	I2C Controller Port 3 Data	Note 2
J2	I2C07_SCL	I2C Controller Port 7 Clock	Note 2
K1	I2C07_SDA	I2C Controller Port 7 Data	Note 2
B3	I2C08_SCL	I2C Controller Port 8 Clock	Note 2
A7	I2C08_SDA	I2C Controller Port 8 Data	Note 2
B6	I2C09_SCL	I2C Controller Port 9 Clock	Note 2
C2	I2C09_SDA	I2C Controller Port 9 Data	Note 2

CEC1702 84 WFBGA	Interface		Notes
JTAG and Debug			
A7	JTAG_CLK	JTAG Test Clock. Also ARM SWDCLK	
E8	JTAG_RST#	JTAG Test Reset (active low)	Note 1
C2	JTAG_TDI	JTAG Test Data In	
B6	JTAG_TDO	JTAG Test Data Out. Also ARM SWO	
B3	JTAG_TMS	JTAG Test Mode Select. Also ARM SWDIO	
F9	TFCLK	Trace FIFO debug port - clock	
F8	TFDATA	Trace FIFO debug port - data	
Keyboard Scan Interface			
J7	KSI0	Keyboard Scan Matrix Input 0	
J3	KSI1	Keyboard Scan Matrix Input 1	
J4	KSI2	Keyboard Scan Matrix Input 1	
K9	KSI3	Keyboard Scan Matrix Input 3	
J10	KSI4	Keyboard Scan Matrix Input 4	
G7	KSI5	Keyboard Scan Matrix Input 5	
J8	KSI6	Keyboard Scan Matrix Input 6	
H5	KSI7	Keyboard Scan Matrix Input 7	
K8	KSO00	Keyboard Scan Matrix Output 0	
C5	KSO01	Keyboard Scan Matrix Output 1	
C9	KSO02	Keyboard Scan Matrix Output 2	
B8	KSO03	Keyboard Scan Matrix Output 3	
H9	KSO04	Keyboard Scan Matrix Output 4	
G9	KSO05	Keyboard Scan Matrix Output 5	
G10	KSO06	Keyboard Scan Matrix Output 6	
H10	KSO07	Keyboard Scan Matrix Output 7	
D10	KSO08	Keyboard Scan Matrix Output 8	
B10	KSO09	Keyboard Scan Matrix Output 9	
C10	KSO11	Keyboard Scan Matrix Output 11	
A10	KSO12	Keyboard Scan Matrix Output 12	
Master Clock Interface			
A4	XTAL1	32.768 KHz Crystal Input	
A2	XTAL2	32.768 KHz Crystal Output (single-ended clock input)	
Miscellaneous Functions			
D7	LED0	LED Output 0	
B9	LED1	LED Output 1	
G4	RC_ID1	RC Identification Detection 1	
F10	RC_ID2	RC Identification Detection 2	

CEC1702 84 WFBGA	Interface		Notes
D2	RESETI#	System Reset Input	
Power			
D5	VBAT	VBAT supply	
D1	VFLT_PLL	Filtered power input for PLL	
F1	VR_CAP	Internal Voltage Regulator Output (Capacitor Required)	Note 4
J1	VSS_ADC	Analog ADC VTR associated ground	
E4	VSS1	VTR I/O Ground pin region 1	
F7	VSS2	VTR I/O Ground pin region 2	
F4	VTR_ANALOG	VTR Power Supply for Internal Analog Logic	
C1	VTR_PLL	VTR associated power used for PLL	
E1	VTR_REG	VTR Internal Voltage Regulator Power Supply	
G6	VTR1	VTR I/O Power, pin region 1	
G5	VTR2	VTR I/O Power, pin region 2	
Serial Ports			
C6	UART0_CTS#	UART 0, Clear to Send Input	
D6	UART0_RTS#	UART 0, Request to Send Output	
E9	UART0_RX	UART 0, Receive Data	
D9	UART0_TX	UART 0, Transmit Data	
E7	UART1_CTS#	UART 1, Clear to Send Input	
E10	UART1_RTS#	UART 1, Request to Send Output	
F8	UART1_RX	UART 1, Receive Data	
F9	UART1_TX	UART 1, Transmit Data	
SPI Controllers Interface			
A10	QSPI1_CLK	Quad SPI Controller Clock, Port 1	
C10	QSPI1_CS#	Quad SPI Controller Chip Select, Port 1	
D10	QSPI1_IO0	Quad SPI Controller Data 0, Port 1	
B10	QSPI1_IO1	Quad SPI Controller Data 1, Port 1	
K6	QSPI0_CLK	Quad SPI Controller Clock, Port 0	
K7	QSPI0_CS#	Quad SPI Controller Chip Select, Port 0	
K5	QSPI0_IO0	Quad SPI Controller Data 0, Port 0	
K3	QSPI0_IO1	Quad SPI Controller Data 1, Port 0	
K4	QSPI0_IO2	Quad SPI Controller Data 2, Port 0	
K2	QSPI0_IO3	Quad SPI Controller Data 3, Port 0	
G4	SPI0_CLK	GP-SPI SPI Clock	
A4	SPI0_CS#	GP-SPI Chip Select	
F10	SPI0_MISO	GP-SPI SPI Output	
B2	SPI0_MOSI	GP-SPI SPI Input	

CEC1702 84 WFBGA	Interface		Notes
VBAT-Powered Control Interface			
B1	BGPO0	VBAT driven GPO	
B4	VCI_IN0#	Input can cause wakeup or interrupt event, active low	Note 3
A5	VCI_IN1#	Input can cause wakeup or interrupt event, active low	Note 3

2.8 Strapping Options

GPIO171 is used for the TAP Controller select strap. If any of the JTAG TAP controllers are used, GPIO171 must only be configured as an output to a VTR powered external function. GPIO171 may only be configured as an input when the JTAG TAP controllers are not needed or when an external driver does not violate the Slave Select Timing.See Section 36.2.1, "TAP Controller Select Strap Option".

TABLE 2-1: STRAPS AND MEANING

Pin	Function	Definition
GPIO171/TFDATA/ UART1_RX/(JTAG_STRAP)	JTAG Boundary Scan	1=Use the JAG TAP Controller for Boundary Scan 0=The JTAG TAP Controller is used for debug