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Kintex-7 FPGA KC724 GTX Transceiver Characterization Board

User Guide

UG932 (v2.2) October 10, 2014

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/10/2012	1.0	Initial Xilinx release.
7/29/2013	2.0	Updated Table 1-15 and Appendix B, Master Constraints File Listing.
12/13/2013	2.1	Updated disclaimer and copyright. Updated Table 1-6, Table 1-7, Table 1-8, Table 1-9, Table 1-10, Table 1-11, Table 1-15, and Table 1-16.
10/10/2014	2.2	Updated first paragraph and modified vendor list in 7 Series GTX Transceiver Power Module. Removed vendor list from References.

Table of Contents

Appendix E: Regulatory and Compliance Information

Chapter 1

KC724 Board Features and Operation

This chapter describes the components, features, and operation of the KC724 Kintex®-7 FPGA GTX Transceiver Characterization Board. The KC724 board provides the hardware environment for characterizing and evaluating the GTX transceivers available on the Kintex-7 XC7K325T-3 FFG900E FPGA. The KC724 board schematic, bill-of-material (BOM), layout files, and reference designs are available online at:

Kintex-7 FPGA KC724 Characterization Kit website

KC724 Board Features

- Kintex-7 XC7K325T-3 FFG900E FPGA
- Onboard power supplies for all necessary voltages
- Terminal blocks for optional use of external power supplies
- Digilent USB JTAG programming port
- System ACE™ SD controller
- Power module supporting Kintex-7 FPGA GTX transceiver power requirements
- A fixed, 200 MHz 2.5V LVDS oscillator wired to multi-region clock capable (MRCC) inputs
- Two pairs of differential MRCC inputs with SMA connectors
- SuperClock-2 module supporting multiple frequencies
- Four Samtec BullsEye connector pads for the GTX transceivers and reference clocks
- Power status LEDs
- General purpose DIP switches, LEDs, push buttons, and test I/O
- Two VITA 57.1 FPGA mezzanine card (FMC) high pin count (HPC) connectors
- USB-to-UART bridge
- I2C bus
- PMBus connectivity to onboard digital power supplies
- Active cooling for the FPGA

The KC724 board block diagram is shown in Figure 1-1.

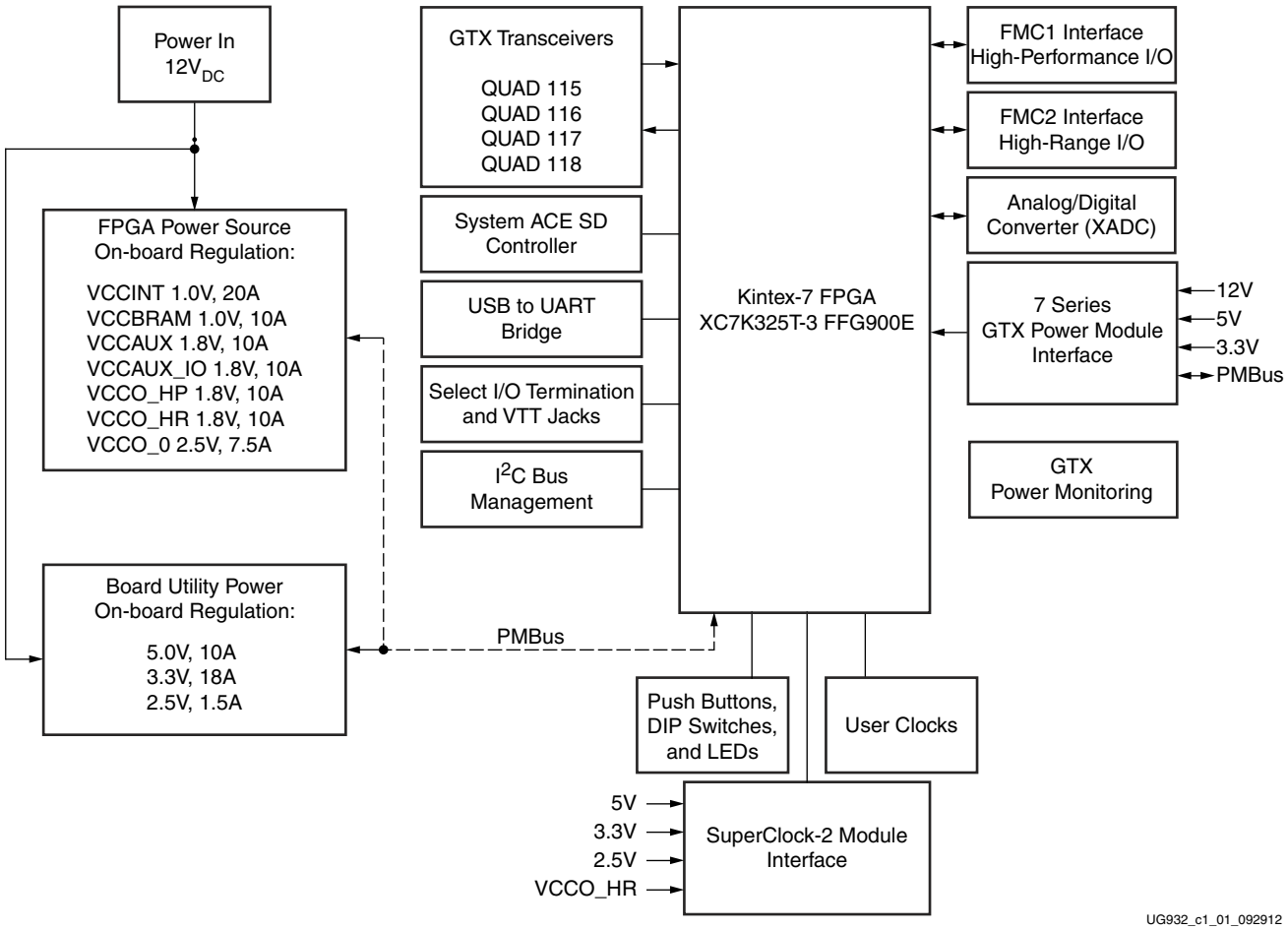


Figure 1-1: **KC724 Board Block Diagram**

Detailed Description

Figure 1-2 shows the KC724 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

Caution! The KC724 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

Caution! Do not remove the rubber feet from the board. The feet provide clearance to prevent short circuits on the back side of the board.

Note: Figure 1-2 is for reference only and might not reflect the current revision of the board.

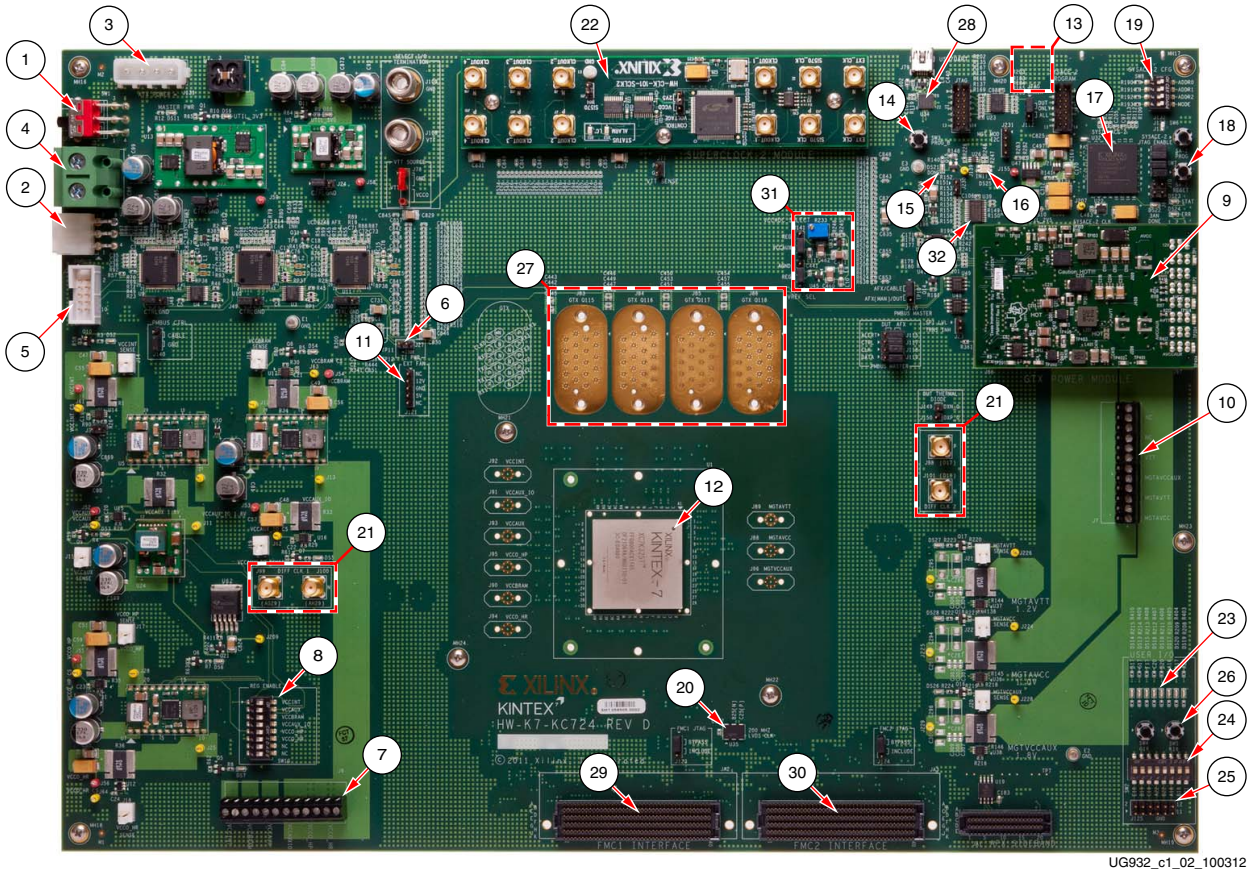


Figure 1-2: **KC724 Board Features. Callouts Listed in Table 1-1**

Table 1-1: **KC724 Board Feature Descriptions**

Figure 1-2 Callout	Reference Designator	Feature Description
1	SW1	Power Switch, page 9
2	J2	12V Mini-Fit Connector, page 9
3	J131	12V ATX Connector, page 9
4	J5	12V Euro-Mag Connector, page 9
5	J26	TI PMBus cable connector, page 13
6	J27	Regulation inhibit connector, page 13
7	J6	Core power terminal block (see Using External Power Sources, page 12)
8	SW10	Core power regulator enable switches, page 13
9		7 Series GTX Transceiver Power Module, page 14
10	J7	GTX transceiver power terminal block, page 15
11	J121	Active Heatsink Power Connector, page 16
12	U1	Kintex-7 XC7K325T-3 FFG900E FPGA, page 17
13	U8	USB JTAG configuration port (Digilent module), page 17
14	SW3	PROG_B Push Button, page 18
15	DS21	DONE LED, page 18
16	DS25	INIT LED, page 19
17	U32	System ACE SD Controller, page 19
18	SW7	System ACE SD Controller Reset, page 19
19	SW8	System ACE SD Configuration Address DIP Switches, page 19
20	U35	200 MHz 2.5V LVDS Oscillator, page 20
21	J98, J99, J100, J101	Differential SMA MRCC Pin Inputs, page 20
22		SuperClock-2 Module, page 20
23	DS13, DS14, DS15, DS16, DS17, DS18, DS19, DS20	User LEDs (Active High), page 22
24	SW2	User DIP Switches (Active High), page 22
25	J125	User Test I/O, page 22
26	SW4, SW5	User Push Buttons (Active High), page 23
27	J83, J84, J85, J86	GTX transceiver connector pads, page 23
28	U34	USB-to-UART Bridge, page 28
29	JA2	FMC1 Connector, page 29
30	JA3	FMC2 Connector, page 29

Table 1-1: **KC724 Board Feature Descriptions *(Cont'd)***

Figure 1-2 Callout	Reference Designator	Feature Description
31		XADC, page 40
32	U39	I2C Bus Management, page 41

Power Management

Callouts 1 through 11 shown in Figure 1-2 refer to components associated with the board's power management system.

Board Power and Switch

The KC724 board is powered through J2 (callout 2, Figure 1-2) using the 12V AC adapter included with the board. J2 is a 6-pin (2 x 3) right angle Mini-Fit type connector.

Caution! When powering the board through J2, use only the power supply provided for use with this board (Xilinx part number 3800033).

Caution! Do **NOT** plug a PC ATX power supply 6-pin connector into J2 on the KC724 board. The ATX 6-pin connector has a different pinout than J2. Connecting an ATX 6-pin connector into J2 will damage the KC724 board and void the board warranty.

Power can also be provided through:

- Connector J131 which accepts an ATX hard disk 4-pin power plug
- Euro-Mag terminal block J5 which can be used to connect to a bench-top power supply

Caution! Because terminal block J5 provides no reverse polarity protection, use a power supply with a current limit set at 5A max.

Caution! Do NOT apply power to J2 and connectors J131 and/or J5 at the same time. Doing so will damage the KC724 board.

The KC724 board power is turned on or off by switch SW1 (callout 1, Figure 1-2). When the switch is in the ON position, power is applied to the board and green LED DS11 illuminates.

Onboard Power Regulation

Figure 1-3 shows the onboard power supply architecture.

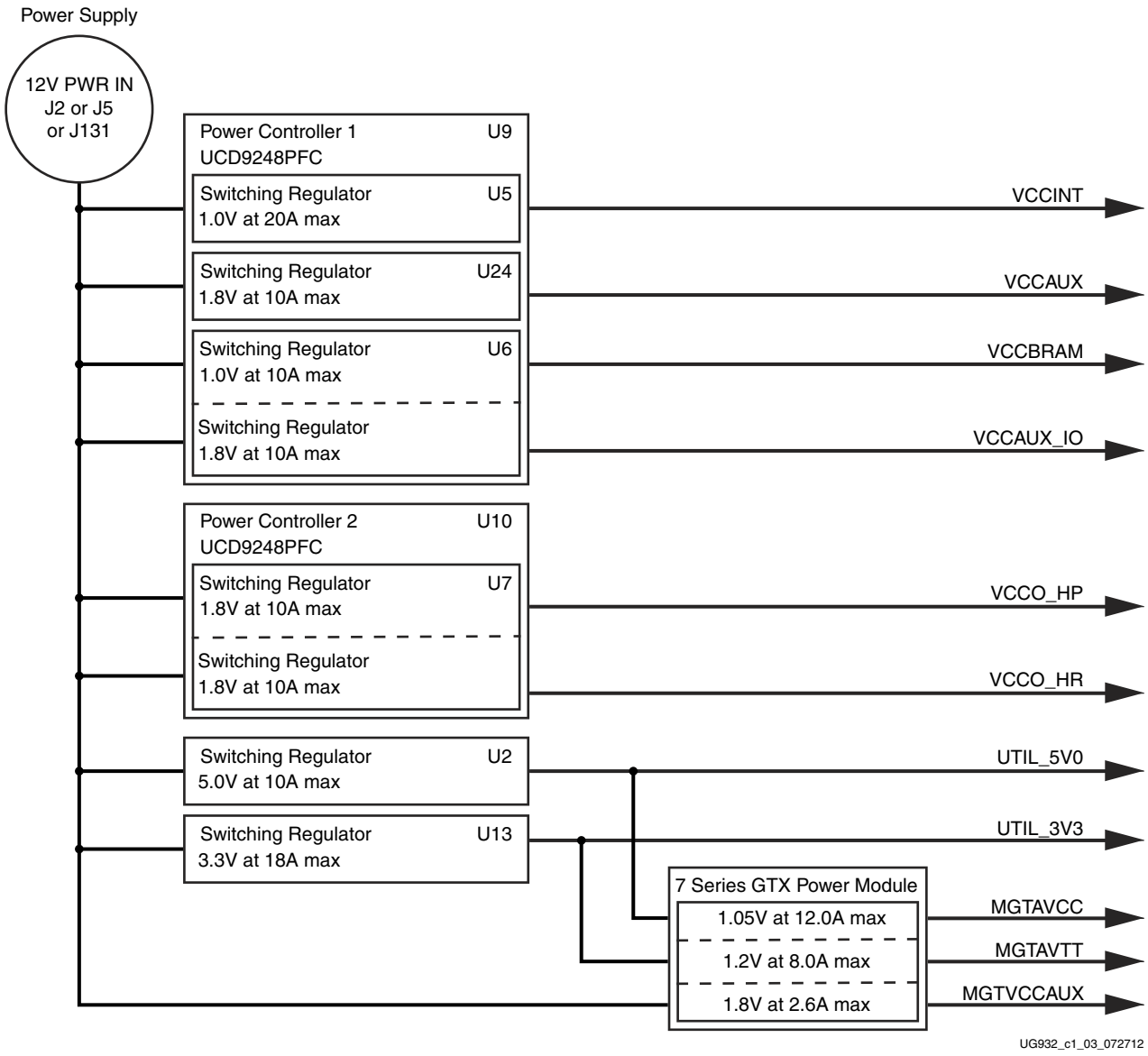


Figure 1-3: **KC724 Board Power Supply Block Diagram**

The KC724 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the core and utility voltages listed in Table 1-2. The board can also be configured to use an external bench power supply for each voltage. See Using External Power Sources.

Table 1-2: **Onboard Power System Devices**

Device	Reference Designator	Description	Power Rail Net Name	Power Rail Voltage
Core voltage controller and regulators				
UCD9248PFC	U9	PMBus compliant digital PWM system controller (Address = 52)		
PTD08D210W	U5	Adjustable switching regulator dual 10A, 0.6V to 3.6V	VCCINT	1.0V
PTD08A010W	U24	Adjustable switching regulator 10A, 0.6Vto 3.6V	VCCAUX	1.8V
PTD08D210W (V_{OUT} A)	U6	Adjustable switching regulator dual 10A, 0.6Vto 3.6V	VCCBRAM	1.0V
PTD08D210W (V_{OUT} B)		Adjustable switching regulator dual 10A, 0.6Vto 3.6V	VCCAUX_IO	1.8V
UCD9248PFC	U10	PMBus compliant digital PWM system controller ((Addr = 53)		
PTD08D210W (V_{OUT} A)	U7	Adjustable switching regulator dual 10A, 0.6Vto 3.6V	VCC_HP	1.8V
PTD08D210W (V_{OUT} B)		Adjustable switching regulator dual 10A, 0.6Vto 3.6V	VCC_HR	1.8V
UCD9248PFC(1)	U11	PMBus compliant digital PWM system controller (Address = 54)		
Utility switching regulators				
PTH12060W	U2	Adjustable switching regulator 10A, 1.2V to 5.5V	UTIL_5V0	5.0V
PTH12020W	U13	Adjustable switching regulator 18A, 1.2V to 5.5V	UTIL_3V3	3.3V
Linear regulators				
TL1963A	U47	Adjustable LDO Regulator 1.5A	UTIL_2V5	2.5V
TPS75925	U62	Fixed LDO regulator, 7.5A	VCCO_0	2.5V
ADP123	U21	Adjustable LDO Regulator, 300mA	VCC_1V2	1.2V
ADP123	U43	Adjustable LDO Regulator, 300mA	VCCADC_ADP	1.8V
REF3012	U45	Fixed LDO regulator, 25 mA	VREF_3012	1.25V

Notes:
1. The UCD9248PFC (U11) at Address 54 monitors MGTAVCC, MGTAVTT, and MGTVCCAUX rail voltage and current levels through the TI Fusion test application.

Using External Power Sources

The maximum output current rating for each power regulator is listed in Table 1-2. If a design exceeds this value on any core power rail, power for that rail must be supplied externally through the 12-position core power terminal block J6 (callout 7, Figure 1-2) using a supply capable of providing the required current.

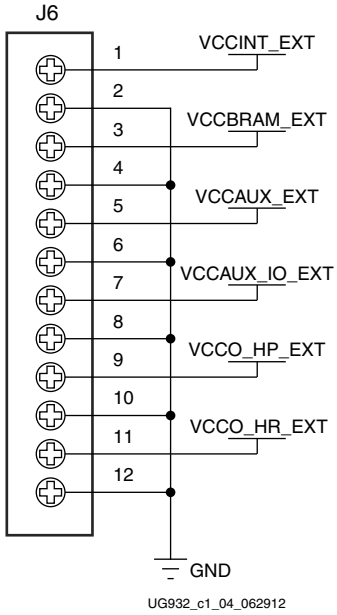


Figure 1-4: **Core Power Terminal Block**

Caution! The SW10 power regulator enable switch (callout 8, Figure 1-2) (see Disabling Onboard Power) must be set to the OFF position before turning ON the main power switch (SW1) and applying external power to the corresponding rail input pin on the core power terminal block J6 (callout 7, Figure 1-2).

Caution! The core power terminal block J6 has a maximum load current contact rating of 24A.

Disabling Onboard Power

Each core power regulator can be disabled through the 8-position regulator enable DIP switch, SW10 as shown in Figure 1-5. A switch in the ON position means the rail is supplied by an onboard regulator. Setting a switch in the opposite (OFF) position disables onboard power for that rail. SW10 is shown in Figure 1-2 as callout 8.

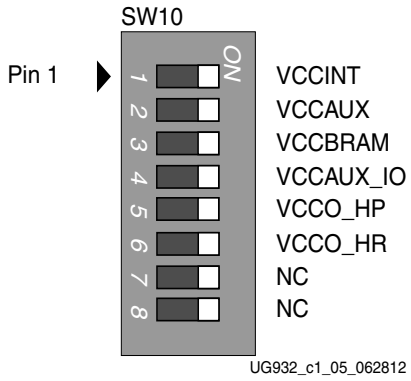


Figure 1-5: **Core Power Regulator Enable Switches**

Note: All onboard power can be disabled by placing a jumper across the TI PWR INH header J27 (callout 6, Figure 1-2). For the purposes of supplying external core power however, disabling onboard power through J27 would require the UTIL_5V0, UTIL_3V3 and UTIL_2V5 be supplied externally as well. The utility rails can be supplied through test points J58, J59 and J155, respectively.

Default Jumper and Switch Positions

A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper and Switch Positions.

Monitoring Voltage and Current

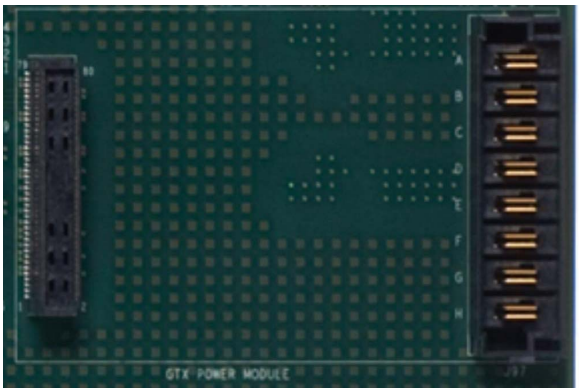
Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power graphical user interface (GUI). The three onboard TI power controllers (U9 at PMBUS address 52, U10 at PMBUS address 53, and U11 at PMBUS address 54) are wired to the same PMBus. The PMBus connector, J26 (callout 5, Figure 1-2), is provided for use with the TI USB Interface Adapter PMBus pod and associated TI GUI.

References

More information about the power system components used by the KC724 board are available from the Texas Instruments Digital Power website.

7 Series GTX Transceiver Power Module

The 7 series GTX transceiver power module (callout 9, Figure 1-2) supplies MGTAVCC, MGTAVTT, and MGTVCCAUX voltages to the FPGA GTX transceivers. Three 7 series GTX power modules from third-party vendors are provided with the KC724 board for evaluation. Any one of the three modules can be plugged into connectors J66 and J97 in the outlined and labeled power module location shown in Figure 1-6.



UG932_C1_05_062512

Figure 1-6: **Mounting Location, 7 Series GTX Transceiver Power Module**

Table 1-3 lists the nominal voltage values for the MGTAVCC, MGTAVTT and MGTVCCAUX power rails. It also lists the maximum current rating for each rail supplied by 7 series GTX modules included with the KC724 board.

Table 1-3: **7 Series GTX Transceiver Power Module**

Power Supply Rail Net Name	Nominal Voltage	Maximum Current Rating
MGTAVCC	1.05V	12A
MGTAVTT	1.2V	8A
MGTVCCAUX	1.8V	2.6A

The GTX transceiver power rails also have corresponding inputs on the GTX transceiver power terminal block J7 as shown in Figure 1-7 to supply each voltage independently from a bench-top power supply. J7 is shown in Figure 1-2 as callout 10.

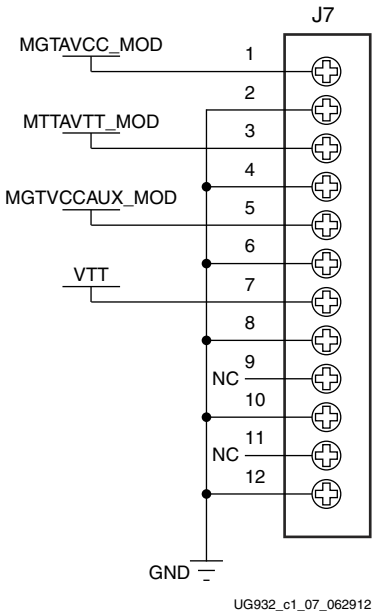


Figure 1-7: **GTX Transceiver Power Terminal Block**

Caution! The 7 series GTX Module **MUST** be removed when providing external power to the GTX transceiver rails.

Caution! The GTX transceiver power terminal block J7 has a maximum load current contact rating of 24A.

Information about the 7 series GTX power supply modules included with the KC724 kit is available from these vendor websites:

- Intersil
- Texas Instruments
- General Electric

Active Heatsink Power Connector

An active heatsink (Figure 1-8) is provided for the FPGA. A 12V fan is affixed to the heatsink and is powered from the 3-pin friction lock header J121 (Figure 1-9).

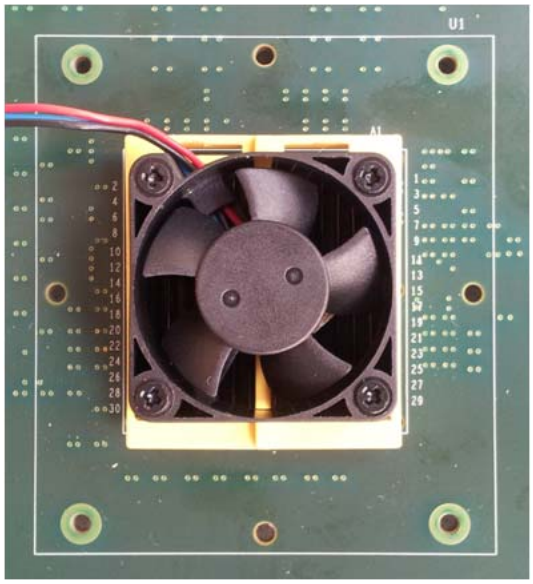


Figure 1-8: **Active FPGA Heatsink**

The fan power connections are detailed in Table 1-4:

Table 1-4: **Fan Power Connections**

Fan Wire	Header Pin
Black	J121.1 - GND
Red	J121.2 - 12V
Blue	J121.3 - NC

Figure 1-9 shows the heatsink fan power connector J121. J121 is shown in Figure 1-2 as callout 11.

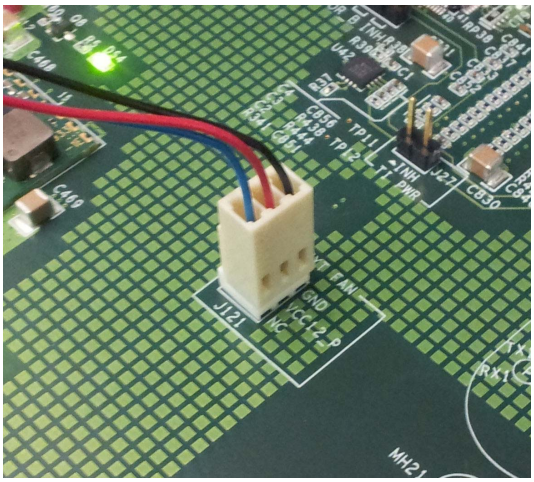


Figure 1-9: **Heatsink Fan Power Connector J121**

Kintex-7 FPGA

The KC724 board is populated with the Kintex-7 XC7K325T-3 FFG900E FPGA at U1 (callout 12, Figure 1-2). For further information on Kintex-7 FPGAs, see *7 Series FPGAs Overview* (DS180) [Ref 1].

FPGA Configuration

The FPGA is configured in JTAG mode only using one of the following options:

- USB JTAG configuration port (Digilent module)
- System ACE SD controller

The FPGA is configured through the Digilent onboard USB-to-JTAG configuration logic module (U8) where a host computer accesses the KC724 board JTAG chain through a standard-A plug to micro-B plug USB cable. (callout 13, Figure 1-2).

The FPGA is configured through the System ACE SD controller by setting the 4-bit configuration address DIP switch (SW8) to select one of eight bitstreams stored on a Secure Digital (SD) memory card (see System ACE SD Configuration Address DIP Switches, page 19).

The JTAG chain of the board is illustrated in Figure 1-10. By default only the Kintex-7 FPGA and the System ACE SD controller are part of the chain (J1 jumper OFF). Installing the J1 jumper adds the FMC interfaces as well.

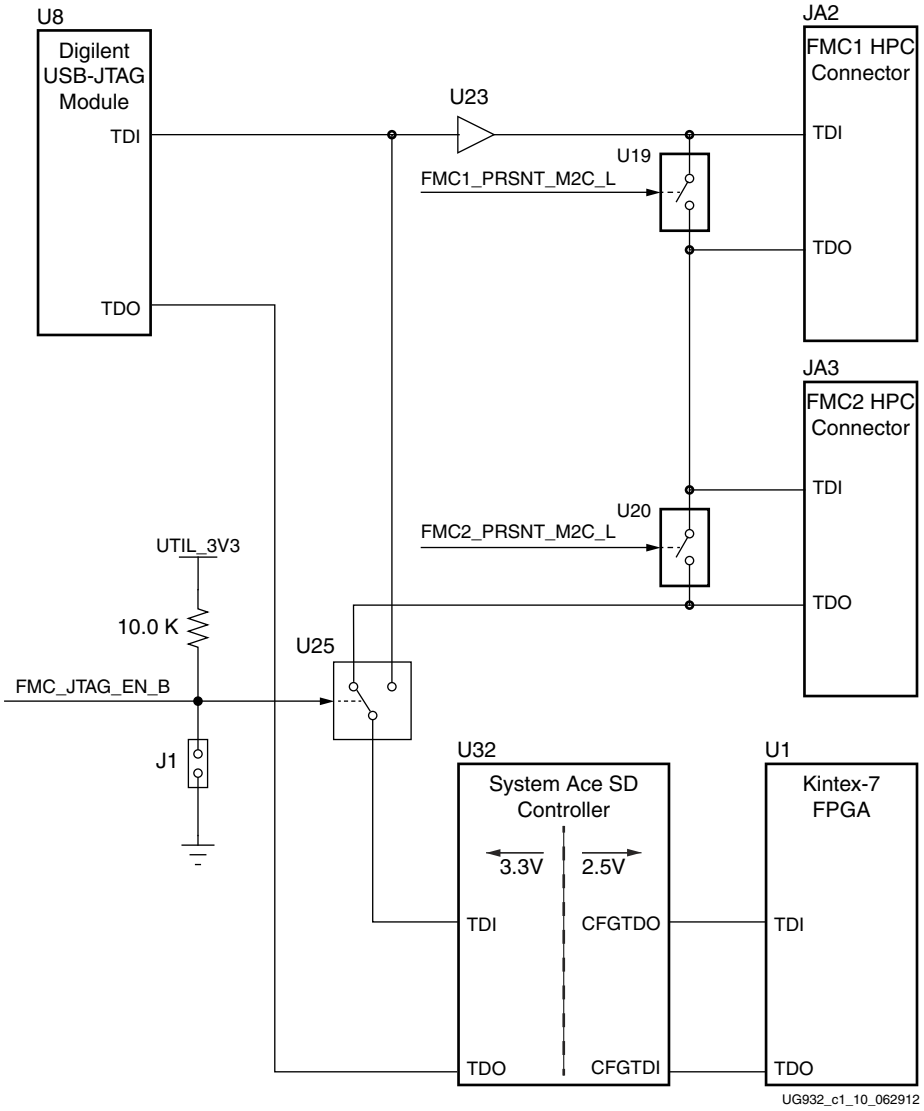


Figure 1-10: **JTAG Chain**

PROG_B Push Button

Pressing the PROG push button SW3 (callout 14, Figure 1-2) grounds the active-Low program pin of the FPGA.

DONE LED

The DONE LED DS21 (callout 15, Figure 1-2) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, DS21 lights indicating the FPGA is successfully configured.

INIT LED

The dual-color INIT LED DS25 (callout 16, Figure 1-2) indicates the FPGA's initialization status. During FPGA initialization the INIT LED illuminates RED. When FPGA initialization has completed the LED illuminates GREEN.

System ACE SD Controller

The onboard System ACE SD controller U32 (callout 17, Figure 1-2) allows storage of multiple configuration files on a Secure Digital (SD) card. These configuration files can be used to program the FPGA. The SD card connects to the SD card connector J8 located directly below the System ACE SD controller on the back side of the board.

System ACE SD Controller Reset

Pressing the SASD RESET push button SW7 (callout 18, Figure 1-2) resets the System ACE SD controller. The reset pin is an active-Low input.

System ACE SD Configuration Address DIP Switches

DIP switch SW8 shown in Figure 1-11 selects one of the eight configuration bitstream addresses in the SD memory card. A switch is in the ON position if set to the far right and in the OFF position if set to the far left. The MODE bit (switch position 4) is not used and can be set either ON or OFF. SW8 is shown in Figure 1-2 as callout 19.

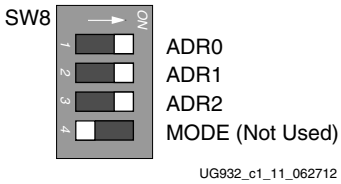


Figure 1-11: **Configuration Address DIP Switch (SW8)**

The switch settings for selecting each address are shown in Table 1-5.

Table 1-5: **SW8 DIP Switch Configuration**

Configuration Bitstream Address	ADR2	ADR1	ADR0
0	ON	ON	ON
1	ON	ON	OFF
2	ON	OFF	ON
3	ON	OFF	OFF
4	OFF	ON	ON
5	OFF	ON	OFF
6	OFF	OFF	ON
7	OFF	OFF	OFF

200 MHz 2.5V LVDS Oscillator

U35 (callout 20, Figure 1-2).

The KC724 board has one 200 MHz 2.5V LVDS oscillator (U35) connected to multi-region clock capable (MRCC) inputs on the FPGA. Table 1-6 lists the FPGA pin connections to the LVDS oscillator.

Table 1-6: **LVDS Oscillator MRCC Connections**

FPGA (U1)				Schematic Net Name	Device (U35)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
C25	SYSTEM CLOCK_P	Input	LVDS	LVDS_OSC_P	4	200 MHz LVDS oscillator	Output
B25	SYSTEM CLOCK_N	Input	LVDS	LVDS_OSC_N	5	201 MHz LVDS oscillator	Output

Differential SMA MRCC Pin Inputs

Callout 21, Figure 1-2.

The KC724 board provides two pairs of differential SMA transceiver clock inputs that can be used for connecting to an external function generator. The FPGA MRCC pins are connected to the SMA connectors as shown in Table 1-7.

Table 1-7: **Differential SMA Clock Connections**

FPGA (U1)				Schematic Net Name	SMA Connector
Pin	Function	Direction	IOSTANDARD		
AG29	USER CLOCK_1_P	Input	LVDS_25	CLK_DIFF_1_P	J99
AH29	USER CLOCK_1_N	Input	LVDS_25	CLK_DIFF_1_N	J100
D17	USER CLOCK_2_P	Input	LVDS_25	CLK_DIFF_2_P	J98
D18	USER CLOCK_2_N	Input	LVDS_25	CLK_DIFF_2_N	J101

SuperClock-2 Module

Callout 22, Figure 1-2.

The SuperClock-2 module connects to the clock module interface connector (J82) and provides a programmable, low-noise and low-jitter clock source for the KC724 board. The clock module maps to FPGA I/O by way of 24 control pins, 3 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-8 shows the FPGA I/O mapping for the SuperClock-2 module interface. The KC724 board also supplies UTIL_5V0, UTIL_3V3, UTIL_2V5 and VCCO_HR input power to the clock module interface.

Table 1-8: **SuperClock-2 FPGA I/O Mapping**

FPGA (U1)				Schematic Net Name	J82 Pin		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
F11	Clock recovery	Input	LVDS_25	CM_LVDS1_P	1	Clock recovery	Output
E11	Clock recovery	Input	LVDS_25	CM_LVDS1_N	3	Clock recovery	Output
C12	Clock recovery	Input	LVDS_25	CM_LVDS2_P	9	Clock recovery	Output

Table 1-8: **SuperClock-2 FPGA I/O Mapping *(Cont'd)***

FPGA (U1)				Schematic Net Name	J82 Pin		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
B12	Clock recovery	Input	LVDS_25	CM_LVDS2_N	11	Clock recovery	Output
AJ3	Clock recovery	Output	LVDS	CM_LVDS3_P	17	Clock recovery	Input
AK3	Clock recovery	Output	LVDS	CM_LVDS3_N	19	Clock recovery	Input
D26	Regional clock	Input	LVDS_25	CM_GCLK_P	25	Global clock	Output
C26	Regional clock	Input	LVDS_25	CM_GCLK_N	27	Global clock	Output
G30	Control I/O	In/Out	LVCMOS18	CM_CTRL_0	61	NC	–
H30	Control I/O	In/Out	LVCMOS18	CM_CTRL_1	63	NC	–
H27	Control I/O	In/Out	LVCMOS18	CM_CTRL_2	65	NC	–
H26	Control I/O	Output	LVCMOS18	CM_CTRL_3	67	DEC	Input
F30	Control I/O	Output	LVCMOS18	CM_CTRL_4	69	INC	Input
G29	Control I/O	Output	LVCMOS18	CM_CTRL_5	71	Align	Input
F27	Control I/O	In/Out	LVCMOS18	CM_CTRL_6	73	NC	–
G27	Control I/O	In/Out	LVCMOS18	CM_CTRL_7	75	NC	–
F28	Control I/O	In/Out	LVCMOS18	CM_CTRL_8	77	NC	–
G28	Control I/O	In/Out	LVCMOS18	CM_CTRL_9	79	LOL	
H25	Control I/O	Output	LVCMOS18	CM_CTRL_10	81	INT_ALRM	Input
H24	Control I/O	Output	LVCMOS18	CM_CTRL_11	83	C1B	Input
E30	Control I/O	Output	LVCMOS18	CM_CTRL_12	85	C2B	Input
E29	Control I/O	Output	LVCMOS18	CM_CTRL_13	87	C3B	Input
A30	Control I/O	Output	LVCMOS18	CM_CTRL_14	89	C1A	Input
B30	Control I/O	Output	LVCMOS18	CM_CTRL_15	91	C2A	Input
C30	Control I/O	In/Out	LVCMOS18	CM_CTRL_16	93	NC	–
D29	Control I/O	Output	LVCMOS18	CM_CTRL_17	95	CS0_C3A	Input
B29	Control I/O	Output	LVCMOS18	CM_CTRL_18	97	CS1_C4A	Input
C29	Control I/O	In/Out	LVCMOS18	CM_CTRL_19	99	NC	–
A26	Control I/O	In/Out	LVCMOS18	CM_CTRL_20	101	NC	–
A25	Control I/O	In/Out	LVCMOS18	CM_CTRL_21	103	NC	–
A28	Control I/O	In/Out	LVCMOS18	CM_CTRL_22	105	NC	–
B28	Control I/O	In/Out	LVCMOS18	CM_CTRL_23	107	NC	–
B24	CM_RESET	Output	LVCMOS18	CM_RST	66	RESET_B	Input

User LEDs (Active High)

Callout 23, Figure 1-2.

DS13 through DS20 are eight active-High LEDs that are connected to user I/O pins on the FPGA as shown in Table 1-10 These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-9: **User LEDs**

FPGA (U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	IOSTANDARD		
A20	User LED	Output	LVCMOS18	APP_LED1	DS19
A17	User LED	Output	LVCMOS18	APP_LED2	DS20
A16	User LED	Output	LVCMOS18	APP_LED3	DS17
B20	User LED	Output	LVCMOS18	APP_LED4	DS18
C20	User LED	Output	LVCMOS18	APP_LED5	DS16
F17	User LED	Output	LVCMOS18	APP_LED6	DS15
G17	User LED	Output	LVCMOS18	APP_LED7	DS13
B17	User LED	Output	LVCMOS18	APP_LED8	DS14

User DIP Switches (Active High)

Callout 24, Figure 1-2.

The DIP switch SW2 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-10. These pins can be used to set control pins or any other purpose. Six of the eight I/Os also map to 2 x 6 test header J125 providing external access for these pins (callout 25, Figure 1-2.).

Table 1-10: **User DIP Switches**

FPGA (U1)				Schematic Net Name	DIP Switch Reference	J125 Test Header Pin
Pin	Function	Direction	IOSTANDARD			
E18	User switch	Input	LVCMOS18	USER_SW1	SW2	2
B19	User switch	Input	LVCMOS18	USER_SW2		4
C19	User switch	Input	LVCMOS18	USER_SW3		6
A22	User switch	Input	LVCMOS18	USER_SW4		8
B22	User switch	Input	LVCMOS18	USER_SW5		10
A18	User switch	Input	LVCMOS18	USER_SW6		12
B18	User switch	Input	LVCMOS18	USER_SW7		–
A21	User switch	Input	LVCMOS18	USER_SW8		–

Figure 1-12 Shows the user test I/O connector J125.

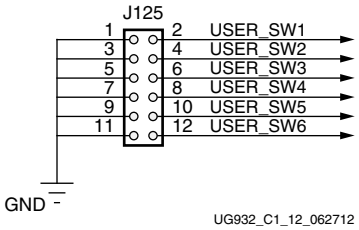


Figure 1-12: **User Test I/O**

User Push Buttons (Active High)

Callout 26, Figure 1-2.

SW4 and SW5 are active-High user push buttons that are connected to user I/O pins on the FPGA as shown in Table 1-11. These switches can be used for any purpose.

Table 1-11: **User Push Buttons**

FPGA (U1)				Schematict Net Name	Reference Designator
Pin	Function	Direction	IOSTANDARD		
K18	User push button	Input	LVCMOS18	USER_PB1	SW5
G19	User push button	Input	LVCMOS18	USER_PB2	SW4

GTX Transceivers and Reference Clocks

Callout 27, Figure 1-2.

The KC724 board provides access to all GTX transceiver and reference clock pins on the FPGA as shown in Figure 1-13. The GTX transceivers are grouped into four sets of four RX-TX *lanes*. Four lanes are referred to as a *Quad*.

Note: Figure 1-13 is for reference only and might not reflect the current revision of the board.

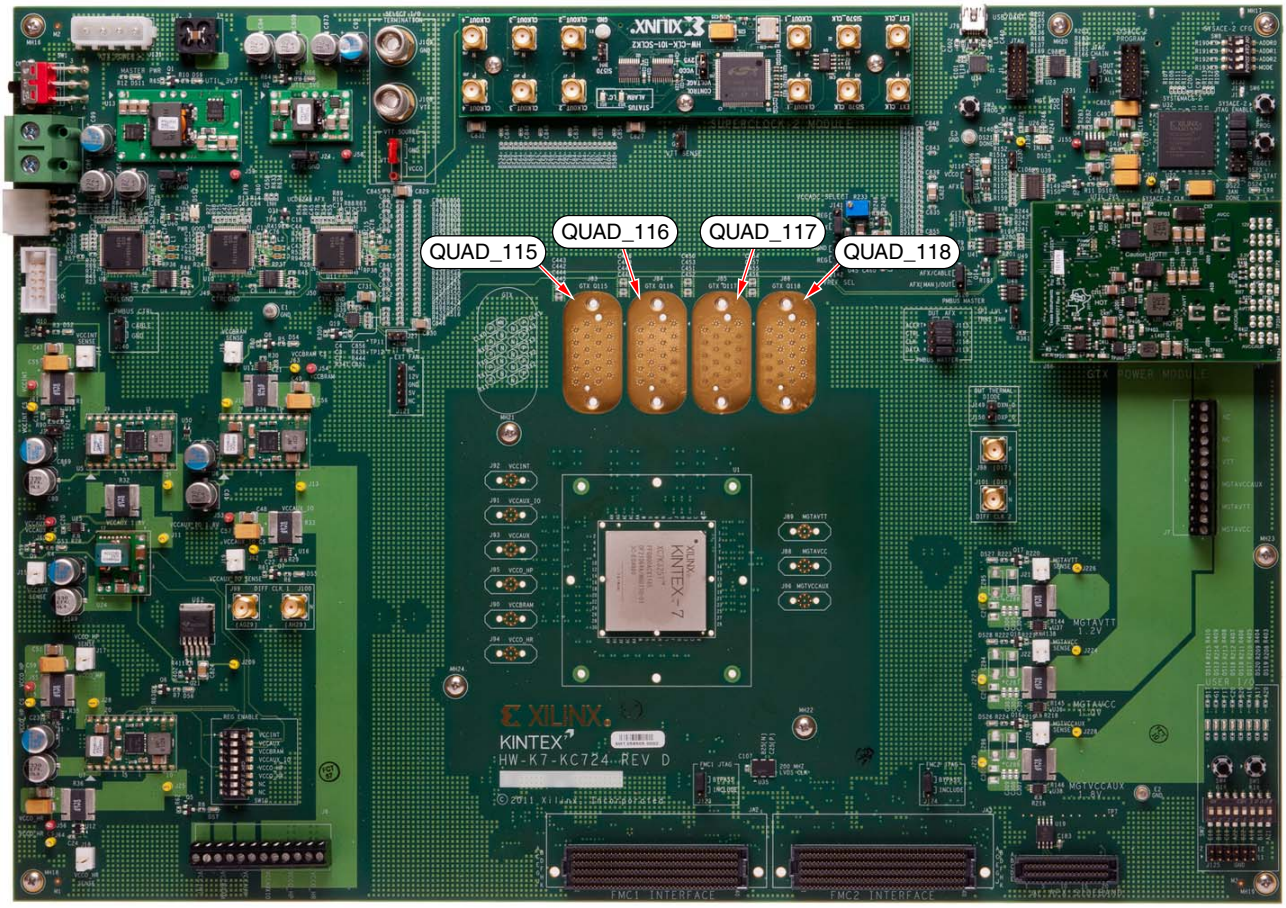


Figure 1-13: **GTX Quad Locations**

Each GTX Quad and its associated reference clocks (CLK0 and CLK1) are brought out to a connector pad which interfaces with Samtec BullsEye connectors used with the Samtec HDR-155805-01-BEYE cable assembly. Contact Samtec, Inc. for information about this or other cable assemblies. Figure 1-14 *A* shows the connector pad. Figure 1-14 *B* shows the connector pinout.

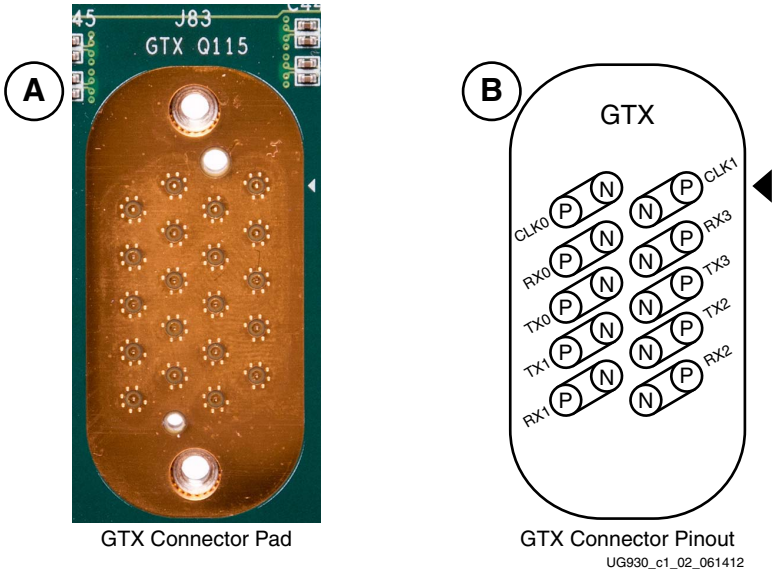


Figure 1-14: **A – GTX Connector Pad. B – GTX Connector Pinout**

Information for each GTX transceiver pin is shown in Table 1-12.

Table 1-12: **GTX Transceiver Pins**

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
Y2	115_TX0_P	115	J83	2,805
Y1	115_TX0_N	115	J83	2,806
AA4	115_RX0_P	115	J83	2,898
AA3	115_RX0_N	115	J83	2,898
V2	115_TX1_P	115	J83	2,525
V1	115_TX1_N	115	J83	2,523
Y6	115_RX1_P	115	J83	2,489
Y5	115_RX1_N	115	J83	2,489
U4	115_TX2_P	115	J83	2,549
U3	115_TX2_N	115	J83	2,549
W4	115_RX2_P	115	J83	2,308
W3	115_RX2_N	115	J83	2,309
T2	115_TX3_P	115	J83	2,840
T1	115_TX3_N	115	J83	2,840