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SP623 Spartan-6 FPGA GTP Transceiver Characterization Board

User Guide

UG751 (v1.1) September 15, 2010

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/22/10	1.0	Initial Xilinx release.
09/15/10	1.1	Added information about the Intersil power module to the paragraphs under GTP Transceiver Power Module, page 13, and to Table 1-2. Removed spaces between net names and associated closing quote marks in the SP623 Master UCF Listing, page 39.

Table of Contents

About This Guide

This document describes the basic setup, features, and operation of the SP623 Spartan-6® FPGA GTP transceiver characterization board. The SP623 board provides the hardware environment for characterizing and evaluating the GTP transceivers available on the Spartan-6 XC6SLX150T-3FGG676 FPGA.

Guide Contents

This user guide contains the following chapters and appendices:

- Chapter 1, SP623 Board Features and Operation describes the components, features, and operation of the SP623 Spartan-6 FPGA GTP transceiver characterization board.
- Appendix A, Default Jumper Positions lists the jumpers that must be installed on the board for proper operation.
- Appendix B, VITA 57.1 FMC HPC Connector Pinout provides a pinout reference for the FPGA mezzanine card (FMC) connector.
- Appendix C, SP623 Master UCF Listing provides a listing of the SP623 master user constraints file (UCF).
- Appendix D, References provides a list of references and links to related documentation.

To find additional documentation, see the Xilinx website at:

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This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *Command Line Tools User Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

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Chapter 1

SP623 Board Features and Operation

This chapter describes the components, features, and operation of the SP623 Spartan®-6 FPGA GTP transceiver characterization board. The SP623 board provides the hardware environment for characterizing and evaluating the GTP transceivers available on the Spartan-6 XC6SLX150T-3FGG676 FPGA.

SP623 Board Features

- Spartan-6 XC6SLX150T-3FGG676 FPGA
- On-board power supplies for all necessary voltages
- Power supply jacks for optional use of external power supplies
- JTAG configuration port for use with Platform Cable USB or Parallel Cable III/IV cables
- System ACE™ controller
- Power module supporting all Spartan-6 FPGA GTP transceiver power requirements
- A fixed, 200 MHz 2.5V LVDS oscillator wired to global clock inputs
- One pair of global clock inputs with SMA connectors
- SuperClock-2 module supporting multiple frequencies
- 16 pairs of SMA connectors for the GTP transceivers
- 8 pairs of SMA connectors for GTP transceiver clock inputs
- Power status LEDs
- General purpose DIP switches, LEDs, push buttons, and test I/O
- Two VITA 57.1 FMC HPC connectors
- USB to UART bridge
- I^2C Bus

The SP623 board block diagram is shown in Figure 1-1.

Caution! The SP623 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

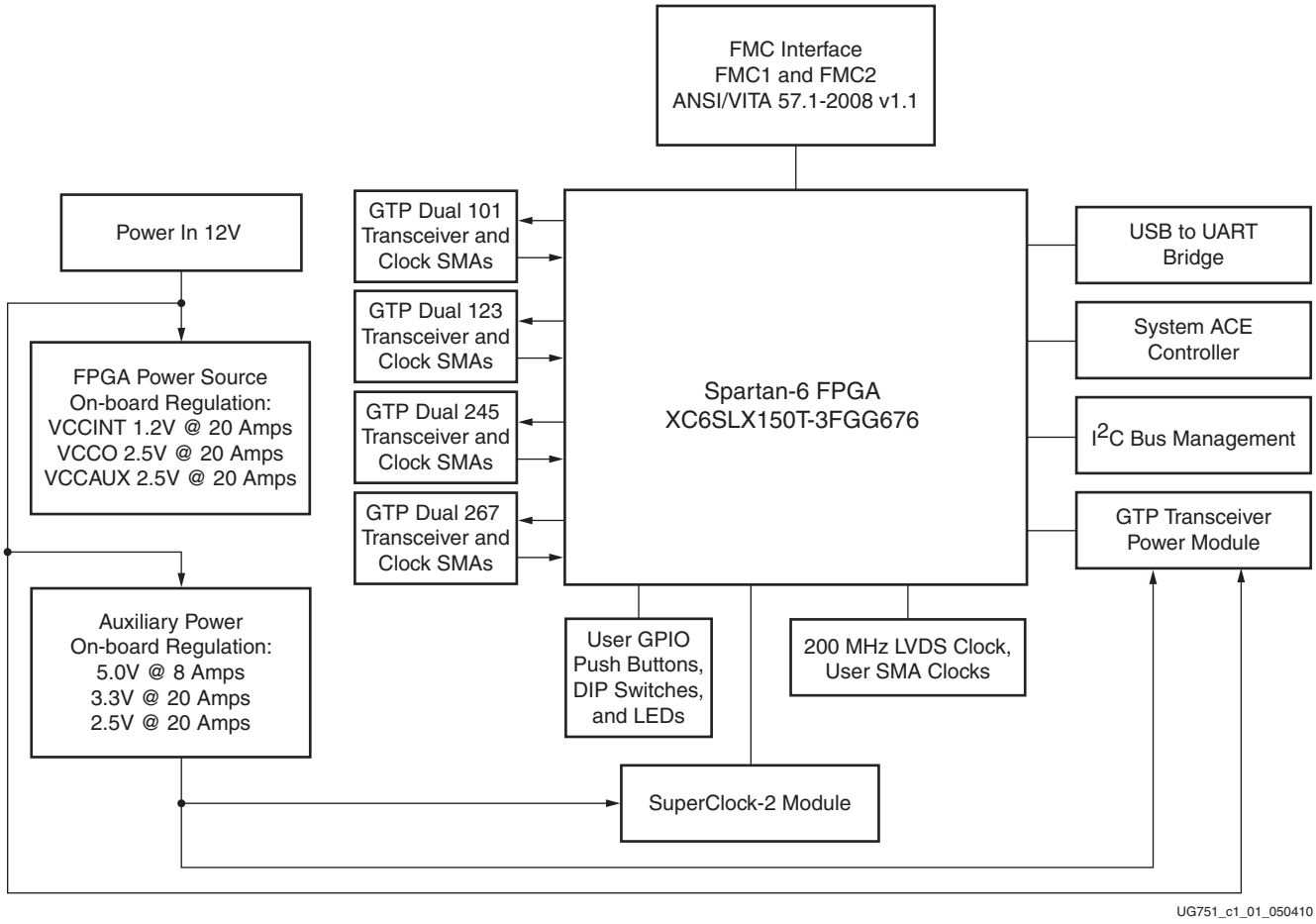
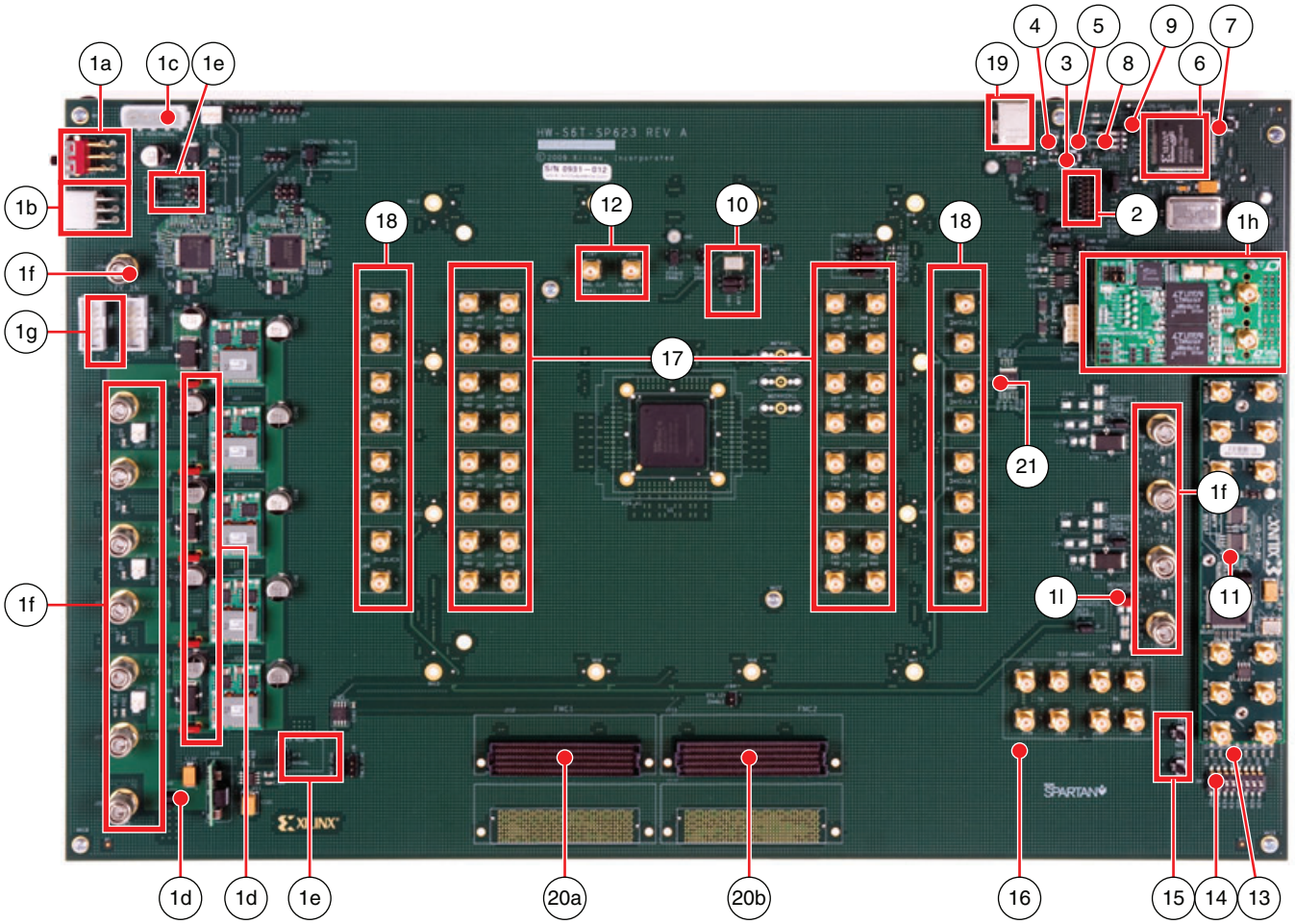


Figure 1-1: **SP623 Board Block Diagram**

Detailed Description

Figure 1-2 shows the SP623 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

Note: The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.



1a	Main power switch (SW1)	8	Configuration address DIP switch (SW3)
1b	12V mini-fit connector (J122)	9	JTAG isolation jumpers (J22, J23, J195, J196)
1c	12V ATX connector (J141)	10	200 MHz 2.5V LVDS oscillator (U7)
1d	Power regulation jumpers (J30, J31, J33, J102, J104,J105)	11	SuperClock-2 module
1e	Regulation inhibit (J14, J19)	12	User SMA global clock inputs (J167, J168)
1f	External power supply jacks	13	User LEDs, active-High (DS10 - DS17)
1g	TI PMBus connector (J6)	14	User DIP switches, active-High (SW1 - SW8)
1h	GTP transceiver power supply module	15	User push buttons, active-High (SW4, SW6)
1i	MGTAVCCPLL isolation jumper (J3)	16	User test I/O (J44)
2	FPGA configuration connector (J1)	17	GTP transceiver pins
3	PROG push button, active-Low (SW5)	18	GTP transceiver clock input SMAs
4	DONE LED (DS6)	19	USB to UART bridge (U26)
5	INIT LED (DS20)	20a	FMC1 (J112)
6	System ACE controller (U25)	20b	FMC2 (J113)
7	System ACE reset, active-Low (SW2)	21	I2C bus management (U14)

UG751_c1_02_041310

Figure 1-2: **Detailed Description of SP623 Board Components**

Power Management

Numbers 1a through 1i refer to the callouts in Figure 1-2:

1a: Main power switch (SW1)

1b: 12V mini-fit connector (J122)

1c: 12V ATX connector (J141)

1d: Power regulation jumpers (J30, J31, J33, J102, J104, J105)

1e: Regulation inhibit (J14, J19)

1f: External power supply jacks (J5, J98, J173, J174, J175, J177, J178, J189, J220, J223, J227, J234)

1g: TI PMBus cable connector (J6)

1h: GTP power supply module

1i: MGTAVCCPLL isolation jumper (J3)

Board Power and Switch

The SP623 board is powered through J122 using the 12V AC adapter included with the board. J122 is a 6-pin (2 x 3) right angle Mini-Fit type connector.

Power can also be provided through:

- Connector J141 which accepts an ATX hard disk 4-pin power plug
- Jack J234 which can be used to connect to a bench-top power supply

Caution! Do NOT plug a PC ATX power supply 6-pin connector into J122 on the SP623 board. The ATX 6-pin connector has a different pinout than J122. Connecting an ATX 6-pin connector into J122 will damage the SP623 board and void the board warranty.

Caution! Do NOT apply power to J122 and connectors J141 and/or J234 at the same time. Doing so will damage the SP623 board.

The SP623 board power is turned on or off by switch SW1. When the switch is in the ON position, power is applied to the board and a green LED (DS36) illuminates.

Onboard Power Regulation

Figure 1-3 shows the on-board power supply architecture.

Note: Power regulation jumpers are not shown in Figure 1-3.

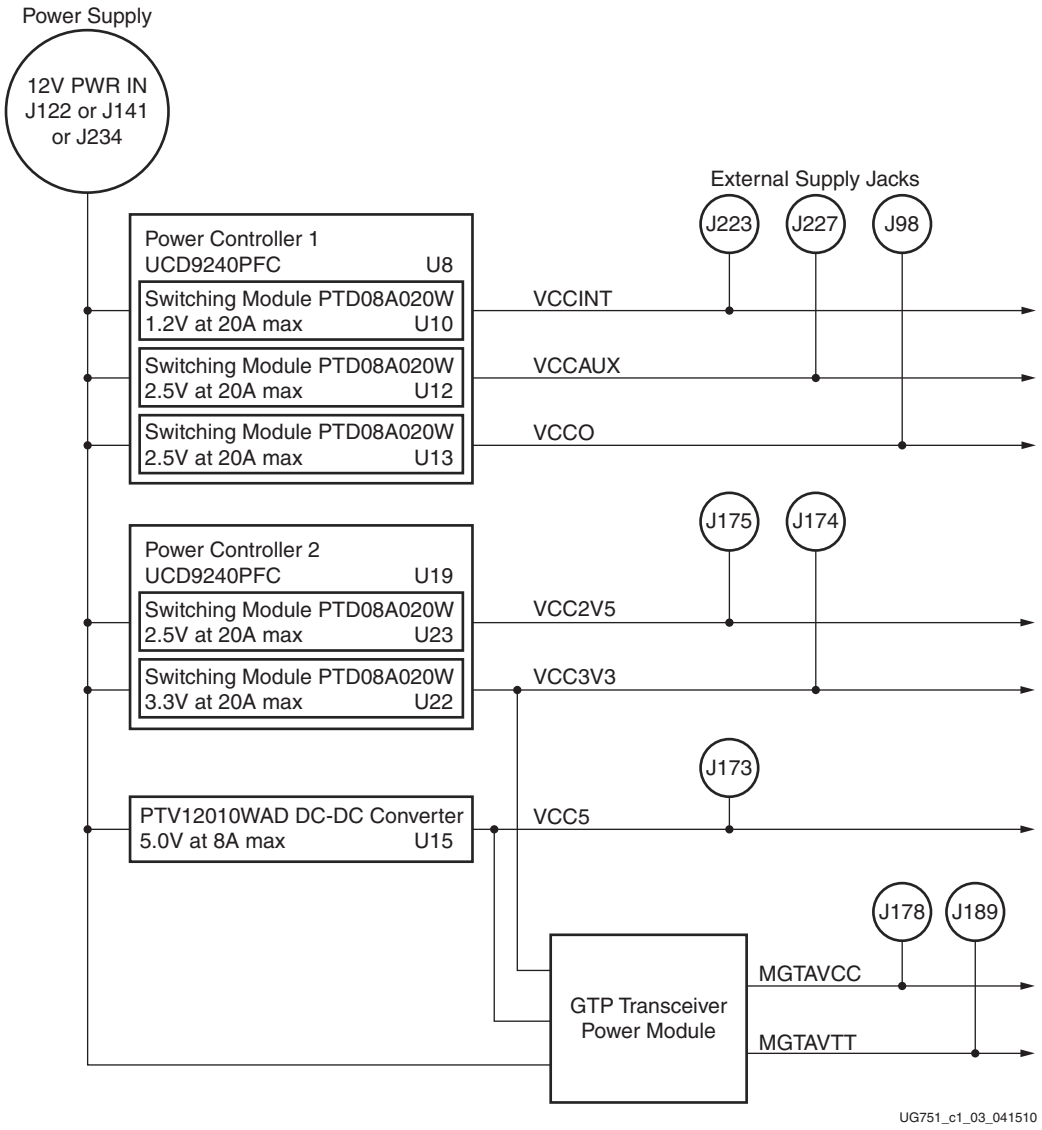


Figure 1-3: **SP623 Board Power Supply Block Diagram**

The SP623 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the core and auxiliary voltages listed in Table 1-1. The board can also be configured to use external bench power supply for each voltage. See Using External Power Sources.

Table 1-1: **Onboard Power System Devices**

Device	Reference Designator	Description	Power Rail Net Name	Typical Voltage	Power Regulation Jumper	External Supply Jack
Core voltage controller and regulators						
UCD9240PFC	U8	PMBus compliant digital PWM system controller (address = 52)				
PTD08A020W	U10	Adjustable switching regulator 20A, 0.6V to 3.6V	VCCINT	1.2V	J102	J223
PTD08A020W	U12	Adjustable switching regulator 20A, 0.6Vto 3.6V	VCCAUX	2.5V	J104	J227
PTD08A020W	U13	Adjustable switching regulator 20A, 0.6V to 3.6V	VCCO	2.5V	J105	J98
Auxiliary voltage controller and regulators						
UCD9240PFC	U19	PMBus compliant digital PWM system controller (address = 53)				
PTD08A020W	U23	Adjustable switching regulator 20A, 0.6V to 3.6V	VCC2V5	2.5V	J31	J175
PTD08A020W	U22	Adjustable switching regulator 20A, 0.6V to 3.6V	VCC3V3	3.3V	J30	J174
5V auxiliary power						
PTV12010WAD	U15	Adjustable switching regulator 8A, 1.2V to 5.5V	VCC5	5.0V	J33	J173

Using External Power Sources

The maximum output current rating for each power regulator is listed in Table 1-1. If a design exceeds this value on any power rail, power for that rail must be supplied through the external power jack using a supply capable of providing the required current.

Each power rail has a corresponding jack and jumper that is used to supply voltage to the rail using an external power supply. The jack, jumper, and regulator for each power rail is listed in Table 1-1.

> ***Caution!*** The power regulation jumper must be removed before applying external power to the power rail through its corresponding supply jack.

Disabling Onboard Power

Voltage regulators U10, U12, U13, U22, and U23 are disabled by installing a jumper across pins 2–3 of header J14. Voltage regulator U15 is disabled by installing a jumper across pins 2–3 of header J19.

Default Jumper Positions

A list of shunts and shorting plugs and their required positions for normal board operation is provided in Appendix A, Default Jumper Positions.

Monitoring Voltage and Current

Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power graphical user interface (GUI). Both onboard TI power controllers are wired to the same PMBus. The PMBus connector, J6, is provided for use with the TI USB Interface Adapter PMBus pod and associated TI GUI.

References

More information about the power system components used by the SP623 board are available from the Texas Instruments digital power website at:

http://www.ti.com/ww/en/analog/digital-power/index.html

GTP Transceiver Power Module

The GTP transceiver power module supplies MGTAVCC and MGTAVTT voltages to the FPGA GTP transceivers. Three power modules are provided with the SP623 board. Any one of the three modules can be plugged into connectors J34 and J179 in the outlined and labeled power module location shown in Figure 1-4.

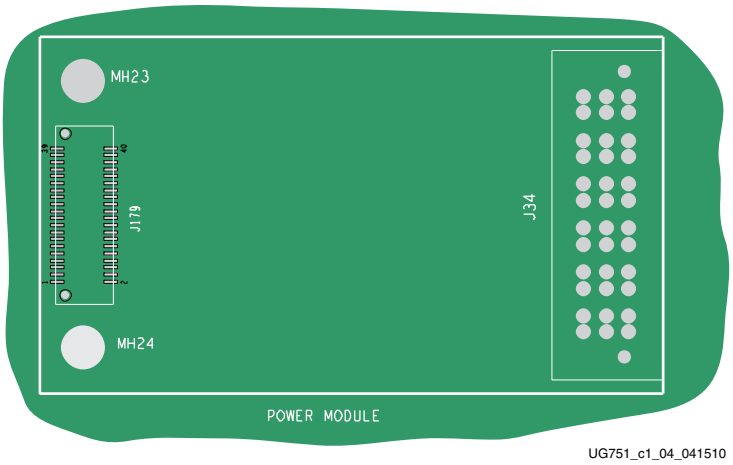


Figure 1-4: **Mounting Location, GTP Transceiver Power Module**

Table 1-2 describes the nominal voltage values for the MGTAVCC and MGTAVTT power rails. It also lists the maximum current ratings for each rail supplied by either module included with the SP623 board.

Table 1-2: **GTP Transceiver Power Module**

Power Supply Rail Net Name	Typical Voltage	Maximum Current Rating			Regulation Jumper			External Supply Jack
		Linear Technology Module	Texas Instruments Module	Intersil Module	Linear Technology Module	Texas Instruments Module	Intersil Module	
MGTAVCC	1.2V	16A	8A	8A	JP1	N/A	N/A	J178
MGTAVTT	1.2V	12A	6A	6A	JP2	N/A	N/A	J189

The GTP transceiver power rails also have corresponding input voltage jacks to supply each voltage independently from a bench-top power supply (See External Supply Jack column in Table 1-2). To supply power externally to one or both rails when the

Linear Technology Module is installed, place jumpers on JP1 and/or JP2 across pins 2–3 (OFF position).

Note: The power regulation jumper must be placed in the OFF position before connecting an external supply to its corresponding supply jack.

The Texas Instruments and Intersil modules do not have voltage regulation jumpers and *must* be removed from the board before providing external power to the GTP transceiver rails.

Note: The Intersil module features an MGTAVCC voltage adjust header, J1. Verify that a jumper is connected across J1 before powering the board with the Intersil module installed. Failure to do so may prevent your design from running properly.

MGTAVCCPLL Rail

The GTP transceiver power module also supplies the MGTAVCCPLL rail through the J3 shorting plug (Figure 1-5). This jumper connects MGTAVCC and MGTAVCCPLL rails by default. The MGTAVCCPLL rail can also be supplied from an external 1.2V (nominal) power supply by removing the J3 shorting plug and then connecting the power supply output to J5.

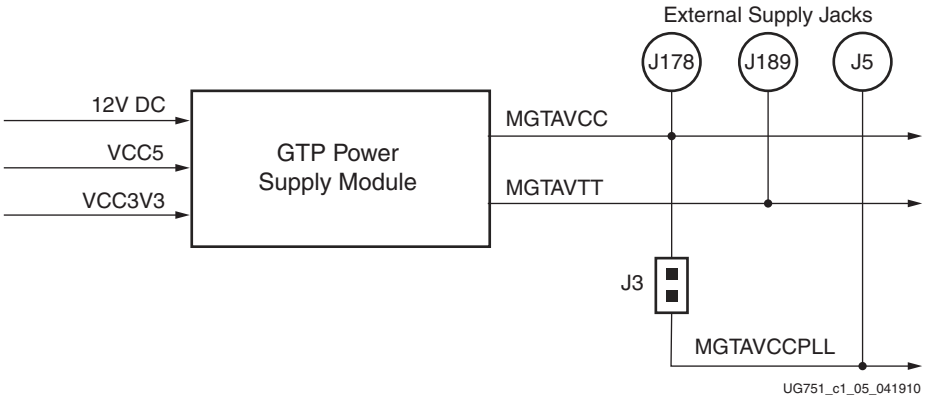


Figure 1-5: **MGTAVCCPLL Isolation Jumper**

FPGA Configuration

[Figure 1-2, callout 2]

The FPGA is configured in JTAG mode only using one of the following options:

- Platform Cable USB
- Parallel Cable IV
- Parallel Cable III
- System ACE controller

Detailed information on the System ACE controller is available in DS080, *System ACE CompactFlash Solution*.

The FPGA is configured through one of the aforementioned cables by connecting the cable to the download cable connector, J1.

The FPGA is configured through the System ACE controller by setting the 3-bit configuration address DIP switches (SW3) to select one of eight bitstreams stored on a CompactFlash memory card (see Configuration Address DIP Switches, page 16).

Note: The System ACE controller is bypassed when the flying wire leads or the Parallel Cable IV cable is used, causing no disruption in the JTAG chain.

The JTAG chain of the board is illustrated in Figure 1-6 (the four System ACE interface isolation jumpers described in JTAG Isolation Jumpers are not shown). Shorting pins 1–2 on header J162 automatically bypasses the FMC modules and the GTP transceiver power supply module in the chain.

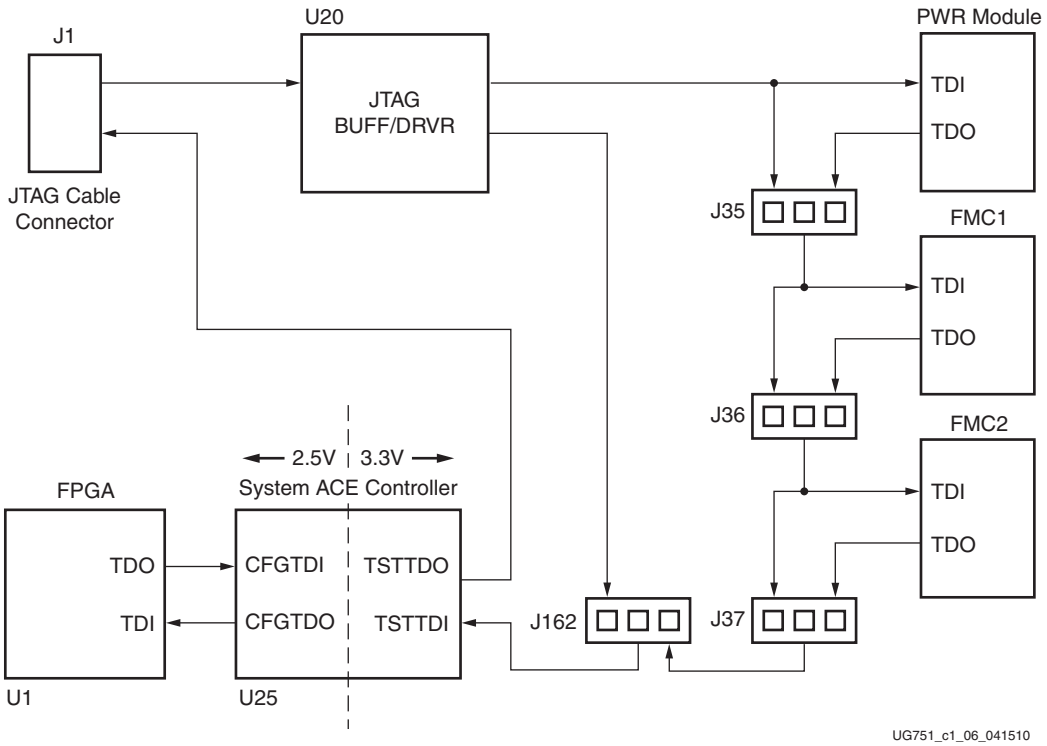


Figure 1-6: **JTAG Chain**

PROG Push Button

[Figure 1-2, callout 3]

Pressing the PROG push button (SW5) grounds the active-Low program pin of the FPGA.

DONE LED

[Figure 1-2, callout 4]

The DONE LED (DS6) indicates the status of the DONE pin of the FPGA. When the DONE pin is high, DS6 lights indicating the FPGA is successfully configured.

INIT LED

[Figure 1-2, callout 5]

The INIT LED (DS20) lights during FPGA initialization.

System ACE Controller

[Figure 1-2, callout 6]

The onboard System ACE controller (U25) allows storage of multiple configuration files on a CompactFlash card. These configuration files can be used to program the FPGA. The CompactFlash card connects to the CompactFlash card connector (U24) located directly below the System ACE controller on the back-side of the board.

System ACE Controller Reset

[Figure 1-2, callout 7]

Pressing push button SW2 (RESET) resets the System ACE controller. Reset is an active-Low input.

Configuration Address DIP Switches

[Figure 1-2, callout 8]

DIP switch SW3 selects one of the eight configuration bitstream addresses in the CompactFlash memory card. The switch settings for selecting each address are identified in Table 1-3.

Table 1-3: **SW3 DIP Switch Configuration**

Address	ADR2	ADR1	ADR0
0	O(1)	O	O
1	O	O	C(2)
2	O	C	O
3	O	C	C
4	C	O	O
5	C	O	C
6	C	C	O
7	C	C	C

Notes:

1. O indicates the open switch position (logic 0).
2. C indicates the closed switch position (logic 1).

JTAG Isolation Jumpers

[Figure 1-2, callout 9]

The group of four 2-pin headers shown in Figure 1-7 provide the option to isolate the FPGA JTAG interface from the System ACE controller by removing the shunts from all four headers. The FPGA JTAG interface can also be driven directly from these headers by attaching the flying wire JTAG cable to pin 2 of each header. Figure 1-7 shows a more detailed representation of the isolation jumpers as part of the broader JTAG chain in Figure 1-6.

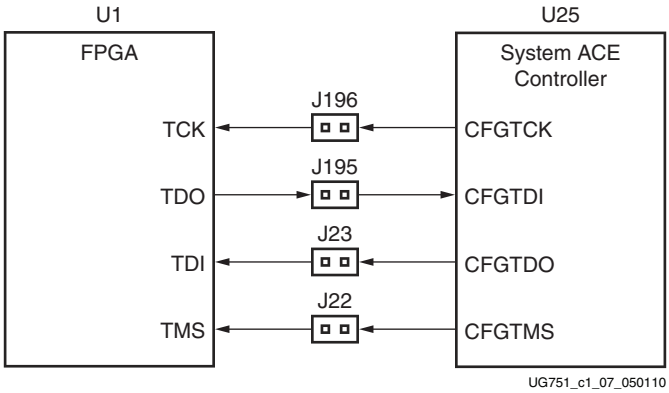


Figure 1-7: **JTAG Isolation Jumpers**

Table 1-4 indicates the FPGA pin name associated with each jumper.

Table 1-4: **JTAG Isolation Jumpers**

Reference Designator	FPGA Pin Name
J22	TMS
J23	TDI
J195	TDO
J196	TCK

200 MHz 2.5V LVDS Oscillator

[Figure 1-2, callout 10]

The SP623 board has one 2.5V LVDS differential 200 MHz oscillator (U7) connected to the FPGA global clock inputs. Table 1-5 lists the FPGA pin connections to the LVDS oscillator. The 200 MHz differential clock is enabled by placing two shunts (P, N) across J188 header pins 1–3 and 2–4 (LVDS).

Table 1-5: **LVDS Oscillator Global Clock Connections**

FPGA Pin	Net Name	U7 Pin
V23	IO_LVDS_CLK_P	4
W24	IO_LVDS_CLK_N	5

SuperClock-2 Module

[Figure 1-2, callout 11]

The SuperClock-2 module connects to the clock module interface connector (J32) and provides a programmable, low-noise clock source for the SP623 board. The clock module maps to FPGA I/O by way of 24 control pins, 3 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-6 shows the FPGA I/O mapping for the SuperClock-2 module interface. The SP623 board also supplies VCC5, VCC3V3, VCC2V5, and VCCO input power to the clock module interface.

Table 1-6: **SuperClock-2 FPGA I/O Mapping**

FPGA Pin	Net Name	J32 Pin
F12	CM_LVDS1_P	1
E12	CM_LVDS1_N	3
V12	CM_LVDS2_P	9
W12	CM_LVDS2_N	11
G12	CM_LVDS3_P	17
F11	CM_LVDS3_N	19
U25	CM_GCLK_P	25
U26	CM_GCLK_N	27
U20	CM_CTRL_0	61
U19	CM_CTRL_1	63
AA24	CM_CTRL_2	65
AA23	CM_CTRL_3	67
T20	CM_CTRL_4	69
T19	CM_CTRL_5	71
U22	CM_CTRL_6	73
U21	CM_CTRL_7	75
AE26	CM_CTRL_8	77
AE25	CM_CTRL_9	79
Y26	CM_CTRL_10	81
Y24	CM_CTRL_11	83
AC26	CM_CTRL_12	85
AC25	CM_CTRL_13	87
AB26	CM_CTRL_14	89
AB24	CM_CTRL_15	91
AD26	CM_CTRL_16	93
AD24	CM_CTRL_17	95
AA26	CM_CTRL_18	97
AA25	CM_CTRL_19	99
W26	CM_CTRL_20	101
W25	CM_CTRL_21	103
V24	CM_CTRL_22	105
T23	CM_CTRL_23	107
T22	CM_RST	66

User SMA Global Clock Inputs

[Figure 1-2, callout 12]

The SP623 board provides two single-ended clock input SMAs that can be used for connecting to an external function generator. These clock inputs can alternatively be used as a differential pair. The FPGA clock pins are connected to the SMAs as shown in Table 1-7.

Note: Jumpers should NOT be installed on AFX SEL headers J99 and J100 if these clock inputs are used.

Table 1-7: **SMA Clock Input Connections**

FPGA Pin	Net Name	SMA Connector
R25	SMA_CLK_P	J167
R26	SMA_CLK_N	J168

User LEDs (Active High)

[Figure 1-2, callout 13]

DS10 through DS17 are eight active-High LEDs that are connected to user I/O on the FPGA as shown in Table 1-8. These LEDs can be used to indicate status, or any other purpose determined by the user.

Table 1-8: **User LEDs**

FPGA Pin	Net Name	Reference Designator
L21	LED1	DS17
L20	LED2	DS16
M23	LED3	DS15
M21	LED4	DS14
N26	LED5	DS13
N25	LED6	DS12
L26	LED7	DS11
L25	LED8	DS10

User DIP Switches (Active High)

[Figure 1-2, callout 14]

DIP switch SW7 provides a set of eight active-High switches that connect to user I/O on the FPGA, as shown in Table 1-9. These pins can be used to set control pins, or other functions determined by the user.

Table 1-9: **User DIP Switches**

FPGA Pin	Net Name	Reference Designator
J26	SW1	SW7
J25	SW2	
K26	SW3	
K24	SW4	
G26	SW5	
G25	SW6	
H26	SW7	
H24	SW8	

User Push Buttons (Active High)

[Figure 1-2, callout 15]

SW5 and SW6 are active-High user push buttons that are connected to user I/O pins on the FPGA, as identified in Table 1-10. These switches can be used for any purpose determined by the user.

Table 1-10: **User Push Buttons**

FPGA Pin	Net Name	Reference Designator
M26	PB_SW1	SW6
M24	PB_SW2	SW4

User Test I/O

[Figure 1-2, callout 16]

A standard 2 x 6, 100-mil pitch header (J44) brings out 6 FPGA I/O for test purposes. Table 1-11 lists these pins.

Table 1-11: **User Test I/O**

FPGA Pin	Net Name	J44 Pin
U1	IO_L40N_M3DQ7_3_U1	2
U2	IO_L40P_M3DQ6_3_U2	4
V1	IO_L39N_M3LDQSN_3_V1	6
V3	IO_L39P_M3LDQS_3_V3	8
AA13	IO_L36N_2_AA13	10
AB13	IO_L36P_2_AB13	12

GTP Transceiver Pins

[Figure 1-2, callout 17]

All FPGA GTP transceiver pins are connected to differential SMA connector pairs. The GTP transceivers are grouped into four sets of two (referred to as *Duals*) which share two differential reference clock pin-pairs (Figure 1-8). The transceiver pins and their corresponding SMA connector are identified in Table 1-12.

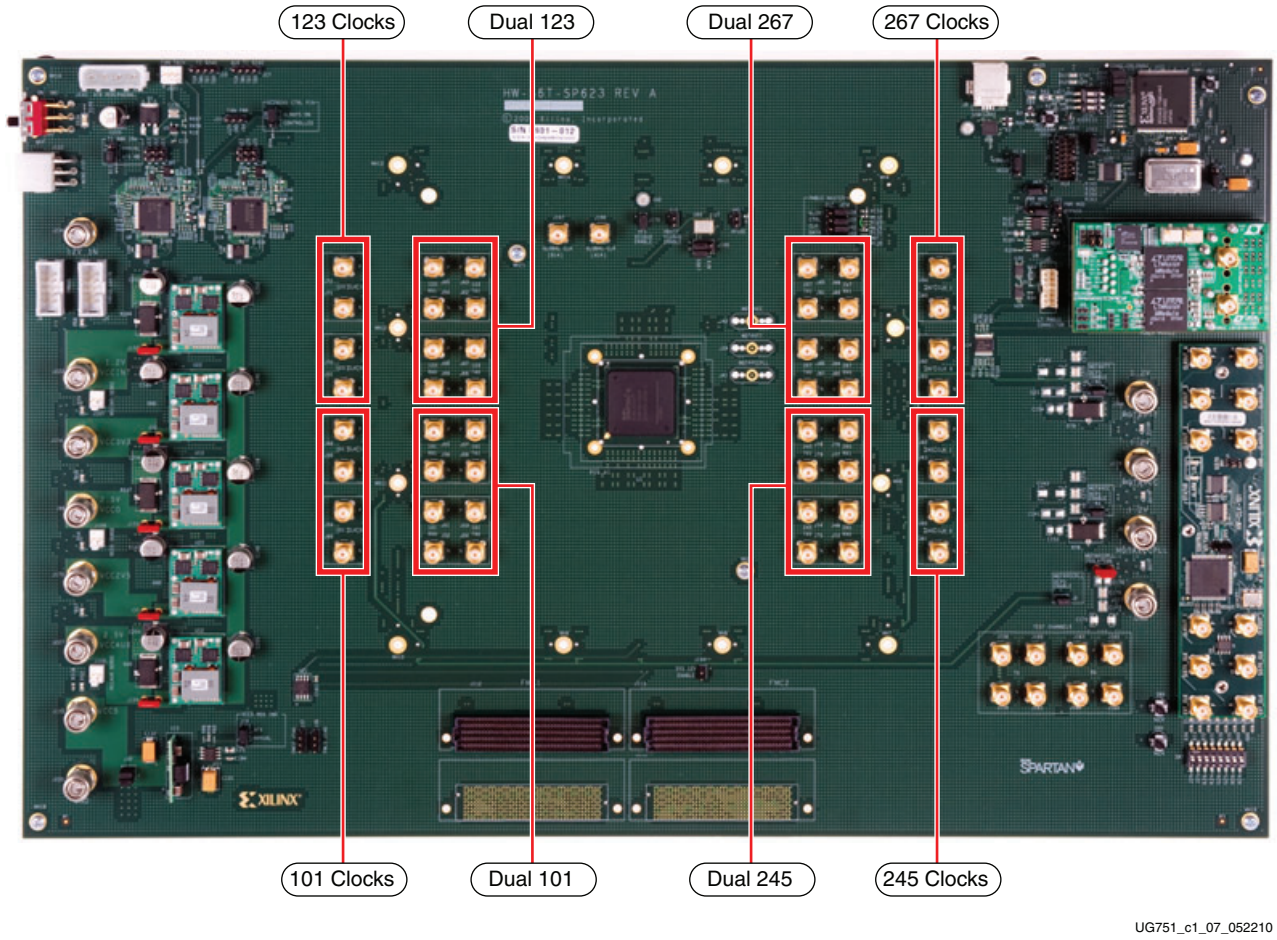


Figure 1-8: **GTP Transceiver and Reference Clock SMA Locations**

Table 1-12: **GTP Transceiver Pins**

FGPA Pin	Net Name	SMA Connector	Trace Length (Mils)
D7	101_RX0_P	J51	4,253
C7	101_RX0_N	J52	4,253
B6	101_TX0_P	J53	3,634
A6	101_TX0_N	J54	3,633
D9	101_RX1_P	J55	3,861
C9	101_RX1_N	J56	3,861

Table 1-12: **GTP Transceiver Pins *(Cont'd)***

FGPA Pin	Net Name	SMA Connector	Trace Length (Mils)
B8	101_TX1_P	J57	2,503
A8	101_TX1_N	J58	2,502
D17	123_RX0_P	J68	3,531
C17	123_RX0_N	J69	3,531
B18	123_TX0_P	J67	3,340
A18	123_TX0_N	J66	3,340
D19	123_RX1_P	J65	3,665
C19	123_RX1_N	J64	3,664
B20	123_TX1_P	J63	2,939
A20	123_TX1_N	J62	2,941
AC8	245_RX0_P	J48	4,316
AD8	245_RX0_N	J73	4,315
AE7	245_TX0_P	J74	3,616
AF7	245_TX0_N	J75	3,615
AC10	245_RX1_P	J76	3,865
AD10	245_RX1_N	J77	3,865
AE9	245_TX1_P	J78	2,563
AF9	245_TX1_N	J79	2,562
AC18	267_RX0_P	J84	3,328
AD18	267_RX0_N	J85	3,327
AE19	267_TX0_P	J86	3,719
AF19	267_TX0_N	J87	3,718
AC20	267_RX1_P	J88	3,952
AD20	267_RX1_N	J89	3,952
AE21	267_TX1_P	J90	3,238
AF21	267_TX1_N	J91	3,239

GTP Transceiver Clock Input SMAs

[Figure 1-2, callout 18]

The SP623 board provides differential SMA connectors that can be used for connecting an external function generator to all GTP transceiver reference clock inputs of the FPGA. The FPGA reference clock pins are connected to the SMA connectors as shown in Table 1-13.

Table 1-13: **GTP Transceiver Clock Inputs to the FPGA**

FPGA Pin	Net Name	SMA Connector
B10	101_REFCLK0_P	J59
A10	101_REFCLK0_N	J60
D11	101_REFCLK1_P	J49
C11	101_REFCLK1_N	J50
D15	123_REFCLK0_P	J70
C15	123_REFCLK0_N	J61
B16	123_REFCLK1_P	J72
A16	123_REFCLK1_N	J71
AE11	245_REFCLK0_P	J80
AF11	245_REFCLK0_N	J81
AC12	245_REFCLK1_P	J82
AD12	245_REFCLK1_N	J83
AC16	267_REFCLK0_P	J92
AD16	267_REFCLK0_N	J93
AE17	267_REFCLK1_P	J94
AF17	267_REFCLK1_N	J95

USB to UART Bridge

[Figure 1-2, callout 19]

Communications between the SP623 board and a host computer are through a USB Mini-B cable connected to J9. Control is provided by U26, a USB to UART bridge (Silicon Laboratories CP2103). Table 1-14 lists the pin assignments and signals for the USB connector J9.

Table 1-14: **USB Mini-B Connector Pin Assignments and Signals**

J9 Pin	Signal Name	Description
1	VBUS	+5V from host system (not used)
2	USB_DATA_N	Bidirectional differential serial data (N-side)
3	USB_DATA_P	Bidirectional differential serial data (P-side)
4	GROUND	Signal ground

The CP2103 supports an IO voltage range of 1.8V to 2.5V on the SP623 board. The connections between the FPGA and CP2103 should use the LVCMOS25 IO standard. UART IP (for example, Xilinx® XPS UART Lite) must be implemented in the FPGA fabric. The FPGA supports the USB to UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to Send (RTS)
- Clear to Send (CTS).

Connections of these signals between the FPGA and the CP2103 at U26 are listed in Table 1-15.

Table 1-15: **FPGA to U26 (CP2103 USB to UART Bridge) Connections**

FPGA Pin	FPGA Function	Net Name	U26 Pin	U26 Function
L23	RTS, output	USB_CTS	22	CTS, input
L23	CTS, input	USB_RTS	23	RTS, output
N20	TX, data out	USB_RX	24	RXD, data in
N19	RX, data in	USB_TX	25	TXD, data out

The bridge device also provides as many as 4 GPIO signals that can be defined by the user for status and control information (Table 1-16).

Table 1-16: **CP2103 USB to UART Bridge User GPIO**

FPGA Pin	Net Name	U26 Pin
P22	USB_GPIO0	19
P21	USB_GPIO1	18
N22	USB_GPIO2	17
N21	USB_GPIO3	16

A royalty-free software driver named Virtual COM Port (VCP) is available from Silicon Laboratories. This driver permits the CP2103 USB to UART bridge to appear as a COM port to the host computer communications application software (for example, HyperTermimal or TeraTerm). The VCP driver must be installed on the host computer prior to establishing communications with the SP623 board.

FMC HPC Connectors

[Figure 1-2, callouts 20a, and 20b]

The SP623 board features two high pin count (HPC) connectors as defined by the VITA 57.1.1 FMC specification. Each FMC HPC connector is a 10 x 40 position socket that is fully populated with 400 pins. See Appendix B, VITA 57.1 FMC HPC Connector Pinout for a cross-reference of signal names to pin coordinates.

The FMC1 HPC connector at J112 on the SP623 board provides connectivity for:

- 58 differential user-defined pairs:
  - 34 LA pairs
  - 24 HA pairs

- 3 differential clocks

The FMC2 HPC connector at J113 on the SP623 board provides connectivity for:

- 57 differential user-defined pairs:
  - 34 LA pairs
  - 23 HA pairs
- 2 differential clocks

Note: The V_{ADJ} voltage for the FMC HPC connectors on the SP623 board is fixed at 2.5V (non-adjustable). The 2.5V rail cannot be turned off. The VITA 57.1 FMC interfaces on the SP623 board are compatible with 2.5V mezzanine cards capable of supporting 2.5V V_{ADJ}.

The connections for the FMC1 and FMC2 connectors are identified in Table 1-17 and Table 1-18, respectively.

Table 1-17: **Vita 57.1 FMC1 HPC Connections at J112**

FPGA Pin	Net Name	FMC Pin
T3	FMC1_CLK0_M2C_P	H4
T1	FMC1_CLK0_M2C_N	H5
B14	FMC1_CLK1_M2C_P	G2
A14	FMC1_CLK1_M2C_N	G3
V4	FMC1_CLK2_M2C_P	K4
W3	FMC1_CLK2_M2C_N	K5
R2	FMC1_HA00_CC_P	F4
R1	FMC1_HA00_CC_N	F5
M4	FMC1_HA01_CC_P	E2
N3	FMC1_HA01_CC_N	E3
N2	FMC1_HA02_P	K7
N1	FMC1_HA02_N	K8
M3	FMC1_HA03_P	J6
M1	FMC1_HA03_N	J7
L2	FMC1_HA04_P	F7
L1	FMC1_HA04_N	F8
K3	FMC1_HA05_P	E6
K1	FMC1_HA05_N	E7
J2	FMC1_HA06_P	K10
J1	FMC1_HA06_N	K11
H3	FMC1_HA07_P	J9
H1	FMC1_HA07_N	J10
G2	FMC1_HA08_P	F10
G1	FMC1_HA08_N	F11