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KCU1250 Board

User Guide

UG1057 (v1.0) December 19, 2014

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/19/2014	1.0	Initial Xilinx release.

Table of Contents

Appendix F: Regulatory and Compliance Information

Appendix F: Additional Resources and Legal Notices

Chapter 1

KCU1250 Board Features and Operation

Introduction

This user guide describes the components, features, and operation of the KCU1250 UltraScale™ FPGA GTH transceiver characterization board. The KCU1250 board provides the hardware environment for characterizing and evaluating the GTH transceivers on an UltraScale XCKU040-2FFVA1156E FPGA. The KCU1250 board schematic, bill-of-material (BOM), layout files, and reference designs are available at the Kintex® UltraScale FPGA KCU1250 Characterization Kit website.

FPGA Compatibility

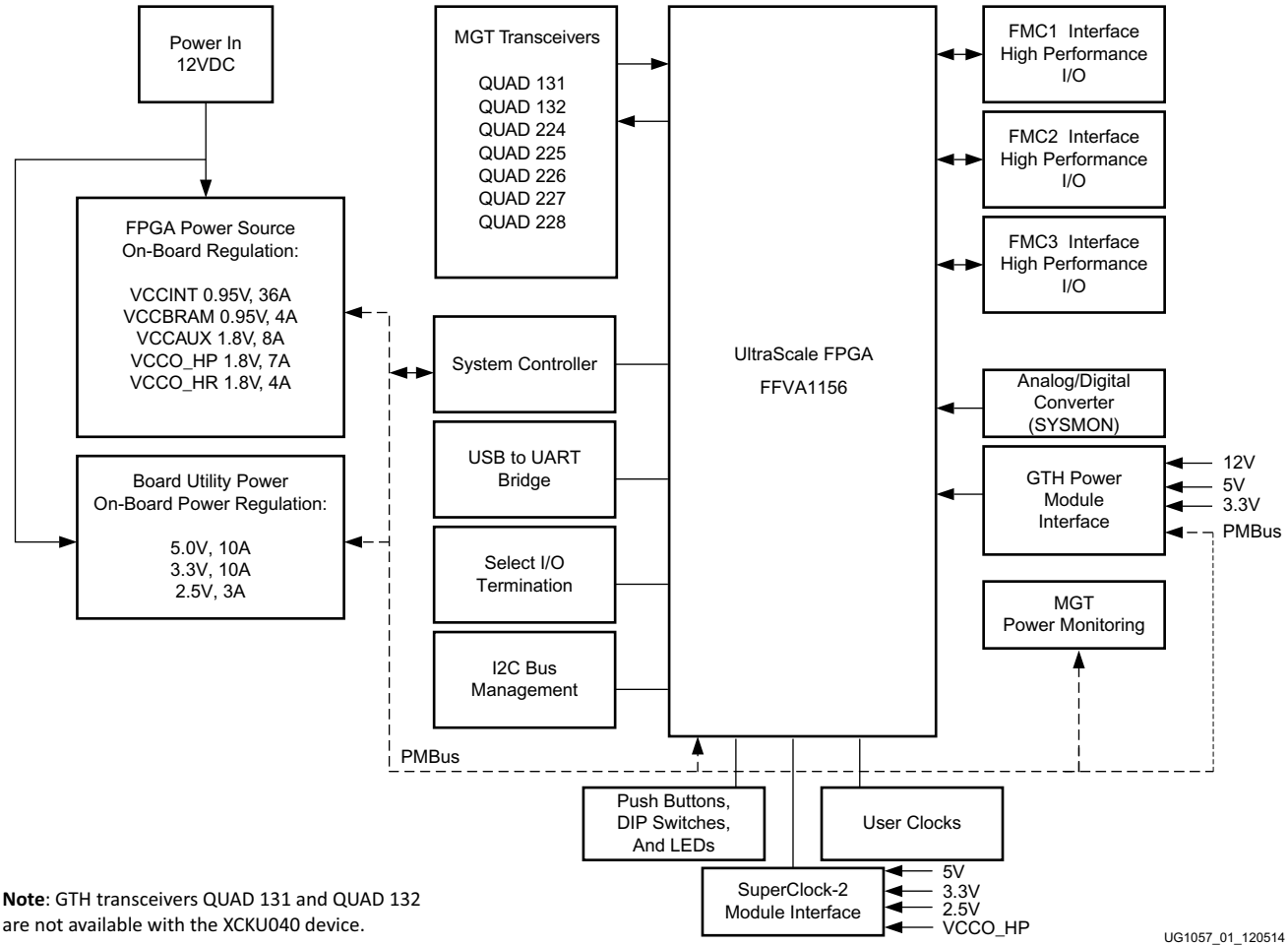
The KCU1250 board is shipped with the Kintex UltraScale XCKU040-2FFVA1156E FPGA. The board also supports other Kintex UltraScale device densities (XCKU035, XCKU060, and XCKU075) in the pin-compatible FFVA1156 package. However, certain GTH transceivers that are available in larger density devices are not available in the XCKU040 device (for example, GTH QUAD_131 and GTH QUAD_132).

KCU1250 Board Features

- UltraScale XCKU040-2FFVA1156E FPGA
- BullsEye cable access to all 20 GTH transceivers on the UltraScale XCKU040-2FFVA1156E FPGA
- Onboard power supplies for all necessary voltages
- Power connectors for optional use of external power supplies
- Digilent USB JTAG programming port
- System controller (Zynq-7000 AP SoC XC7Z010-CLG225)
- MGT power module supporting UltraScale FPGA GTH transceiver power requirements
- A fixed, 300 MHz 2.5V LVDS oscillator wired to multi-region clock capable (MRCC) inputs
- Two pairs of differential MRCC inputs with SMA connectors
- SuperClock-2 module supporting programmable clock outputs

- Samtec BullsEye connector pads for the FPGA GTH transceivers and reference clocks
- General purpose DIP switches, LEDs, pushbuttons, and test I/O
- Three VITA 57.1 FPGA mezzanine card (FMC) high pin count (HPC) connectors
- USB to dual-UART bridge
- I2C bus
- PMBus connectivity to the boards digital power supplies
- Active cooling for the FPGA

The KCU1250 board block diagram is shown in Figure 1-1.



Note: GTH transceivers QUAD 131 and QUAD 132 are not available with the XCKU040 device.

Figure 1-1: **KCU1250 Board Block Diagram**

Detailed Description

Figure 1-2 shows the KCU1250 board. Each numbered feature referenced in Figure 1-2 is described in Table 1-1 and in subsequent sections.

CAUTION! *The KCU1250 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board*

CAUTION! *Do not remove the rubber feet from the board. The feet provide clearance to prevent short circuits on the back side of the board*

IMPORTANT: *Figure 1-2 is for reference only and might not reflect the current revision of the board.*

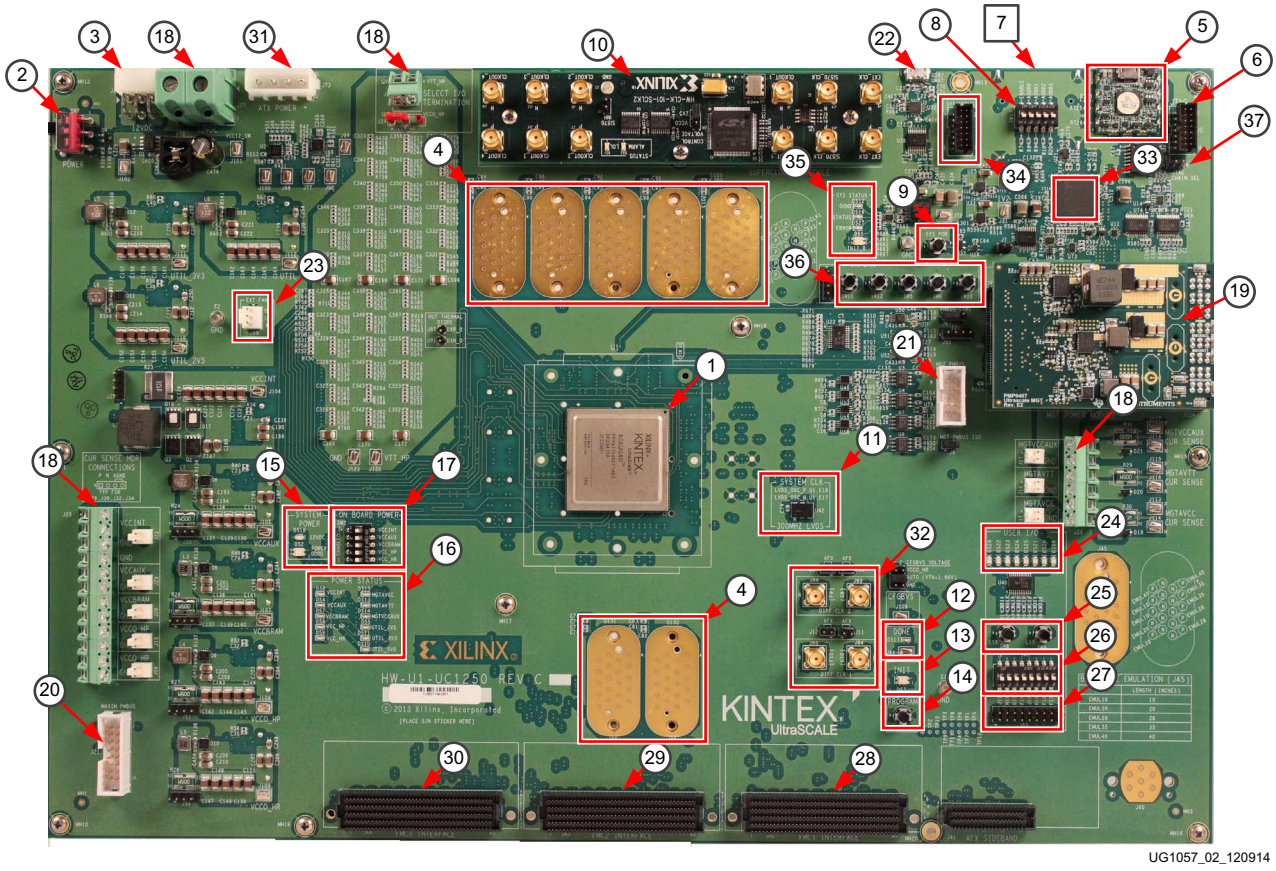


Figure 1-2: **KCU1250 Board Features**

Table 1-1 describes the callouts in Figure 1-2.

Table 1-1: **KCU1250 Board Features and Operation**

Figure 1-2 Callout	Reference Designator	Feature Description
1	U1	UltraScale XCKU040-2FFVA1156E FPGA, page 18
2	SW1	Power switch, page 10
3	J28	12V mini-fit connector, page 9
4	J37, J38, J39, J40, J41, J42, J43	GTH transceiver connector pads Q224, Q225, Q226, Q227, Q228 page 28
5	U80	Digilent USB JTAG connector (micro-B receptacle), page 18
6	J2	Platform USB JTAG connector (alternate access for programming cables), page 18
7	J10	SD card connector (back-side of board), page 18
8	SW13	System controller configuration DIP switches, page 21
9	SW4	System controller power on reset (SYS_POR) button, page 20
10	J36	SuperClock-2 module, page 24
11	U42	300 MHz LVDS oscillator, page 23
12	DS17	FPGA DONE status LED, page 25
13	DS3	FPGA INIT status LED, page 25
14	SW7	FPGA PROGRAM pushbutton, page 27
15	DS18	12V system power status LED, page 14
16	DS4, DS5, DS6, DS7, DS8, DS9, DS10, DS28, DS13, DS14, DS15	Status LEDS for FPGA logic, transceiver and utility power
17	SW2	Power regulation inhibitor switch for onboard regulators, page 13
18	J5, J25, J26, J27	External power supply connectors, page 13 and page 14
19	J46, J124	MGT transceiver power supply module, page 15
20	J21	FPGA and utility rails PMBUS connector, page 14
21	J4	MGT rails PMBUS connector, page 13
22	J1	Connector for USB to dual-UART bridge (mini-B receptacle), page 23
23	J99	Power connector for active heatsink, page 16
24	DS19, DS20, DS21, DS22, DS23, DS24, DS25, DS26	User LEDs (active-High), page 25
25	SW8, SW9	User pushbuttons (active-High), page 27
26	SW3	User DIP switches (active-High), page 26
27	J95	User I/O header, page 27
28	JA2	FMC1 connector, page 35
29	JA3	FMC2 connector page 38

Table 1-1: **KCU1250 Board Features and Operation *(Cont'd)***

Figure 1-2 Callout	Reference Designator	Feature Description
30	JA4	FMC3 connector page 41
31	J73	ATX power connector page 9
32	J83, J84, J85, J86	SMA connectors to differential MRCC pins on FPGA, page 23
33	U38	System controller
34	J3	System controller JTAG connector
35	DS1, DS12, DS16, DS27	System controller status LEDs
36	SW5, SW6, SW10, SW11, SW12	System controller GPIO pushbuttons
37	J36	JTAG chain select

Power Management

12V Input Power

The KCU1250 board receives 12V main power through J28 (callout 3, Figure 1-2) using the 12V AC adapter included with the KCU1250 board characterization kit. J28 is a 6-pin (2 x 3), right angle, mini-fit connector.

CAUTION! *When supplying 12V through J28, use only the power supply provided for use with this board (Xilinx part number 3800033).*

CAUTION! *Do NOT use a 6-pin, PC ATX power supply connector with J28. The pinout of the 6-pin, PC ATX connector is not compatible with J28 and the board will be damaged if an attempt is made to power it from a PC ATX power supply connector.*

12V power can also be provided through:

- Connector J73 (callout 31, Figure 1-2), which accepts an ATX hard drive 4-pin power plug
- Connector J27 (callout 18, Figure 1-2), which can be connected to a bench-top power supply

CAUTION! *Because connector J73 provides no reverse polarity protection, use a power supply with a current limit set at 6A maximum.*

CAUTION! *Do NOT apply 12V power to more than a single input source. For example, do not apply power to J73 and J27 at the same time.*

CAUTION! *The KCU1250 board uses a P-channel MOSFET power switch (FDS6681Z, reference designator Q1) that is rated for 20A @ 12V. It is critical that the power consumed by the DUT and peripheral circuitry does not exceed this limit.*

Power Switch

The KCU1250 board main power is turned on or off using the SW1 switch (callout 2, Figure 1-2). When the switch is in the on position, power is applied to the board and the green LED DS18 illuminates (callout 15, Figure 1-2).

Onboard Power Regulation

Figure 1-3 shows the onboard power supply architecture.

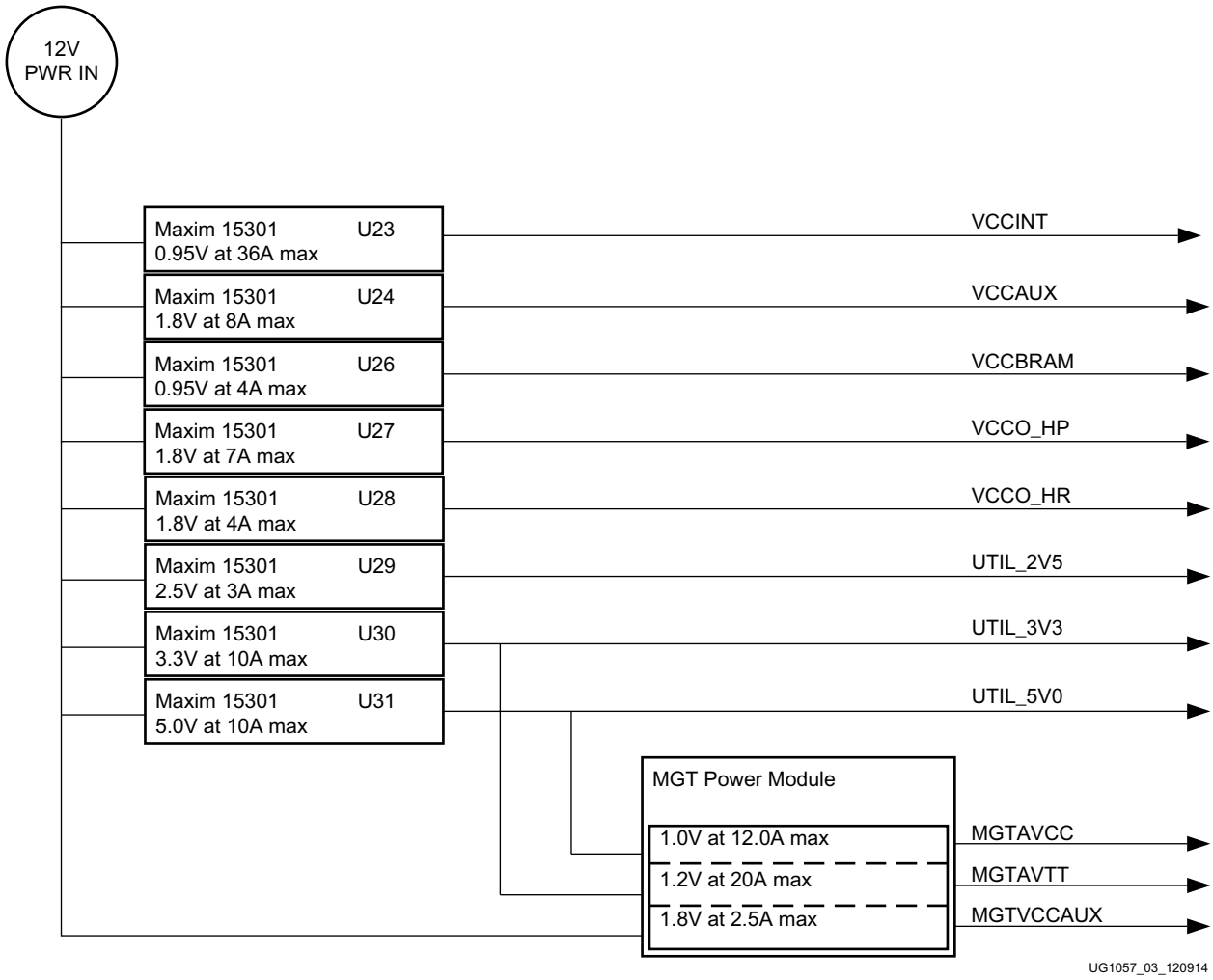


Figure 1-3: **KCU1250 Board Power Supply Block Diagram**

The KCU1250 board uses power regulators and PMBus compliant digital PWM system controllers from Maxim Integrated to supply the FPGA logic and utilities voltages listed in Table 1-2. The board can also be configured to use an external bench power supply for each voltage. See Using External Power Sources.

Table 1-2: **Onboard Power System Devices**

Device Part Number	Reference Designator	Description	Power Rail Net Name	Voltage
FPGA Logic				
Maxim MAX15301	U23	InTune Digital Point of Load (PoL) Controller, 36A	V_{CCINT}	0.95V
Maxim MAX15301	U24	InTune Digital Point of Load (PoL) Controller, 8A	V_{CCAUX}	1.8V
Maxim MAX15301	U26	InTune Digital Point of Load (PoL) Controller, 4A	V_{CCBRAM}	0.95V
Maxim MAX15301	U27	InTune Digital Point of Load (PoL) Controller, 7A	V_{CCO_HP}	1.8V
Maxim MAX15301	U28	InTune Digital Point of Load (PoL) Controller, 4A	V_{CCO_HR}	1.8V
Utility				
Maxim MAX15301	U31	InTune Digital Point of Load (PoL) Controller, 10A	UTIL_5V0	5.0V
Maxim MAX15301	U30	InTune Digital Point of Load (PoL) Controller, 10A	UTIL_3V3	3.3V
Maxim MAX15301	U29	InTune Digital Point of Load (PoL) Controller, 3A	UTIL_2V5	2.5V
MGT Transceivers (monitoring only)				
INA226	U50	Current shunt and power monitor with I2C interface	MGTAVCC	1.0V
INA226	U51	Current shunt and power monitor with I2C interface	MGTAVTT	1.2V
INA226	U52	Current shunt and power monitor with I2C interface	MGTVCCAUX	1.8V
System Controller				
Maxim MAX15053	U13	Fixed LDO regulator	SYS_1V0	1.0V
Maxim MAX15027	U33	Fixed LDO regulator	VCC_1V2	1.2V
Maxim MAX15027	U25	Fixed LDO regulator	VCC_1V8	1.8V

Notes:

1. The output voltages of the Max15301 can be reprogrammed using the Maxim InTune Digital Power Tool [Ref 5]. However, extreme caution must be taken when attempting to modify any of the onboard regulators. An incorrectly programmed regulator can damage onboard components.

Using External Power Sources

Each power rail for the FPGA logic and MGT transceivers has an associated Euro-Mag spring-clamp terminal block (callout 18, Figure 1-2), which can be used to provide power from an external source (Table 1-3).

CAUTION! *Do NOT apply power to any of the FPGA logic external power supply connectors without first disabling the associated regulator or regulators. Failing to disable the regulator can damage the board.*

Each onboard FPGA logic regulator can be disabled using its respective power regulation inhibitor dip switch (callout 17, Figure 1-2). A regulator is disabled when the power regulation inhibitor switch is set to the on position. Table 1-3 lists external power connectors for the different power rails.

Table 1-3: **FPGA Logic and MGT Transceiver Rails**

	Power Rail Net Name	External Supply Connector	Power Regulation Jumper
FPGA Logic	V_{CCINT}	J25	J22
	V_{CCAUX}		J23
	V_{CCBRAM}		J20
	V_{CCO_HP}		J19
	V_{CCO_HR}		J18
MGT Transceiver	MGTAVCC	J26	NA
	MGTAVTT		NA
	MGTVCCAUX		NA

Notes:

1. The MGT power module must be removed before providing external power to any of the transceiver rails (see MGT Transceiver Power Module, page 15)

Default Jumper and Switch Positions

A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.

Monitoring Voltage and Current

Voltage and current monitoring and control for the Maxim power system is available through either the KCU1250 system controller or via the Maxim PowerTool™ software graphical user interface.

The KCU1250 system controller is the simplest and most convenient way to monitor the voltage and current values for the power rails listed in Table 1-3. For details on how to use this built-in feature, see Power Monitoring Data Menu in Appendix D.

The KCU1250 board includes these PMBus connectors:

- J21 (callout 20, Figure 1-2), for use with the Maxim USB-to-PMBus interface dongle (MAXPOWERTOOL002 [Ref 8]) and the InTune Digital Power GUI.
- J4 (callout 21, Figure 1-2) is used to connect to the MGT power module PMBus using the vendor's application tool (for example, Texas Instruments USB-to-GPIO interface adaptor (EVM-P960 [Ref 9]) and the Fusion Digital Power GUI).

The onboard Maxim power controllers (U23, U24, U26, U27, U28, U29, U30, and U31) by default are isolated from the MGT power modules PMBus. However, the two interfaces can be linked by removing J8 next to the MGT power module PMBus connector J4. This configuration is required when using a Maxim MGT power module to allow for monitoring and controlling both FPGA power rails and the transceiver power rails using the Maxim InTune Digital Power GUI.

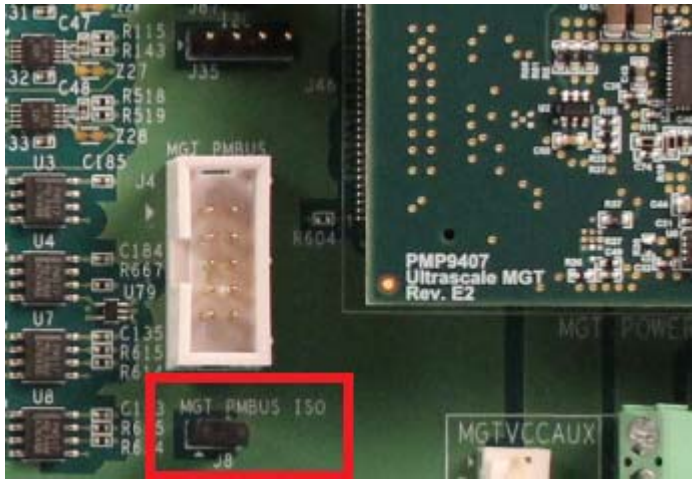


Figure 1-4:

More information about the power system components used on the KCU1250 board is available from the Maxim Integrated InTune digital power website [Ref 5].

MGT Transceiver Power Module

The KCU1250 board includes one MGT transceiver power module (callout 19, Figure 1-2). The MGT power modules supply the MGTAVCC, MGTAVTT, and MGTVCCAUX power rails, which connect to the FPGA MGT transceivers. MGT power modules from third-party vendors are provided with the KCU1250 board for evaluation (Maxim Integrated MAXIM001 and Texas Instruments PMP9463 [Ref 5]). Either one of the modules can be plugged into J46 and J124 on the outlined and labeled power module locations shown in Figure 1-5.

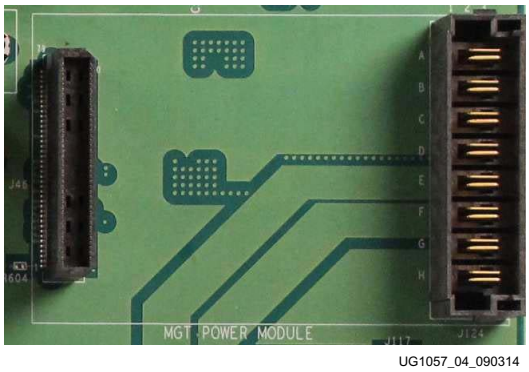


Figure 1-5: **Mounting Location, MGT Power Module**

Table 1-4 lists the nominal voltage values for MGTAVCC, MGTAVTT, and MGTVCCAUX power rails. It also lists the maximum current rating for each rail supplied by MGT modules included with the KCU1250 board.

Table 1-4: **MGT Power Modules**

MGT Transceiver Rail Net Name	Nominal Voltage	Maximum Current Rating
MGTAVCC	1.0V	12A
MGTAVTT	1.2V	20A
MGTVCCAUX	1.8V	2.5A

The MGT transceiver power rails can also be supplied externally. The external supply connectors are described in Table 1-3.

CAUTION! *The MGT Power Module MUST be removed when providing external power to the MGT transceiver rails.*

Information about the available MGT power modules included with the KCU1250 board characterization kit is available from the vendor websites [Ref 5].

Active Heatsink Power Connector

An active heat sink (Figure 1-6) is provided for the FPGA (callout 23, Figure 1-2). A 12V fan is affixed to the heat sink and is powered from the 3-pin friction lock header J99 (Figure 1-7).

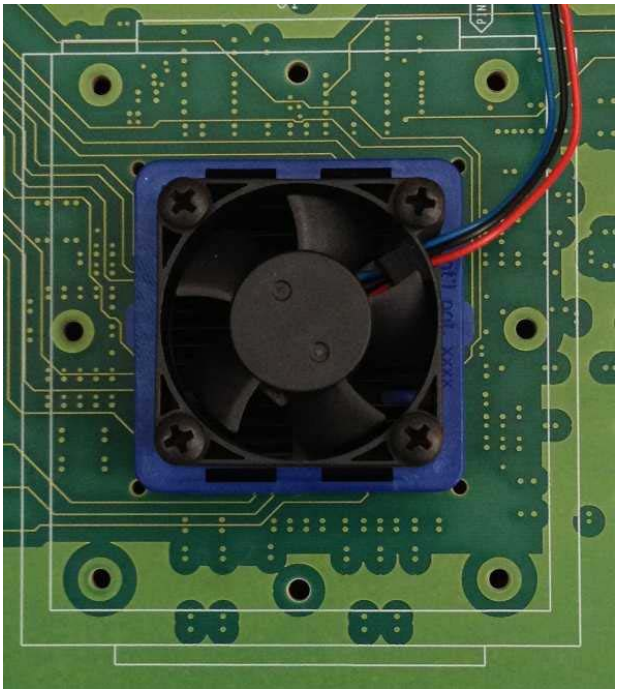


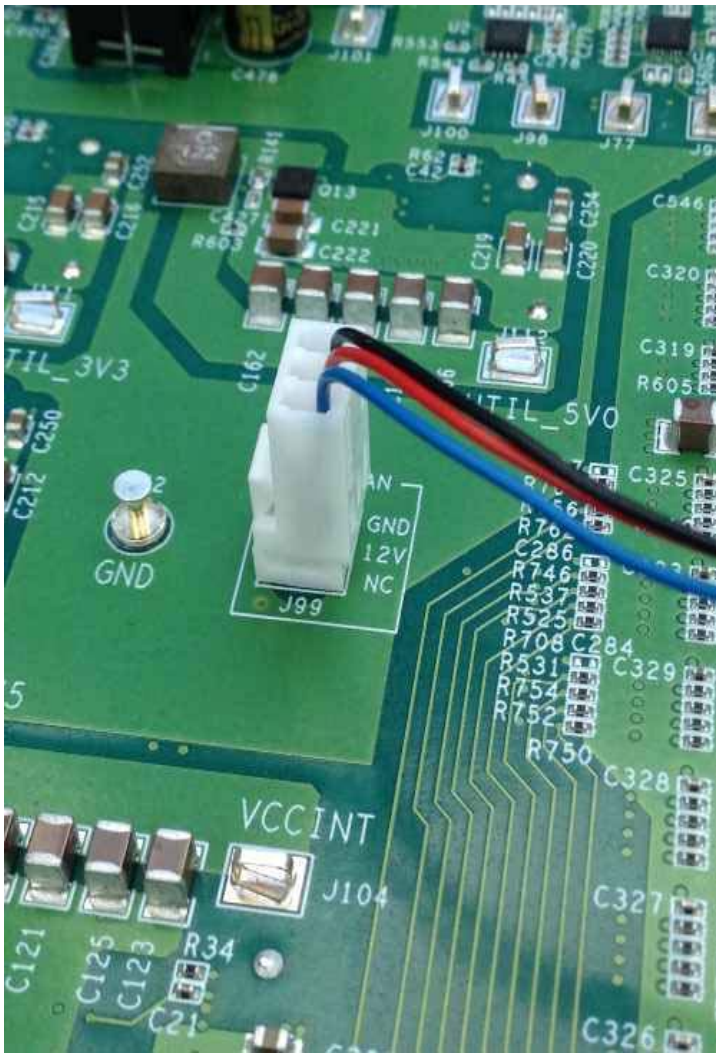
Figure 1-6: **Active FPGA Heat Sink**

The fan power connections are detailed in Table 1-6:

Table 1-5: **Fan Power Connections**

Fan Wire	Header Pin
Black	J99.1 - GND
Red	J99.2 - 12V
Blue	J99.3 - NC

Figure 1-7 shows the heat sink fan power connector J99.



UG1057_06_090314

Figure 1-7: **Heat Sink Fan Power Connector J99**

UltraScale FPGA

The KCU1250 board is populated with the UltraScale XCKU040-2FFVA1156E FPGA at U1 (callout 1, Figure 1-2). For further information on UltraScale FPGAs, see *UltraScale Architecture and Product Overview* (DS890) [Ref 1].

FPGA Configuration

The FPGA is configured though one of these options:

- Digilent embedded USB JTAG connector (callout 5, Figure 1-2)
- Platform cable USB JTAG cable connector (callout 6, Figure 1-2)
- SD card using the Zynq-7000 AP SoC system controller in 8-bit SelectMAP mode (callout 7, Figure 1-2)

The KCU1250 board includes an embedded USB-to-JTAG configuration module (Digilent U80), which allows a host computer to access the JTAG chain using a standard A to micro-B USB cable. Alternatively, a JTAG connector (J2) is available to access the JTAG chain using the Xilinx platform cable USB II configuration cable. Additionally, the FPGA can be configured from an SD card installed in J10 with the help of the system controller U38, which reads a predefined bit file from the SD card and configures the FPGA in 8-bit SelectMAP configuration mode. See FPGA CONFIG Menu.

The JTAG chain of the KCU1250 board is shown in Figure 1-8. By default, only the UltraScale FPGA is part of the chain (J6 jumper uninstalled). Installing the J6 jumper enables an 8-bit bus transceiver (U69, SN74AVC8T245) and adds the FMC interfaces to the chain.

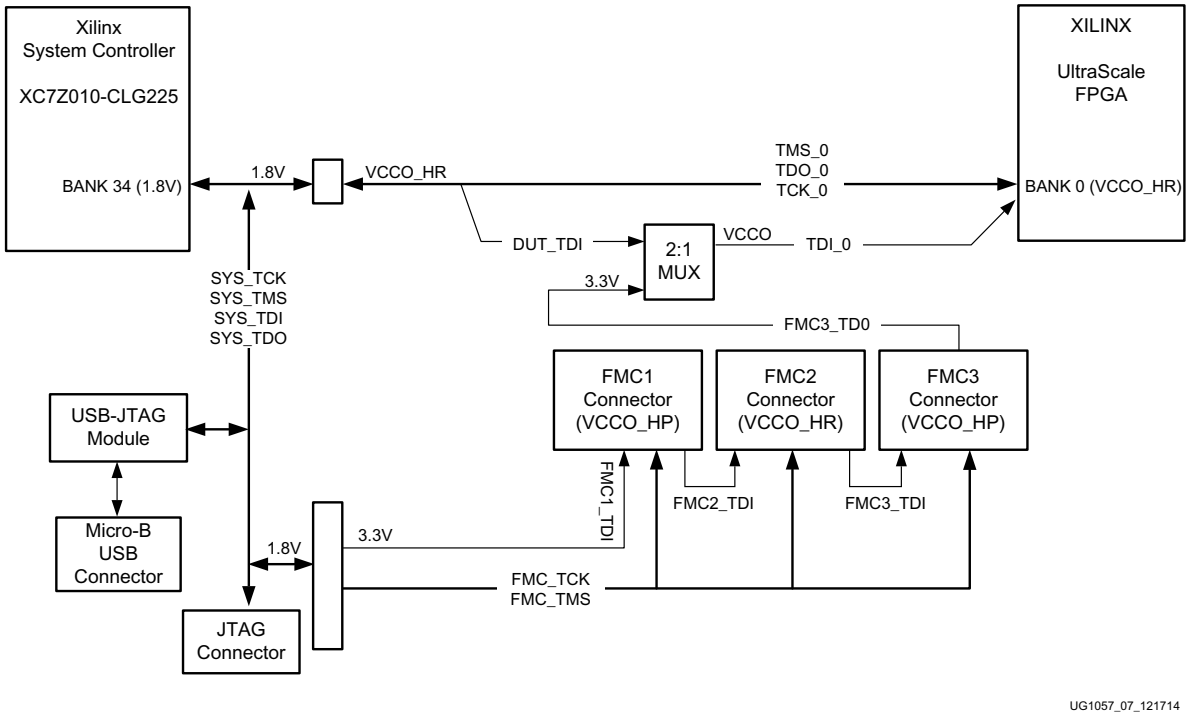


Figure 1-8: **JTAG Chain**

PROGRAM Pushbutton

Pressing the PROGRAM pushbutton SW7 (callout 14, Figure 1-2) asserts the active-Low program pin of the FPGA.

DONE LED

The DONE LED DS17 (callout 12, Figure 1-2) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, DS17 lights up indicating the FPGA is successfully configured.

INIT LED

The dual-color INIT LED DS3 (callout 13, Figure 1-2) indicates the FPGA initialization status. During FPGA initialization, the INIT LED illuminates RED. When FPGA initialization has completed, the LED illuminates GREEN.

System Controller

The KCU1250 board utilizes a Xilinx XC7Z010-CLG225 Zynq-7000 AP SoC U38 (callout 33, Figure D-1) system controller that can be used to:

- Configure the FPGA using predefined selection of configuration bit files on an SD card using 8-bit SelectMAP configuration
- Select the output frequencies of the SuperClock-2 module
- Monitor the onboard power system (PMBus)

See Appendix D, System Controller for information on the system controller menu options.

System Controller Reset

The SYS_POR pushbutton SW4 (callout 9, Figure 1-2) asserts the active-Low system controller Power-On Reset (SYS_POR). When SYS_POR is reasserted, the system controller is reconfigured using the controller design stored on an attached SPI flash.

System Controller Status LEDs

DS1, DS12, DS16, and DS27 (callout 35, Figure 1-2) show the system controller INIT_B, DONE, STATUS, and ERROR status, respectively.

System Controller Configuration DIP Switches

The DIP switch SW13 (callout 8, Figure 1-2) shown in Figure 1-9 selects the address of the UltraScale FPGA configuration bitstream to be loaded from the SD card. The switch ON position is indicated by the arrow next to bit 1 of the switch.

The ENABLE bit (switch position 1) is used to enable the SD card configuration mode.

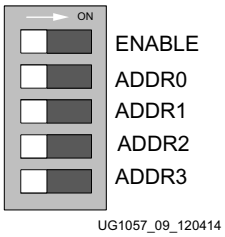


Figure 1-9: **Configuration DIP Switch (SW13)**

The switch settings for selecting each address are shown in Table 1-6.

Table 1-6: **SW13 DIP Switch Configuration**

Configuration Bitstream Address	ADDR3	ADDR2	ADDR1	ADDR0
0	OFF	OFF	OFF	OFF
1	OFF	OFF	OFF	ON
2	OFF	OFF	ON	OFF
3	OFF	OFF	ON	ON
4	OFF	ON	OFF	OFF
5	OFF	ON	OFF	ON
6	OFF	ON	ON	OFF
7	OFF	ON	ON	ON
8	ON	OFF	OFF	OFF
9	ON	OFF	OFF	ON
10	ON	OFF	ON	OFF
11	ON	OFF	ON	ON
12	ON	ON	OFF	OFF
13	ON	ON	OFF	ON
14	ON	ON	ON	OFF
15	ON	ON	ON	ON

System Controller GPIO Pushbuttons

SW5, SW6, SW10, SW11, SW12 (callout 36, Figure 1-2) are active-High pushbuttons connected to GPIO pins on the system controller. See GPIO Data Menu for more details.

USB to Dual-UART Bridge

The KCU1250 board uses a single-chip USB to dual-UART bridge (U32, Silicon Laboratories CP2105) for simultaneous serial communication between a host terminal and the UltraScale FPGA, and between a host terminal and the Zynq-7000 AP SoC system controller. The onboard micro-B receptacle USB connector J1 (callout 22, Figure 1-2) is connected to the dual-UART bridge.

The FPGA connects through a serial communication terminal connection (115200-8-N-1) using the standard communication port of the Silicon Labs USB to dual-UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to send (RTS)
- Clear to send (CTS)

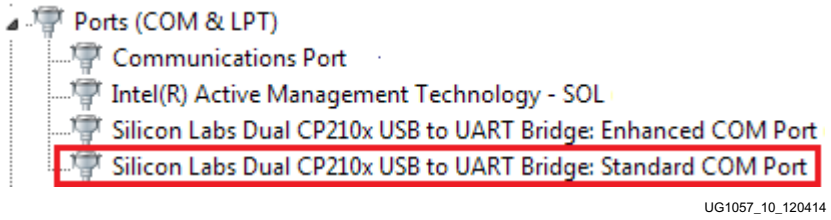


Figure 1-10: **Silicon Labs USB to UART Bridge Standard COM Port**

The dual-UART interface connections are split between two components:

- UART1 SCI (standard) interface is connected to the XCKU040 FPGA
- UART2 ECI (enhanced) interface is connected to the XC7Z010 system controller

Silicon Labs provides royalty-free virtual COM port (VCP) drivers for the host computer. These drivers permit the CP2105GM dual USB-to-UART bridge to appear as a pair of COM ports to communications application software (for example, TeraTerm or HyperTerm) that runs on the host computer.

IMPORTANT: *The VCP device drivers must be installed on the host PC prior to establishing communications with the KCU1250 board.*

The driver assigns the higher PC COM port number to UART1 (SCI) and the lower PC COM port number to UART(ECI).

The connections of these signals between the FPGA and the Silicon Labs CP2105 are listed in Table 1-7.

Table 1-7: **FPGA to UART Connection**

FPGA(U1)				Schematic Net Name	Device(U32)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
D14	RTS	Output	LVCMOS18	UART_CTS_I_B	18	CTS	Input
C14	CTS	Input	LVCMOS18	UART_RTS_O_B	19	RTS	Output
A14	TX	Output	LVCMOS18	UART_RXD_I	20	RXD	Input
B14	RX	Input	LVCMOS18	UART_TXD_O	21	TXD	Output

The bridge device also provides as many as four GPIO signals that you can define for status and control information (Table 1-8).

Table 1-8: **CP2105 USB to Dual-UART Bridge User GPIO**

FPGA(U1)				Schematic Net Name	Device(U32)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
F14	SelectIO™	In/Out	LVCMOS18	UART_GPIO_0	24	GPIO	In/Out
G14	SelectIO	In/Out	LVCMOS18	UART_GPIO_1	23	GPIO	In/Out
J14	SelectIO	In/Out	LVCMOS18	UART_GPIO_2	22	GPIO	In/Out
J15	SelectIO	In/Out	LVCMOS18	UART_GPIO_3	15	GPIO	In/Out

The second port of the CP2105 USB to dual-UART is connected to the onboard system controller. See Appendix D, System Controller.

300 MHz LVDS Oscillator

The KCU1250 board has one 300 MHz LVDS oscillator U42 (callout 11, Figure 1-2) connected to multi-region clock capable (MRCC) inputs on the FPGA. Table 1-9 lists the FPGA pin connections to the LVDS oscillator.

Table 1-9: **10 LVDS Oscillator MRCC Connections**

FPGA (U1)				Schematic Net Name	Device (42)		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
E18	SYSTEM CLOCK_P	Input	LVDS	LVDS_OSC_P	4	300 MHz LVDS oscillator	Output
E17	SYSTEM CLOCK_N	Input	LVDS	LVDS_OSC_N	5	300 MHz LVDS oscillator	Output

Differential SMA MRCC Pin Inputs

The KCU1250 board provides two pairs of differential SMA transceiver clock inputs (callout 32, Figure 1-2) that can be used for connecting to an external clock source. The FPGA MRCC pins are connected to the SMA connectors as shown in Table 1-10.

Table 1-10: **Differential SMA Clock Connections**

FPGA(U1)				Schematic Net Name	SMA Connector
Pin	Function	Direction	IOSTANDARD		
G10	USER CLOCK_1_P	Input	LVDS	CLK_DIFF_1_P	J84
F10	USER CLOCK_1_N	Input	LVDS	CLK_DIFF_1_N	J85
G9	USER CLOCK_2_P	Input	LVDS	CLK_DIFF_2_P	J83
F9	USER CLOCK_2_N	Input	LVDS	CLK_DIFF_2_N	J86

SuperClock-2 Module

The SuperClock-2 module (callout 10, Figure 1-2) connects to the clock module interface connector (J36) and provides a programmable, low-noise and low-jitter clock source for the KCU1250 board (see *SuperClock-2 Module User Guide* (UG770) [Ref 4]). The clock module maps to FPGA I/O by way of 14 control pins, 2 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-11 shows the FPGA I/O mapping for the SuperClock-2 module interface. The KCU1250 board supplies UTIL_5V0, UTIL_3V3, UTIL_2V5, and V_{CCO_HP} input power to the clock module interface.

Table 1-11: **SuperClock-2 FPGA I/O Mapping**

FPGA(U1)				Schematic Net Name	J36 Pin		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
U34	Clock recovery	Input	LVDS	CM_LVDS1_P	1	Clock recovery	Output
V34	Clock recovery	Input	LVDS	CM_LVDS1_N	3	Clock recovery	Output
J8	Clock recovery	Input	LVDS	CM_LVDS2_P	9	Clock recovery	Output
H8	Clock recovery	Input	LVDS	CM_LVDS2_N	11	Clock recovery	Output
AK22	Regional clock	Input	LVDS	CM_GCLK_P	25	Global clock	Output
AK23	Regional clock	Input	LVDS	CM_GCLK_N	27	Global clock	Output
AN23	Control I/O	Output	LVCMOS18	CM_H_DEC	67	DEC	Input
AP23	Control I/O	Output	LVCMOS18	CM_H_INC	69	INC	Input
AP24	Control I/O	Output	LVCMOS18	CM_FS_ALIGN	71	ALIGN	Input
AP25	Control I/O	Input	LVCMOS18	CM_H_LOL	79	LOL	Output

Table 1-11: **SuperClock-2 FPGA I/O Mapping *(Cont'd)***

FPGA(U1)				Schematic Net Name	J36 Pin		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
AP20	Control I/O	Output	LVCMOS18	CM_H_INT_ALRM	81	INT_ALRM	Input
AP21	Control I/O	Output	LVCMOS18	CM_C1B	83	C1B	Input
AM24	Control I/O	Output	LVCMOS18	CM_C2B	85	C2B	Input
AN24	Control I/O	Output	LVCMOS18	CM_C3B	87	C3B	Input
AM22	Control I/O	Output	LVCMOS18	CM_C1A	89	C1A	Input
AN22	Control I/O	Output	LVCMOS18	CM_C2A	91	C2A	Input
AM21	Control I/O	Output	LVCMOS18	CM_H_CS0_C3A	95	CS0_C3A	Input
AN21	Control I/O	Output	LVCMOS18	CM_H_CS1_C4A	97	CS1_C4A	Input
AL24	CM_RESET	Output	LVCMOS18	CM_RST	66	RESET_B	Input

User LEDs (Active-High)

DS19 through DS26 (callout 24, Figure 1-2) are eight active-High LEDs that are connected to user I/O pins on the FPGA, as shown in Table 1-12. These LEDs can be used to indicate status (or other functions).

Table 1-12: **User LEDs**

FPGA(U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	IOSTANDARD		
D18	User LED	Output	LVCMOS18	APP_LED1	DS19
D19	User LED	Output	LVCMOS18	APP_LED2	DS20
C18	User LED	Output	LVCMOS18	APP_LED3	DS21
C19	User LED	Output	LVCMOS18	APP_LED4	DS25
B19	User LED	Output	LVCMOS18	APP_LED5	DS24
D18	User LED	Output	LVCMOS18	APP_LED6	DS23
D19	User LED	Output	LVCMOS18	APP_LED7	DS22
C18	User LED	Output	LVCMOS18	APP_LED8	DS26