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ML623 Virtex-6 FPGA GTX Transceiver Characterization Board

User Guide

UG724 (v1.1) September 15, 2010

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/30/10	1.0	Initial Xilinx release.
09/15/10	1.1	Added information about the Intersil power module to the paragraphs under GTX Transceiver Power Module, page 13, and to Table 1-2. Corrected sequence of P and N suffixes to Table 1-18 starting on FPGA pin T31 and ending on pin W27.

Table of Contents

About This Guide

This document describes the basic setup, features, and operation of the ML623 Virtex-6 FPGA GTX transceiver characterization board. The ML623 board provides the hardware environment for characterizing and evaluating the GTX transceivers available on the Virtex®-6 XC6VLX240T-2FFG1156C FPGA.

Guide Contents

This user guide contains the following chapters and appendices:

- Chapter 1, ML623 Board Features and Operation, describes the components, features, and operation of the ML623 Virtex-6 FPGA GTX transceiver characterization board.
- Appendix A, Default Jumper Positions, lists the jumpers that must be installed on the board for proper operation.
- Appendix B, VITA 57.1 FMC HPC Connector Pinout, provides a pinout reference for the FPGA mezzanine card (FMC) connector.
- Appendix C, ML623 Master UCF Listing, provides a listing of the ML623 master user constraints file (UCF).
- Appendix D, References, provides a list of references and links to related documentation.

To find additional documentation, see the Xilinx website at:

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Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *Command Line Tools User Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

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Chapter 1

ML623 Board Features and Operation

This chapter describes the components, features, and operation of the ML623 Virtex-6 FPGA GTX transceiver characterization board. The ML623 board provides the hardware environment for characterizing and evaluating the GTX transceivers available on the Virtex®-6 XC6VLX240T-2FFG1156C FPGA.

ML623 Board Features

- Virtex-6 XC6VLX240T-2FFG1156C FPGA
- On-board power supplies for all necessary voltages
- Power supply jacks for optional use of external power supplies
- JTAG configuration port for use with Platform Cable USB or Parallel Cable III/IV cables
- System ACE™ controller
- Power module supporting all Virtex-6 FPGA GTX transceiver power requirements
- A fixed, 200 MHz 2.5V LVDS oscillator wired to global clock inputs
- Two single-ended global clock inputs with SMA connectors
- Two pairs of differential global clock inputs with SMA connectors
- SuperClock-2 module supporting multiple frequencies
- 40 pairs of SMA connectors for the GTX transceivers
- 10 differential SMA connector pairs for the GTX transceiver clock inputs
- Power status LEDs
- General purpose DIP switches, LEDs, push buttons, and test I/O
- Three VITA 57.1 FMC HPC connectors
- System Monitor interface
- USB to UART bridge
- I^2C bus

The ML623 board block diagram is shown in Figure 1-1.

Caution! The ML623 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

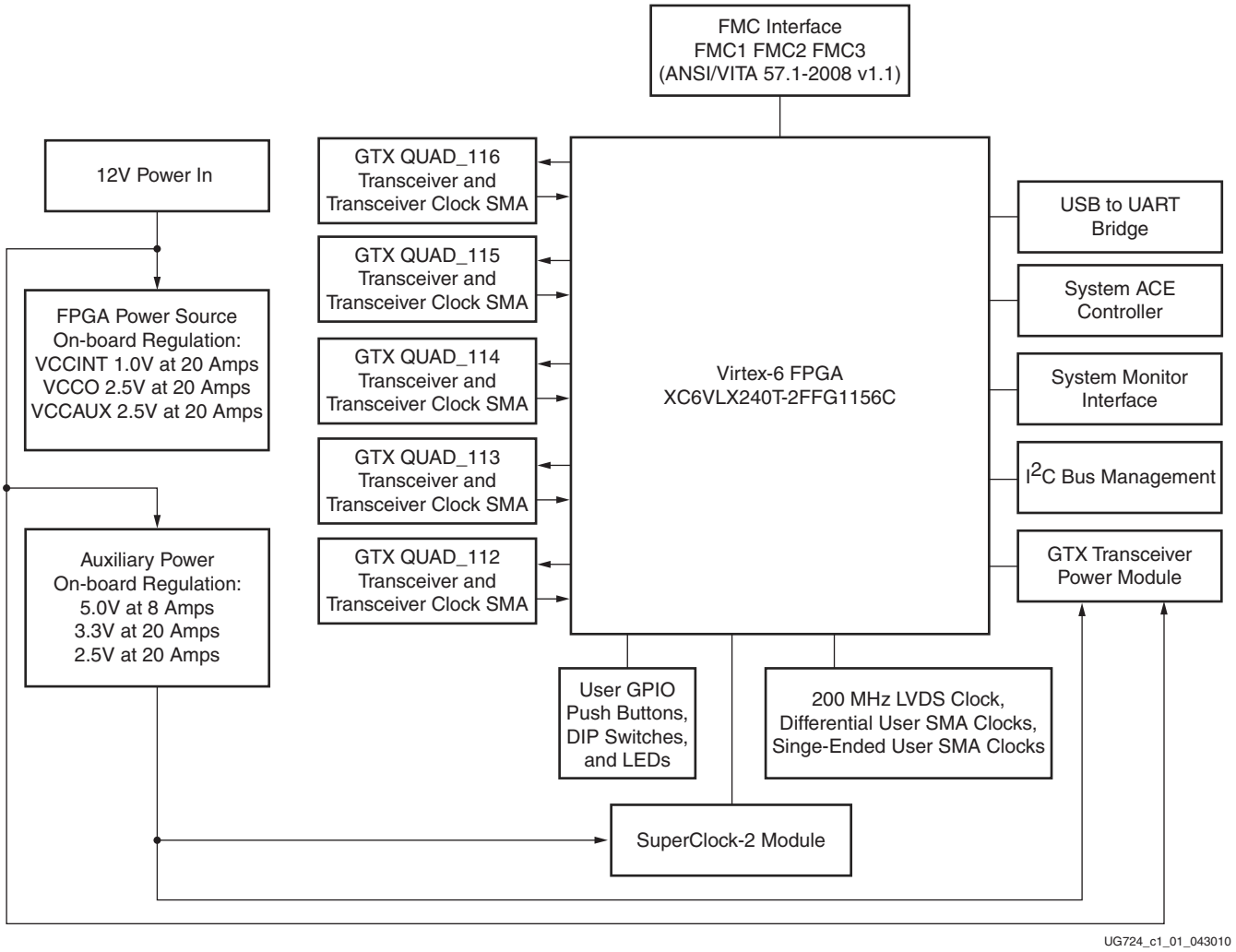
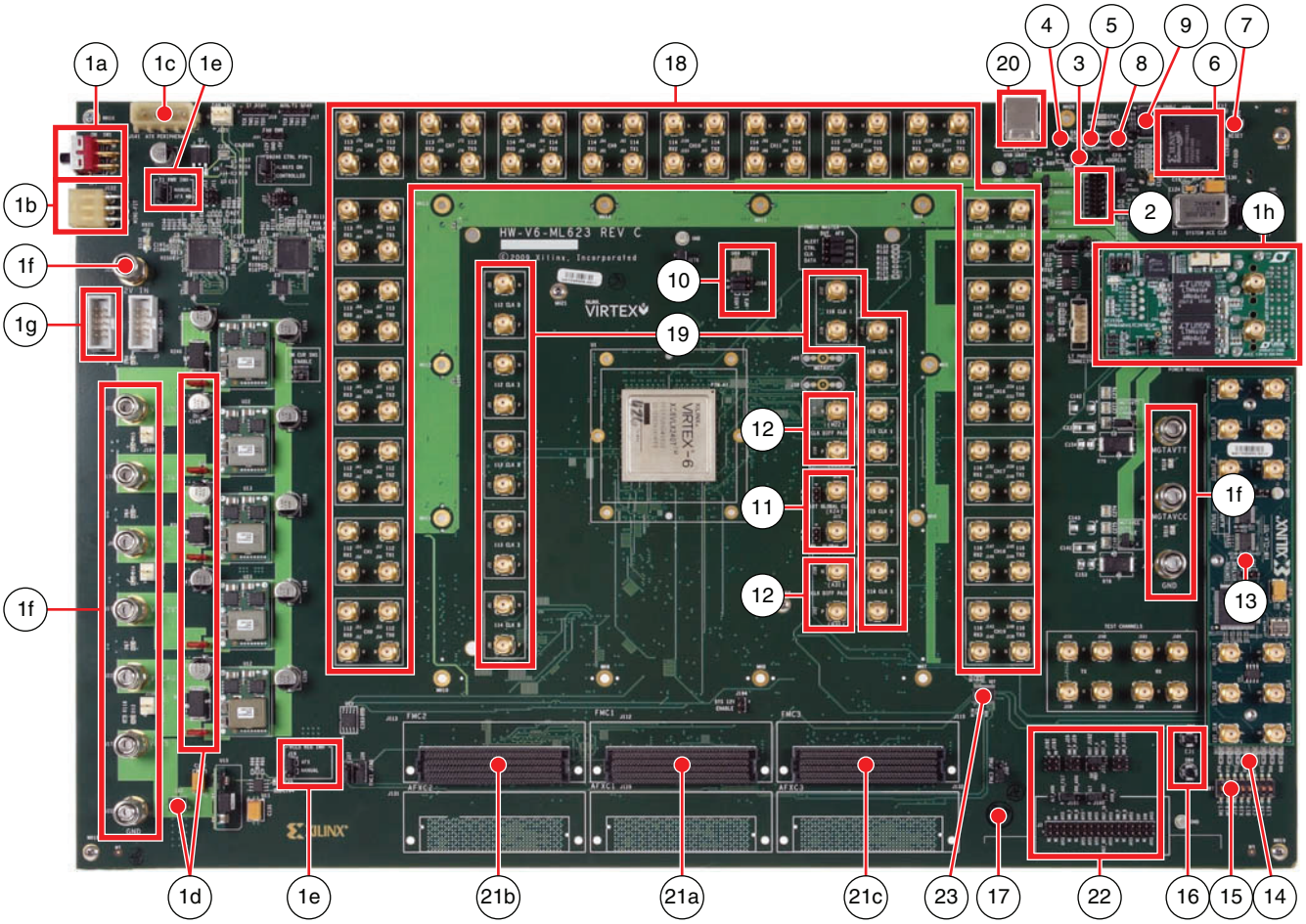


Figure 1-1: **ML623 Board Block Diagram**

Detailed Description

Figure 1-2 shows the ML623 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

Note: The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.



1a	Main Power Switch (SW1)	10	200 MHz 2.5V LVDS oscillator (U7)
1b	12V Mini-Fit connector (J122)	11	Single-ended SMA global clock input (J171, J172)
1c	12V ATX connector (J141)	12	Differential SMA global clock inputs (J167, J166, J169, J170)
1d	Power regulation jumpers (J30, J31, J33, J102, J104, J105)	13	SuperClock-2 module
1e	Regulation Inhibit (J14, J19)	14	User LEDs, active High (DS10 - DS17)
1f	External power supply jacks	15	User DIP switches, active High (SW7)
1g	TI PMBus connector (J6)	16	User push buttons, active High (SW4, SW6)
1h	GTX Transceiver power supply module	17	User test I/O (J197)
2	FPGA configuration connector (J1)	18	GTX transceiver pins
3	PROG push button, active Low (SW5)	19	GTX transceiver clock input SMAs
4	DONE LED (DS6)	20	USB to UART bridge (U26)
5	INIT LED (DS20)	21a	FMC1 connector (J112)
6	System ACE controller (U25)	21b	FMC2 connector (J113)
7	System ACE reset, active Low (SW2)	21c	FMC3 connector (J115)
8	Configuration address DIP switch (SW3)	22	System Monitor
9	JTAG isolation jumpers (J22, J23, J195, J196)	23	I^2C Bus Management (U27)

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Figure 1-2: **Detailed Description of ML623 Board Components**

Power Management

Numbers 1a through 1h refer to the callouts in Figure 1-2:

1a: Main power switch (SW1)

1b: 12V Mini-Fit connector (J122)

1c: 12V ATX connector (J141)

1d: Power regulation jumpers (J30, J31, J33, J102, J104, J105)

1e: Regulation inhibit (J14, J19)

1f: External power supply jacks (J98, J173, J174, J175, J177, J178, J189, J220, J223, J227, J234)

1g: TI PMBus cable connector (J6)

1h: GTX transceiver power supply module

Board Power and Switch

The ML623 board is powered through J122 using the 12V AC adapter included with the board. J122 is a 6-pin (2 x 3) right angle Mini-Fit type connector.

Power can also be provided through:

- Connector J141 which accepts an ATX hard disk 4-pin power plug
- Jack J234 which can be used to connect to a bench-top power supply

Caution! Do NOT plug a PC ATX power supply 6-pin connector into J122 on the ML623 board. The ATX 6-pin connector has a different pinout than J122. Connecting an ATX 6-pin connector into J122 will damage the ML623 board and void the board warranty.

Caution! Do NOT apply power to J122 and connectors J141 and/or J234 at the same time. Doing so will damage the ML623 board.

The ML623 board power is turned on or off by switch SW1. When the switch is in the ON position, power is applied to the board and a green LED (DS36) illuminates.

Onboard Power Regulation

Figure 1-3 shows the onboard power supply architecture.

Note: Power regulation jumpers are not shown in Figure 1-3.

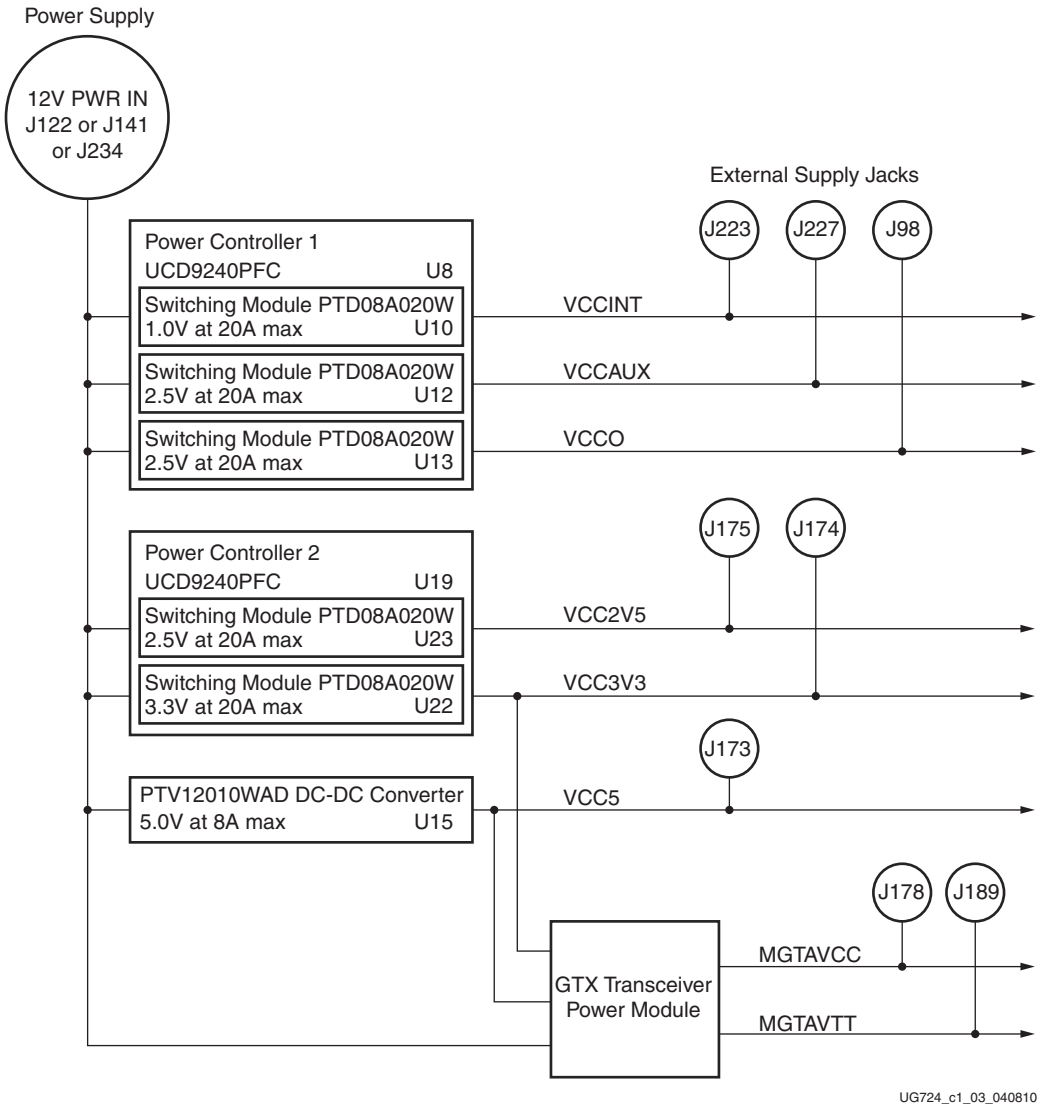

Figure 1-3: **ML623 Board Power Supply Block Diagram**

The ML623 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the core and auxiliary voltages listed in Table 1-1. The board can also be configured to use external bench power supply for each voltage. See Using External Power Sources.

Table 1-1: **Onboard Power System Devices**

Device	Reference Designator	Description	Power Rail Net Name	Typical Voltage	Power Regulation Jumper	External Supply Jack
Core voltage controller and regulators						
UCD9240PFC	U8	PMBus compliant digital PWM system controller (address = 52)				
PTD08A020W	U10	Adjustable switching regulator 20A, 0.6V to 3.6V	VCCINT	1.0V	J102	J223
PTD08A020W	U12	Adjustable switching regulator 20A, 0.6Vto 3.6V	VCCAUX	2.5V	J104	J227
PTD08A020W	U13	Adjustable switching regulator 20A, 0.6V to 3.6V	VCCO	2.5V	J105	J98
Auxiliary voltage controller and regulators						
UCD9240PFC	U19	PMBus compliant digital PWM system controller (address = 53)				
PTD08A020W	U23	Adjustable switching regulator 20A, 0.6V to 3.6V	VCC2V5	2.5V	J31	J175
PTD08A020W	U22	Adjustable switching regulator 20A, 0.6V to 3.6V	VCC3V3	3.3V	J30	J174
5V auxiliary power						
PTV12010WAD	U15	Adjustable switching regulator 8A, 1.2V to 5.5V	VCC5	5.0V	J33	J173

Using External Power Sources

The maximum output current rating for each power regulator is listed in Table 1-1. If a design exceeds this value on any power rail, power for that rail must be supplied through the external power jack using a supply capable of providing the required current.

Each power rail has a corresponding jack and jumper that is used to supply voltage to the rail using an external power supply. The jack, jumper, and regulator for each power rail is listed in Table 1-1.

> ***Caution!*** The power regulation jumper must be removed before applying external power to the power rail through its corresponding supply jack.

Disabling Onboard Power

Voltage regulators U10, U12, U13, U22, and U23 are disabled by installing a jumper across pins 2–3 of header J14. Voltage regulator U15 is disabled by installing a jumper across pins 2–3 of header J19.

Default Jumper Positions

A list of shunts and shorting plugs and their required positions for normal board operation is provided in Appendix A, Default Jumper Positions.

Monitoring Voltage and Current

Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power graphical user interface (GUI). Both onboard TI power controllers are wired to the same PMBus. The PMBus connector, J6, is provided for use with the TI USB Interface Adapter PMBus pod and associated TI GUI.

References

More information about the power system components used by the ML623 board are available from the Texas Instruments digital power website at:

http://www.ti.com/ww/en/analog/digital-power/index.html

GTX Transceiver Power Module

The GTX transceiver power module supplies MGTAVCC and MGTAVTT voltages to the FPGA GTX transceivers. Three power modules are provided with the ML623 board. Any one of the three modules can be plugged into connectors J34 and J179 in the outlined and labeled power module location shown in Figure 1-4.

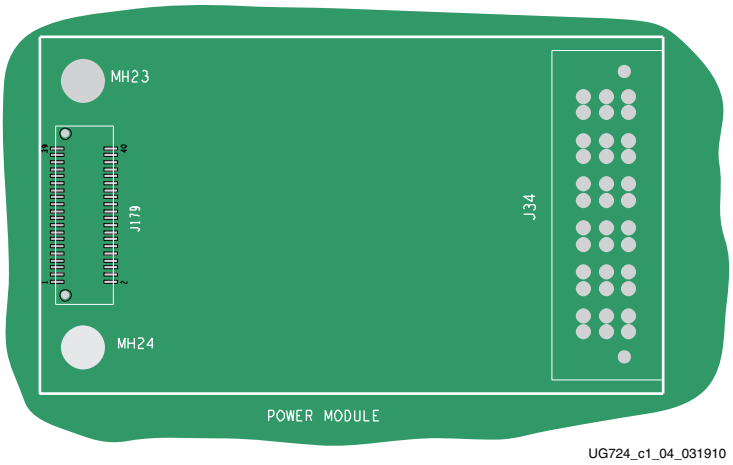

Figure 1-4: **Mounting Location, GTX Transceiver Power Module**

Table 1-2 describes the nominal voltage values for the MGTAVCC and MGTAVTT power rails. It also lists the maximum current ratings for each rail supplied by either module included with the ML623 board.

Table 1-2: **GTX Transceiver Power Module**

Power Supply Rail Net Name	Typical Voltage	Maximum Current Rating			Regulation Jumper			External Supply Jack
		Linear Technology Module	Texas Instruments Module	Intersil Module	Linear Technology Module	Texas Instruments Module	Intersil Module	
MGTAVCC	1.025V	20A	10A	10A	JP1	N/A	N/A	J178
MGTAVTT	1.2V	12A	6A	6A	JP2	N/A	N/A	J189

The GTX transceiver power rails also have corresponding input voltage jacks to supply each voltage independently from a bench-top power supply (See External Supply Jack column in Table 1-2). To supply power externally to one or both rails when the Linear

Technology Module is installed, place jumpers on JP1 and/or JP2 across pins 2–3 (OFF position).

Note: The power regulation jumper must be placed in the OFF position before connecting an external supply to its corresponding supply jack.

The Texas Instruments and Intersil modules do not have voltage regulation jumpers and *must* be removed from the board before providing external power to the GTX transceiver rails.

Caution! The Intersil module features an MGTAVCC voltage adjust header, J1. Make sure to remove any jumper across J1 before powering the board with the Intersil module installed. Failure to do so may damage the FPGA.

FPGA Configuration

[Figure 1-2, callout 2]

The FPGA is configured in JTAG mode only using one of the following options:

- Platform Cable USB
- Parallel Cable IV
- Parallel Cable III
- System ACE controller

Detailed information on the System ACE controller is available in DS080, *System ACE CompactFlash Solution*.

The FPGA is configured through one of the aforementioned cables by connecting the cable to the download cable connector, J1.

The FPGA is configured through the System ACE controller by setting the 3-bit configuration address DIP switches (SW3) to select one of eight bitstreams stored on a CompactFlash memory card (see Configuration Address DIP Switches, page 16).

Note: The System ACE controller is bypassed when the flying wire leads or the Parallel Cable IV cable is used, causing no disruption in the JTAG chain.

The JTAG chain of the board is illustrated in Figure 1-5 (the four System ACE interface isolation jumpers described in JTAG Isolation Jumpers are not shown). Shorting pins 1–2 on header J162 automatically bypasses the FMC modules and the GTX transceiver power supply module in the chain.

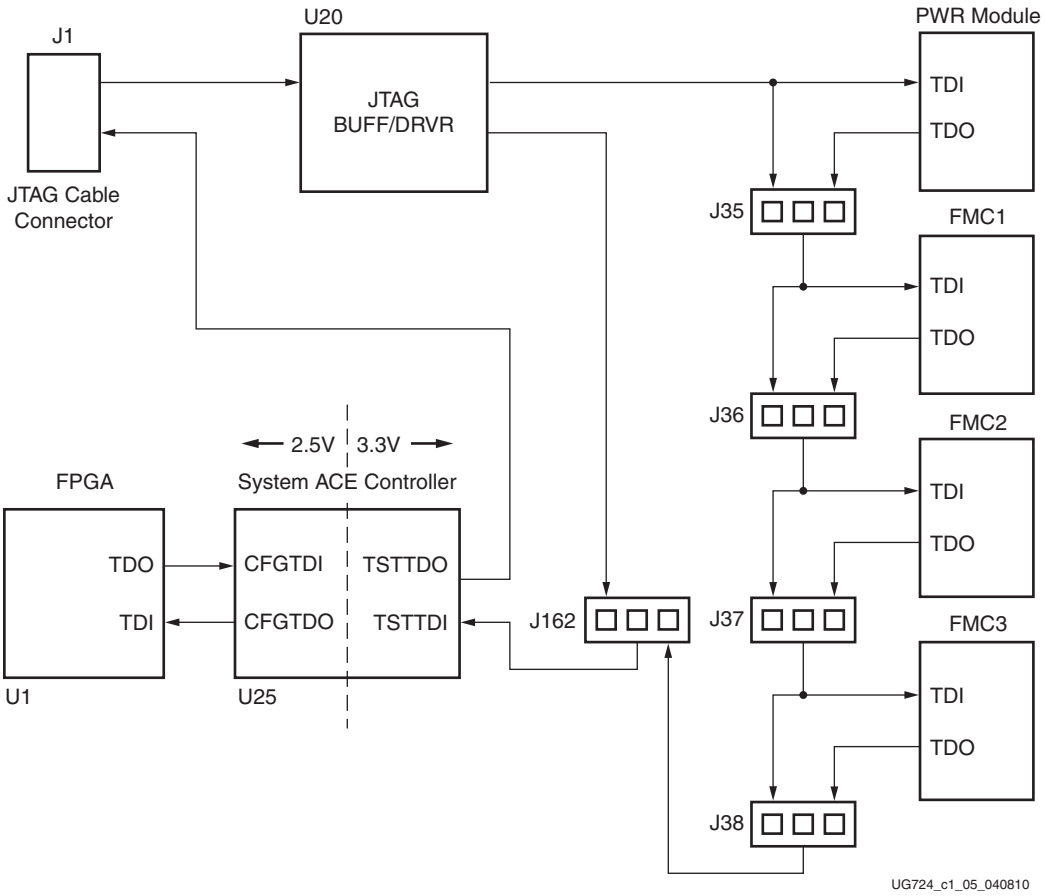

Figure 1-5: **JTAG Chain**

PROG Push Button

[Figure 1-2, callout 3]

Pressing the PROG push button (SW5) grounds the active-Low program pin of the FPGA.

DONE LED

[Figure 1-2, callout 4]

The DONE LED (DS6) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, DS6 lights indicating the FPGA is successfully configured.

INIT LED

[Figure 1-2, callout 5]

The INIT LED (DS20) lights during FPGA initialization.

System ACE Controller

[Figure 1-2, callout 6]

The onboard System ACE controller (U25) allows storage of multiple configuration files on a CompactFlash card. These configuration files can be used to program the FPGA. The CompactFlash card connects to the CompactFlash card connector (U24) located directly below the System ACE controller on the back side of the board.

System ACE Controller Reset

[Figure 1-2, callout 7]

Pressing push button SW2 (RESET) resets the System ACE controller. Reset is an active-Low input.

Configuration Address DIP Switches

[Figure 1-2, callout 8]

DIP switch SW3 selects one of the eight configuration bitstream addresses in the CompactFlash memory card. The switch settings for selecting each address are shown in Table 1-3.

Table 1-3: **SW3 DIP Switch Configuration**

Address	ADR2	ADR1	ADR0
0	O(1)	O	O
1	O	O	C(2)
2	O	C	O
3	O	C	C
4	C	O	O
5	C	O	C
6	C	C	O
7	C	C	C

Notes:

1. O indicates the open switch position (logic 0).
2. C indicates the closed switch position (logic 1).

JTAG Isolation Jumpers

[Figure 1-2, callout 9]

The group of four 2-pin headers shown in Figure 1-6 provide the option to isolate the FPGA JTAG interface from the System ACE controller by removing the shunts from all four headers. The FPGA JTAG interface can also be driven directly from these headers by attaching the flying wire JTAG cable to pin 2 of each header. Figure 1-6 shows a more detailed representation of the isolation jumpers as part of the broader JTAG chain in Figure 1-5.

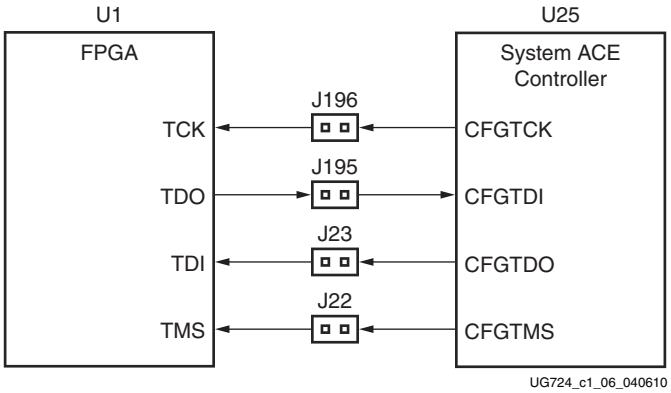

Figure 1-6: **JTAG Isolation Jumpers**

Table 1-4 indicates the FPGA pin name associated with each jumper.

Table 1-4: **JTAG Isolation Jumpers**

Reference Designator	FPGA Pin Name
J22	TMS
J23	TDI
J195	TDO
J196	TCK

200 MHz 2.5V LVDS Oscillator

[Figure 1-2, callout 10]

The ML623 board has one 2.5V LVDS differential 200 MHz oscillator (U7) connected to the FPGA global clock inputs. Table 1-5 lists the FPGA pin connections to the LVDS oscillator. The 200 MHz differential clock is enabled by placing two shunts (P, N) across J188 header pins 1–3 and 2–4 (LVDS).

Table 1-5: **LVDS Oscillator Global Clock Connections**

FPGA Pin	Net Name	U7 Pin
J9	IO_LVDS_CLK_P	4
H9	IO_LVDS_CLK_N	5

Single-Ended SMA Global Clock Inputs

[Figure 1-2, callout 11]

The ML623 board provides two single-ended clock input SMA connectors that can be used for connecting to an external function generator. The FPGA clock pins are connected to the SMA connectors as shown in Table 1-6.

To use these clock inputs, remove jumpers across AFX SEL headers J186 and J187.

Table 1-6: **Single-Ended SMA Clock Connections**

FPGA Pin	Net Name	SMA Connector
H28	CLK_A	J171
K24	CLK_B	J172

Differential SMA Global Clock Inputs

[Figure 1-2, callout 12]

The ML623 board provides two pairs of differential SMA transceiver clock inputs that can be used for connecting to an external function generator. The FPGA clock pins are connected to the SMA connectors as shown in Table 1-7.

Table 1-7: **Differential SMA Clock Connections**

FPGA Pin	Net Name	SMA Connector
B31	CLK_DIFF_A_P	J167
A31	CLK_DIFF_A_N	J168
L23	CLK_DIFF_B_P	J169
M22	CLK_DIFF_B_N	J170

SuperClock-2 Module

[Figure 1-2, callout 13]

The SuperClock-2 module connects to the clock module interface connector (J32) and provides a programmable, low-noise clock source for the ML623 board. The clock module maps to FPGA I/O by way of 24 control pins, 3 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-8 shows the FPGA I/O mapping for the SuperClock-2 module interface. The ML623 board also supplies 5V, 3.3V, and 2.5V input power to the clock module interface.

Table 1-8: **SuperClock-2 FPGA I/O Mapping**

FPGA Pin	Net Name	J32 Pin
J17	CM_LVDS1_P	1
J16	CM_LVDS1_N	3
K18	CM_LVDS2_P	9
K17	CM_LVDS2_N	11
E16	CM_LVDS3_P	17
D16	CM_LVDS3_N	19
A16	CM_GCLK_P	25
B16	CM_GCLK_N	27
C18	CM_CTRL_0	61
B18	CM_CTRL_1	63

Table 1-8: **SuperClock-2 FPGA I/O Mapping *(Cont'd)***

FPGA Pin	Net Name	J32 Pin
K22	CM_CTRL_2	65
K21	CM_CTRL_3	67
A19	CM_CTRL_4	69
A18	CM_CTRL_5	71
J22	CM_CTRL_6	73
H22	CM_CTRL_7	75
D19	CM_CTRL_8	77
E19	CM_CTRL_9	79
E21	CM_CTRL_10	81
D21	CM_CTRL_11	83
H20	CM_CTRL_12	85
H19	CM_CTRL_13	87
A20	CM_CTRL_14	89
E23	CM_CTRL_15	91
E22	CM_CTRL_16	93
B22	CM_CTRL_17	95
B21	CM_CTRL_18	97
J21	CM_CTRL_19	99
J20	CM_CTRL_20	101
C23	CM_CTRL_21	103
B23	CM_CTRL_22	105
G22	CM_CTRL_23	107
G21	CM_RST	66

User LEDs (Active High)

[Figure 1-2, callout 14]

DS10 through DS17 are eight active-High LEDs that are connected to user I/O pins on the FPGA as shown in Table 1-9. These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-9: **User LEDs**

FPGA Pin	Net Name	Reference Designator
M15	LED1	DS17
M16	LED2	DS16

Table 1-9: **User LEDs *(Cont'd)***

FPGA Pin	Net Name	Reference Designator
F15	LED3	DS15
G15	LED4	DS14
B15	LED5	DS13
A15	LED6	DS12
G16	LED7	DS11
F16	LED8	DS10

User DIP Switches (Active High)

[Figure 1-2, callout 15]

The DIP switch SW7 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-10. These pins can be used to set control pins or any other purpose determined by the user.

Table 1-10: **User DIP Switches**

FPGA Pin	Net Name	Reference Designator
M17	SW1	SW7
M18	SW2	
J19	SW3	
K19	SW4	
B17	SW5	
C17	SW6	
L18	SW7	
L19	SW8	

User Push Buttons (Active High)

[Figure 1-2, callout 16]

SW5 and SW6 are active-High user push buttons that are connected to user I/O pins on the FPGA as shown in Table 1-11. These switches can be used for any purpose determined by the user.

Table 1-11: **User Push Buttons**

FPGA Pin	Net Name	Reference Designator
E31	PB_SW1	SW6
F31	PB_SW2	SW4

User Test I/O

[Figure 1-2, callout 17]

A standard 2 x 6, 100-mil pitch header (J197) brings out 6 FPGA I/O for test purposes. Table 1-12 lists these pins.

Table 1-12: **User Test I/O**

FPGA Pin	Net Name	J197 Pin
U30	IO_L8N_SRCC_14_U30	2
U31	IO_L8P_SRCC_14_U31	4
D32	IO_L15N_16_D32	6
D31	IO_L15P_16_D31	8
K27	IO_L9N_MRCC_16_K27	10
K26	IO_L9P_MRCC_16_K26	12

GTX Transceiver Pins

[Figure 1-2, callout 18]

All FPGA GTX transceiver pins are connected to differential SMA connector pairs. The GTX transceivers are grouped into five sets of four (referred to as *Quads)* which share two differential reference clock pin pairs (Figure 1-7). The transceiver pins and their corresponding SMA connector are shown in Table 1-13.

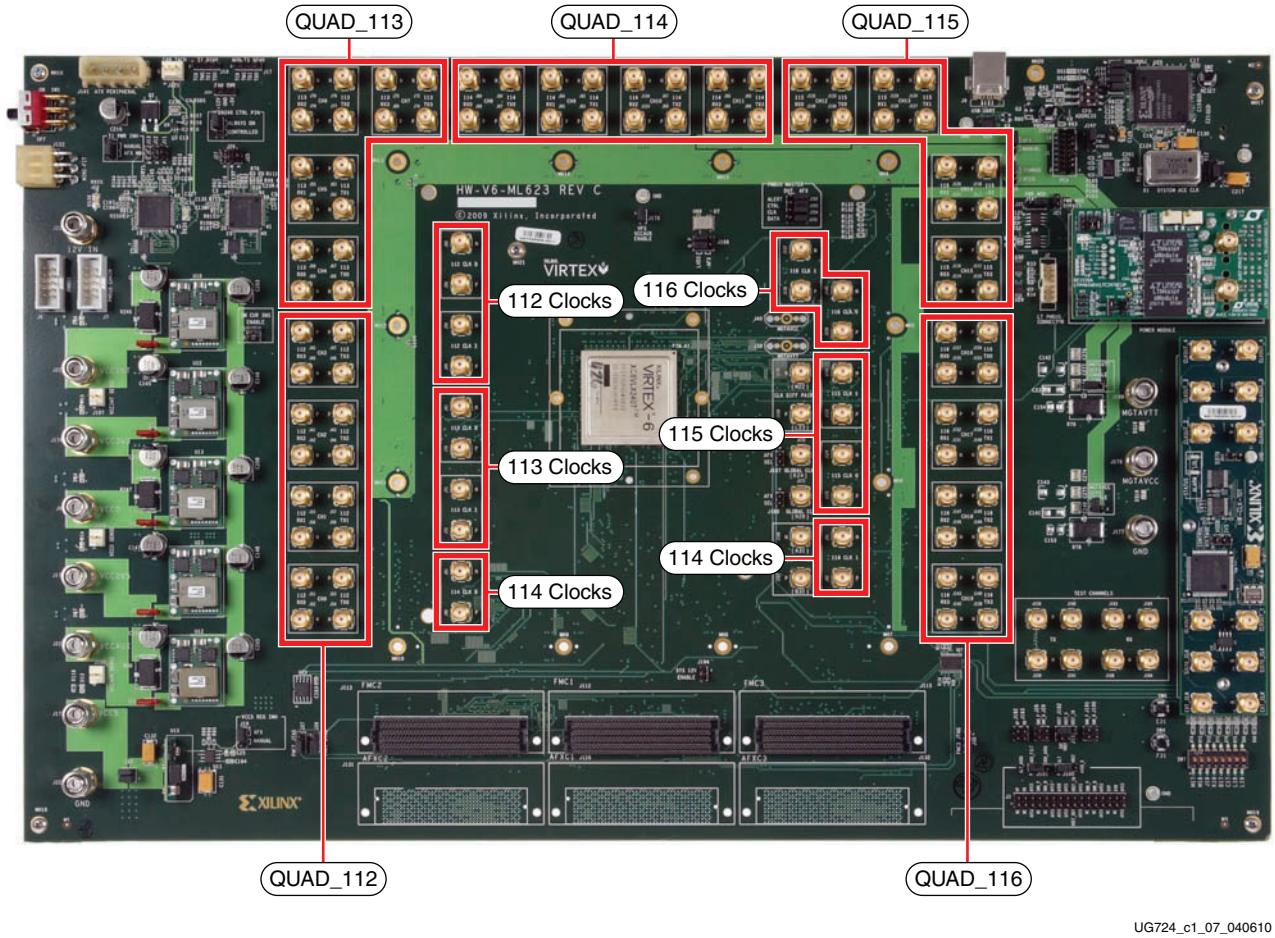

Figure 1-7: **GTX Transceiver and Reference Clock SMA Locations**

Table 1-13: **GTX Transceiver Pins**

FPGA Pin	Net Name	SMA Connector	Trace Length (Mils)
AP5	112_RX0_P	J51	7,365
AP6	112_RX0_N	J52	7,361
AP1	112_TX0_P	J53	9,861
AP2	112_TX0_N	J54	9,853
AM5	112_RX1_P	J55	6,449
AM6	112_RX1_N	J56	6,438
AN3	112_TX1_P	J57	9,079
AN4	112_TX1_N	J58	9,089
AL3	112_RX2_P	J41	5,624
AL4	112_RX2_N	J42	5,634

Table 1-13: **GTX Transceiver Pins *(Cont'd)***

FPGA Pin	Net Name	SMA Connector	Trace Length (Mils)
AM1	112_TX2_P	J43	8,185
AM2	112_TX2_N	J44	8,193
AJ3	112_RX3_P	J45	5,748
AJ4	112_RX3_N	J46	5,738
AK1	112_TX3_P	J47	7,348
AK2	112_TX3_N	J48	7,356
AG3	113_RX0_P	J68	6,550
AG4	113_RX0_N	J69	6,550
AH1	113_TX0_P	J67	6,722
AH2	113_TX0_N	J66	6,729
AF5	113_RX1_P	J65	7,531
AF6	113_RX1_N	J64	7,542
AF1	113_TX1_P	J63	6,520
AF2	113_TX1_N	J62	6,528
AE3	113_RX2_P	J79	8,300
AE4	113_RX2_N	J78	8,307
AD1	113_TX2_P	J77	7,553
AD2	113_TX2_N	J76	7,558
AC3	113_RX3_P	J80	7,166
AC4	113_RX3_N	J75	7,175
AB1	113_TX3_P	J74	6,595
AB2	113_TX3_N	J73	6,599
AA3	114_RX0_P	J88	6,112
AA4	114_RX0_N	J89	6,119
Y1	114_TX0_P	J87	5,441
Y2	114_TX0_N	J86	5,449
W3	114_RX1_P	J85	5,096
W4	114_RX1_N	J84	5,102
V1	114_TX1_P	J83	4,435
V2	114_TX1_N	J82	4,442
U3	114_RX2_P	J103	4,398
U4	114_RX2_N	J100	4,424
T1	114_TX2_P	J99	4,633

Table 1-13: **GTX Transceiver Pins *(Cont'd)***

FPGA Pin	Net Name	SMA Connector	Trace Length (Mils)
T2	114_TX2_N	J97	4,625
R3	114_RX3_P	J96	5,068
R4	114_RX3_N	J95	5,075
P1	114_TX3_P	J94	5,614
P2	114_TX3_N	J93	5,619
N3	115_RX0_P	J136	6,166
N4	115_RX0_N	J135	6,172
M1	115_TX0_P	J134	6,678
M2	115_TX0_N	J133	6,676
L3	115_RX1_P	J130	7,150
L4	115_RX1_N	J128	7,156
K1	115_TX1_P	J127	7,640
K2	115_TX1_N	J126	7,650
K5	115_RX2_P	J120	6,957
K6	115_RX2_N	J121	6,964
H1	115_TX2_P	J118	7,669
H2	115_TX2_N	J117	7,665
J3	115_RX3_P	J116	7,397
J4	115_RX3_N	J114	7,387
F1	115_TX3_P	J111	7,626
F2	115_TX3_N	J110	7,634
G3	116_RX0_P	J157	8,171
G4	116_RX0_N	J155	8,181
D1	116_TX0_P	J154	8,113
D2	116_TX0_N	J153	8,111
E3	116_RX1_P	J152	9,019
E4	116_RX1_N	J151	9,028
C3	116_TX1_P	J150	9,203
C4	116_TX1_N	J149	9,198
D5	116_RX2_P	J147	9,536
D6	116_RX2_N	J146	9,548
B1	116_TX2_P	J145	10,015
B2	116_TX2_N	J144	10,018

Table 1-13: **GTX Transceiver Pins *(Cont'd)***

FPGA Pin	Net Name	SMA Connector	Trace Length (Mils)
B5	116_RX3_P	J143	9,846
B6	116_RX3_N	J142	9,837
A3	116_TX3_P	J140	10,663
A4	116_TX3_N	J139	10,659

GTX Transceiver Clock Input SMAs

[Figure 1-2, callout 19]

The ML623 board provides differential SMA connectors that can be used for connecting an external function generator to all GTX transceiver reference clock inputs of the FPGA. The FPGA reference clock pins are connected to the SMA connectors as shown in Table 1-14.

Table 1-14: **GTX Transceiver Clock Inputs to the FPGA**

FPGA Pin	Net Name	SMA Connector
AK6	112_REFCLK0_P	J59
AK5	112_REFCLK0_N	J60
AH6	112_REFCLK1_P	J49
AH5	112_REFCLK1_N	J50
AD6	113_REFCLK0_P	J70
AD5	113_REFCLK0_N	J61
AB6	113_REFCLK1_P	J72
AB5	113_REFCLK1_N	J71
V6	114_REFCLK0_P	J90
V5	114_REFCLK0_N	J81
T6	114_REFCLK1_P	J92
T5	114_REFCLK1_N	J91
P6	115_REFCLK0_P	J125
P5	115_REFCLK0_N	J124
M6	115_REFCLK1_P	J123
M5	115_REFCLK1_N	J106
H6	116_REFCLK0_P	J156
H5	116_REFCLK0_N	J148
F6	116_REFCLK1_P	J138
F5	116_REFCLK1_N	J137