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ML628
Virtex-6 FPGA
GTX and GTH Transceiver
Characterization Board
User Guide

UG771 (v1.0.1) July 6, 2011

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/23/11	1.0	Initial Xilinx release.
07/06/11	1.0.1	Revised link in Appendix D, on page 71 to point to the version of UG806 supporting ISE software version 13.2.

Table of Contents

About This Guide

This document describes the basic setup, features, and operation of the ML628 Virtex®-6 FPGA GTX and GTH transceiver characterization board. The ML628 board provides the hardware environment for characterizing and evaluating the GTX and GTH transceivers available on the Virtex-6 XC6VHX380T-2C FFG1923 FPGA. The latest revision of this document is available online at:

http://www.xilinx.com/products/boards/ml628/reference_designs.htm

Guide Contents

This user guide contains the following chapters and appendices:

- Chapter 1, ML628 Board Features and Operation, describes the components, features, and operation of the ML628 Virtex-6 FPGA GTX and GTH transceiver characterization board.
- Appendix A, Default Jumper Positions, lists the jumpers that must be installed on the board for proper operation.
- Appendix B, VITA 57.1 FMC HPC Connector Pinout, provides a pinout reference for the FPGA mezzanine card (FMC) connector.
- Appendix C, ML628 Master UCF Listing, provides a listing of the ML628 master user constraints file (UCF).
- Appendix D, References, provides a list of references and links to related documentation.

To find additional documentation, see the Xilinx website at:

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Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *Command Line Tools User Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

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Chapter 1

ML628 Board Features and Operation

This chapter describes the components, features, and operation of the ML628 Virtex®-6 FPGA GTX and GTH transceiver characterization board. The ML628 board provides the hardware environment for characterizing and evaluating the GTX and GTH transceivers available on the Virtex-6 XC6VHX380T-2C FFG1923 FPGA. ML628 schematics, bill-of-material (BOM), layout files and reference designs are available online at:

http://www.xilinx.com/products/boards/ml628/reference_designs.htm

ML628 Board Features

- Virtex-6 XC6VHX380T-2C FFG1923 FPGA
- On-board power supplies for all necessary voltages
- Power supply jacks for optional use of external power supplies
- JTAG configuration port for use with Platform Cable USB or Parallel Cable III/IV cables
- System ACE™ controller
- Separate power modules supporting all Virtex-6 FPGA GTX and GTH transceiver power requirements
- A fixed, 200 MHz 2.5V LVDS oscillator wired to global clock inputs
- Two single-ended global clock inputs with SMA connectors
- Two pairs of differential global clock inputs with SMA connectors
- SuperClock-2 module supporting multiple frequencies
- Six Samtec BullsEye connector pads for the GTH transceivers and reference clocks
- Ten Samtec BullsEye connector pads for the GTX transceivers and reference clocks
- Power status LEDs
- General purpose DIP switches, LEDs, push buttons, and test I/O
- Two VITA 57.1 FMC HPC connectors
- USB to UART bridge
- I^2C bus
- PMBus connectivity to on-board digital power supplies
- Active cooling for the FPGA

The ML628 board block diagram is shown in Figure 1-1.

Caution! The ML628 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

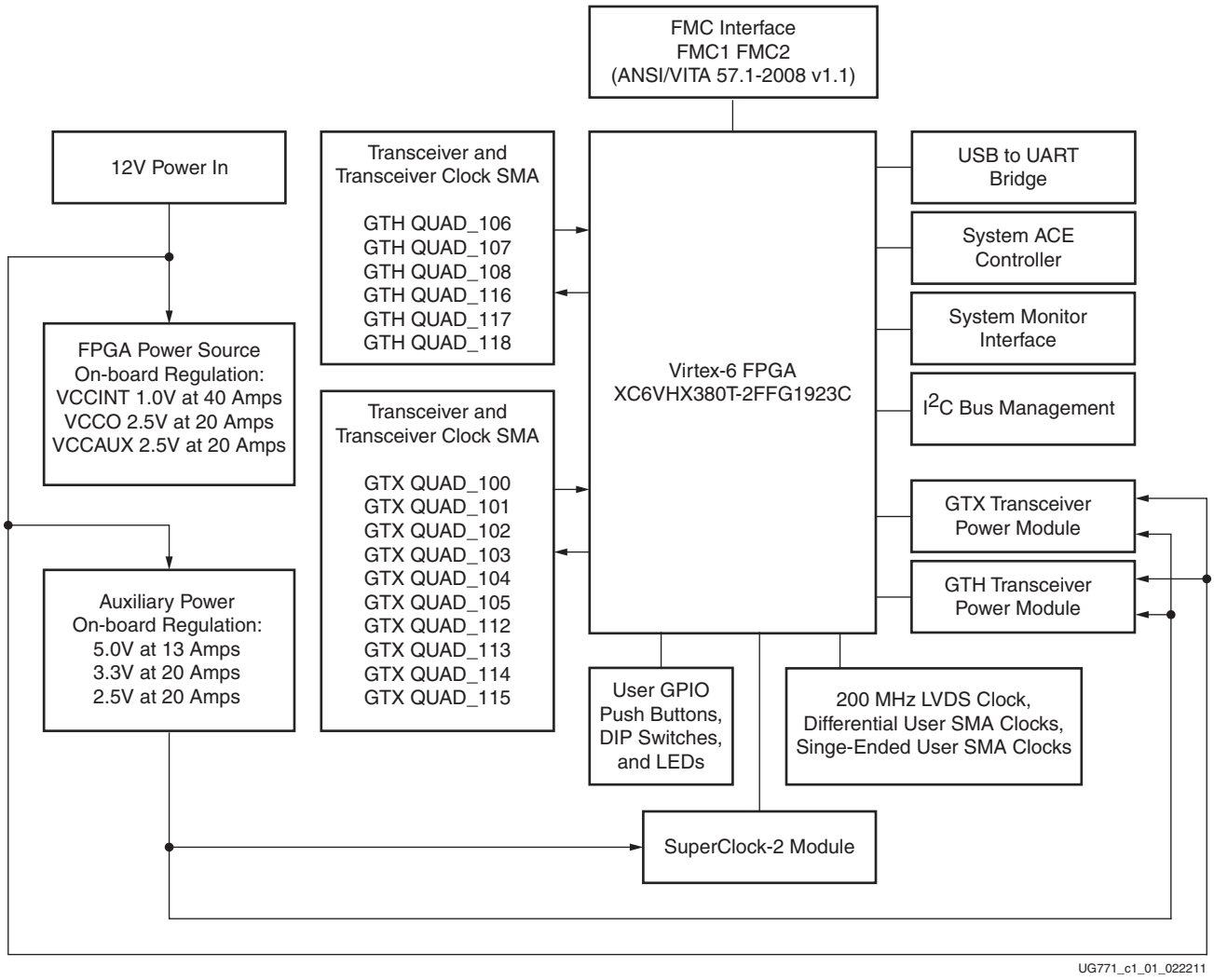
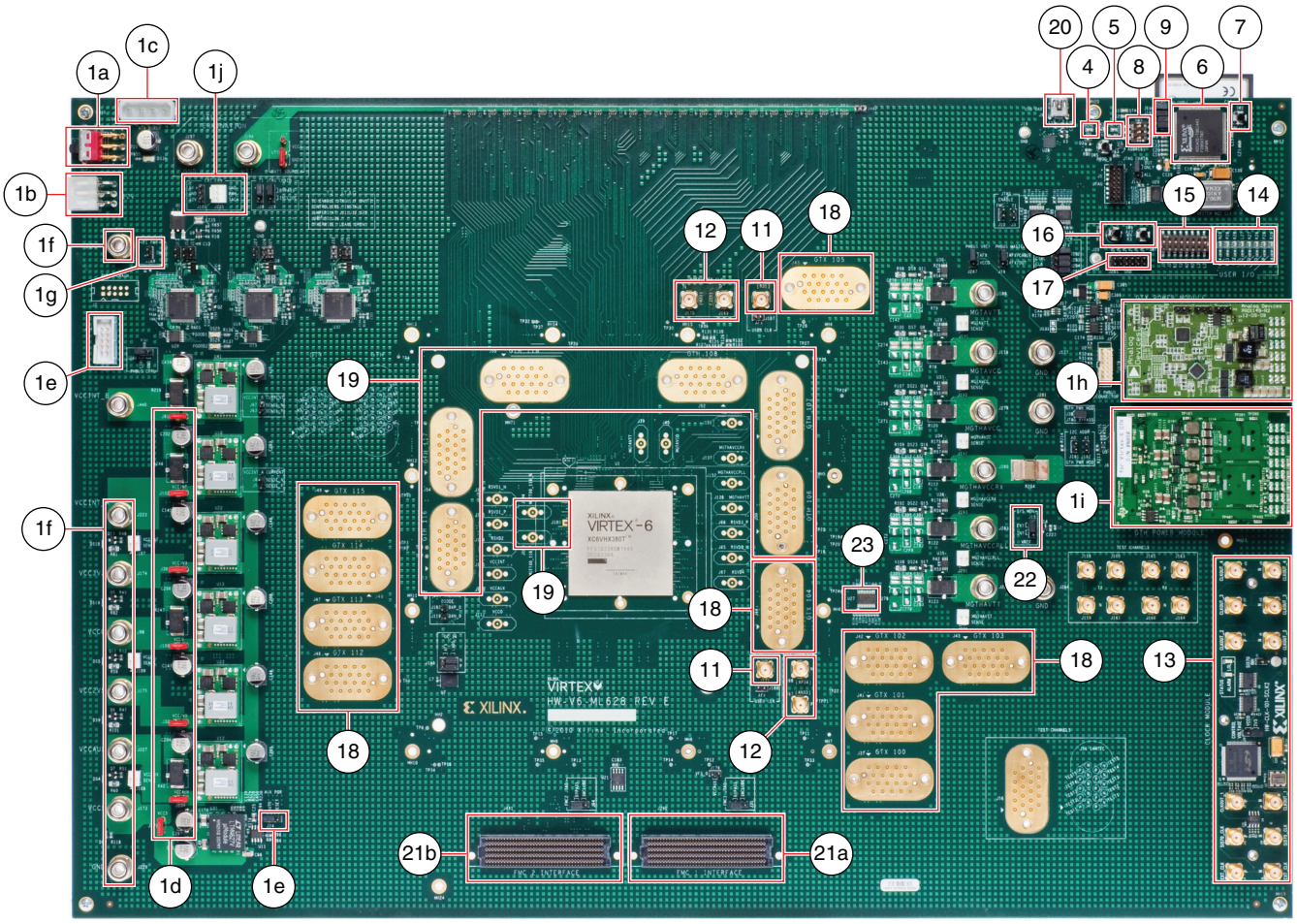


Figure 1-1: **ML628 Board Block Diagram**

Detailed Description

Figure 1-2 shows the ML628 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

Note: Figure 1-2 is for reference only and might not reflect the current revision of the board.



1a Main power switch (SW1)
1b 12V Mini-Fit connector (J122)
1c 12V ATX connector (J141)
1d Power regulation jumpers (J30, J32, J61, J102, J104, J105, J129)
1e Regulation inhibit (J289)
1f External power supply jacks
1g TI PMBus connector (J14)
1h GTX transceiver power supply module
1i GTH transceiver power supply module
1j Active cooling power connector (J221)
2 FPGA configuration connector (J1)
3 PROG_B push button, active Low (SW5)
4 DONE LED (DS6)
5 INIT LED (DS20)
6 System ACE controller (U25)
7 System ACE reset, active Low (SW2)
8 Configuration address DIP switch (SW3)
9 JTAG isolation jumpers (J22, J23, J195, J196)
10 200 MHz 2.5V LVDS oscillator (U7)
11 Single-ended SMA global clock input (J171, J172)
12 Differential SMA global clock inputs (J167 - J170)
13 SuperClock-2 module
14 User LEDs, active High (DS10 - DS17)
15 User DIP switches, active High (SW7)
16 User push buttons, active High (SW4, SW6)
17 User test I/O (J285)
18 GTX transceiver Connector Pad
19 GTH transceiver Connector Pad
20 USB to UART bridge (J9 and U26)
21a FMC1 connector (J290)
21b FMC2 connector (J441)
22 System Monitor
23 I^2C bus management (U27)

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Figure 1-2: **ML628 Board Features**

Power Management

Numbers 1a through 1j refer to the callouts in Figure 1-2:

1a: Main power switch (SW1)

1b: 12V Mini-Fit connector (J122)

1c: 12V ATX connector (J141)

1d: Power regulation jumpers (J30, J32, J61, J102, J104, J105, J129)

1e: Regulation inhibit (J289)

1f: External power supply jacks (J234, J440, J223, J174, J98, J175, J227, J173, J220)

1g: TI PMBus cable connector (J14)

1h: GTX transceiver power supply module

1i: GTH transceiver power supply module

1j: Active heatsink power connector

Board Power and Switch

The ML628 board is powered through J122 using the 12V AC adapter included with the board. J122 is a 6-pin (2 x 3) right angle Mini-Fit type connector.

Caution! Do ***NOT*** plug a PC ATX power supply 6-pin connector into J122 on the ML628 board. The ATX 6-pin connector has a different pinout than J122. Connecting an ATX 6-pin connector into J122 will damage the ML628 board and void the board warranty.

Power can also be provided through:

- Connector J141 which accepts an ATX hard disk 4-pin power plug
- Jack J234 which can be used to connect to a bench-top power supply

  Caution! Do ***NOT*** apply power to J122 and connectors J141 and/or J234 at the same time. Doing so will damage the ML628 board.

The ML628 board power is turned on or off by switch SW1. When the switch is in the ON position, power is applied to the board and a green LED (DS36) illuminates.

Onboard Power Regulation

Figure 1-3 shows the onboard power supply architecture.

Note: Power regulation jumpers are not shown in Figure 1-3.

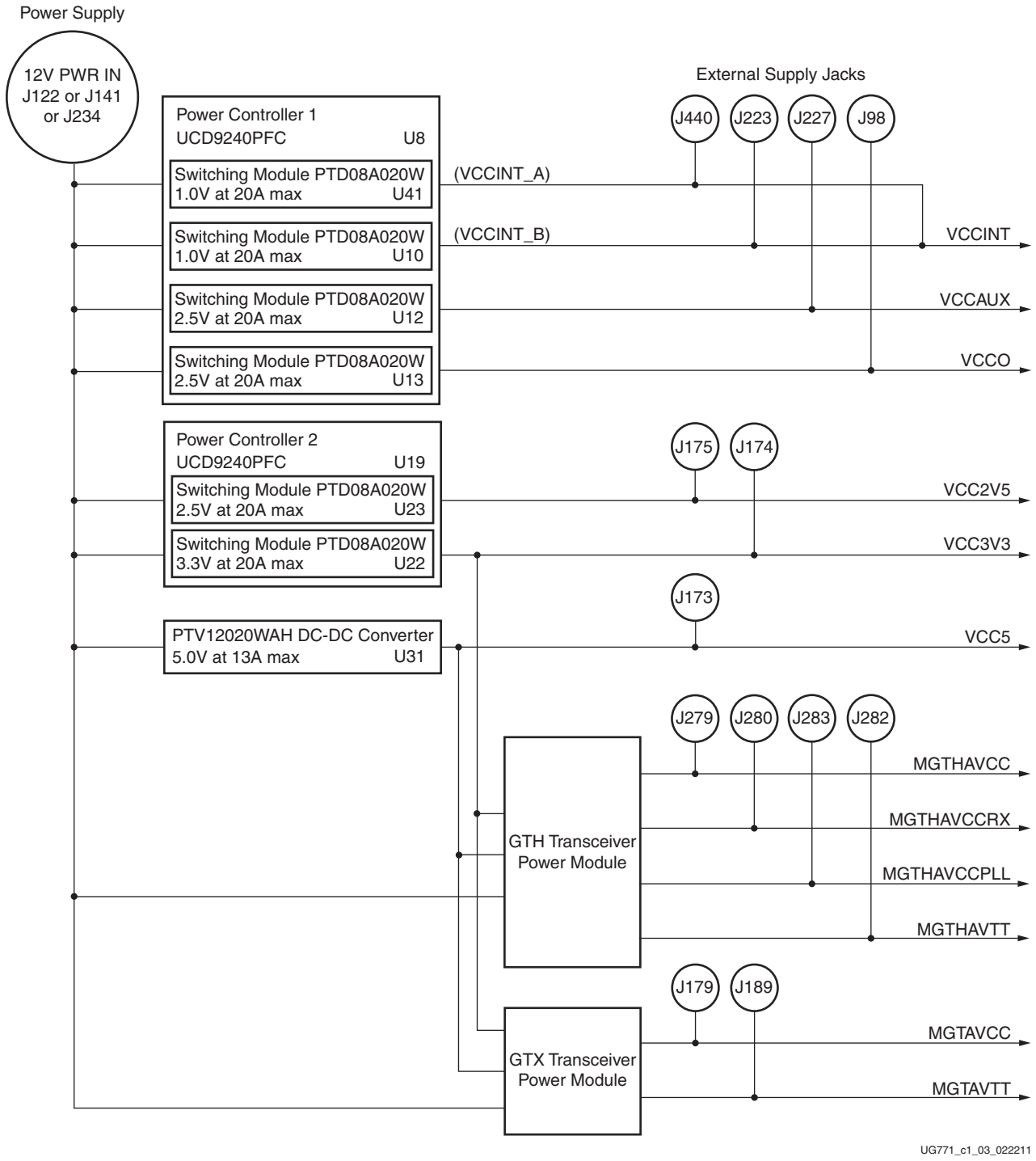

Figure 1-3: **ML628 Board Power Supply Block Diagram**

The ML628 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the core and auxiliary voltages listed in Table 1-1. The board can also be configured to use external bench power supply for each voltage. See Using External Power Sources.

Table 1-1: **Onboard Power System Devices**

Device	Reference Designator	Description	Power Rail Net Name	Typical Voltage	Power Regulation Jumper	External Supply Jack
Core voltage controller and regulators						
UCD9240PFC	U8	PMBus compliant digital PWM system controller (address = 52)				
PTD08A020W	U10	Adjustable switching regulator 20A, 0.6V to 3.6V	VCCINT[1]	1.0V	J102	J223
PTD08A020W	U41	Adjustable switching regulator 20A, 0.6V to 3.6V	VCCINT (VCCINT_B)	1.0V	J61	J440
PTD08A020W	U12	Adjustable switching regulator 20A, 0.6Vto 3.6V	VCCAUX	2.5V	J104	J227
PTD08A020W	U13	Adjustable switching regulator 20A, 0.6V to 3.6V	VCCO	2.5V	J105	J98
Auxiliary voltage controller and regulators						
UCD9240PFC	U19	PMBus compliant digital PWM system controller (address = 53)				
PTD08A020W	U23	Adjustable switching regulator 20A, 0.6V to 3.6V	VCC2V5	2.5V	J31	J175
PTD08A020W	U22	Adjustable switching regulator 20A, 0.6V to 3.6V	VCC3V3	3.3V	J30	J174
5V auxiliary power						
PTV12020WAH	U31	Switching regulator 13A, 5.0V	VCC5	5.0V	J129	J173

Notes:

1. The UCD9240PCF (U8) synchronizes the PTD power stages (U10 and U41) so that a maximum of 40A can be supplied to the VCCINT rail

Using External Power Sources

The maximum output current rating for each power regulator is listed in Table 1-1. If a design exceeds this value on any power rail, power for that rail must be supplied through the external power jack using a supply capable of providing the required current.

Each power rail has a corresponding jack and jumper that is used to supply voltage to the rail using an external power supply. The jack, jumper, and regulator for each power rail is listed in Table 1-1.

> ***Caution!*** The power regulation jumper (see Power Regulation Jumper column inTable 1-1) must be removed before applying external power to the power rail through its corresponding supply jack.
>
> ***Caution!*** The external power supply jacks have a maximum current rating of 15A.

Disabling Onboard Power

Voltage regulators U10, U12, U13, U22, U23, and U41 are disabled by installing a jumper at J289 (TI PWR INHIBIT). Voltage regulator U31 is disabled by installing a jumper across pins 2–3 of header J24 (AUX POR - RESET).

Default Jumper Positions

A list of shunts and shorting plugs and their required positions for normal board operation is provided in Appendix A, Default Jumper Positions.

Monitoring Voltage and Current

Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power graphical user interface (GUI). The three onboard TI power controllers (U8 at PMBUS address 52, U19 at PMBUS address 53, and U32 at PMBUS address 54) are wired to the same PMBus. The PMBus connector, J14, is provided for use with the TI USB Interface Adapter PMBus pod and associated TI GUI.

References

More information about the power system components used by the ML628 board are available from the Texas Instruments digital power website at:

http://www.ti.com/ww/en/analog/digital-power/index.html

GTH Transceiver Power Module

The GTH transceiver power module supplies MGTHAVCC, MGTHAVCCRX, MGTHAVTT and MGTHAVCCPLL voltages to the FPGA GTH transceivers. Two GTH power modules are provided with the ML628 board for evaluation. Either of the modules can be plugged into the connectors J6 and J197 in the outlined and labeled power module location shown in Figure 1-4.

Note: The GTH and GTX power modules have different connectors and form factors to prevent GTH modules from being connected to the GTX headers and vice versa.

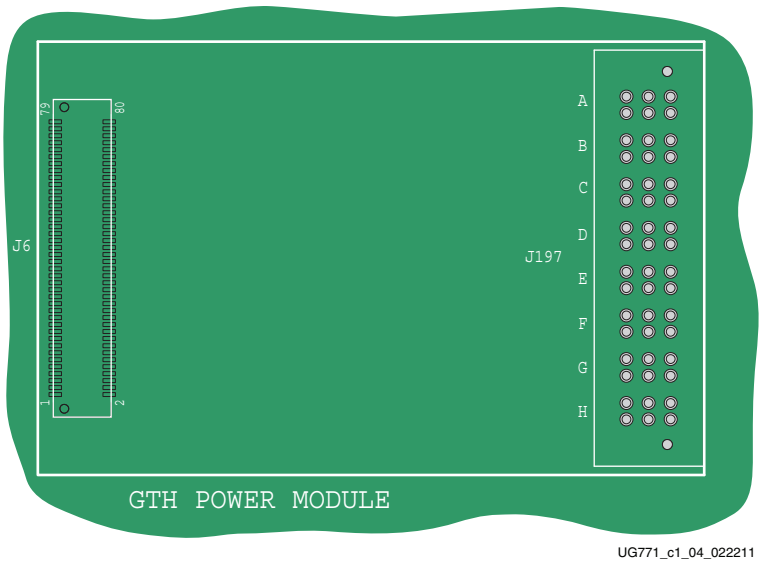

Figure 1-4: **Mounting Location, GTH Transceiver Power Module**

Table 1-2 describes the nominal voltage values for the MGTHAVCC, MGTHAVCCRX, MGTHAVTT and MGTHAVCCPLL power rails. The table also lists the maximum current ratings for each rail supplied by either module.

Table 1-2: **GTH Transceiver Power Module**

Power Supply Rail Net Name	Nominal Voltage	Maximum Current Rating
MGTHAVCC	1.1V	5.10A
MGTHAVCCRX	1.1V	3.45A
MGTHAVTT	1.2V	1.50A
MGTHAVCCPLL	1.8V	2.60A

The GTH transceiver power rails also have corresponding input voltage jacks to supply each voltage independently from a bench-top power supply. The external jacks are indicated in Table 1-3.

Caution! The GTH module ***MUST*** be removed when providing external power to the GTH transceiver rails.

Table 1-3: **GTH External Supply Jacks**

Power Supply Rail Net Name	External Supply Jack
MGTHAVCC	J279
MGTHAVCCRX	J280
MGTHAVTT	J282
MGTHAVCCPLL	J283

GTX Transceiver Power Module

The GTX transceiver power module supplies MGTAVCC and MGTAVTT voltages to the FPGA GTX transceivers. Three GTX power modules are provided with the ML628 board for evaluation. Any one of the three modules can be plugged into connectors J34 and J179 in the outlined and labeled power module location shown in Figure 1-5.

Note: The GTX and GTH power modules have different connectors and form factors to prevent GTX modules from being connected to the GTH headers and vice versa.

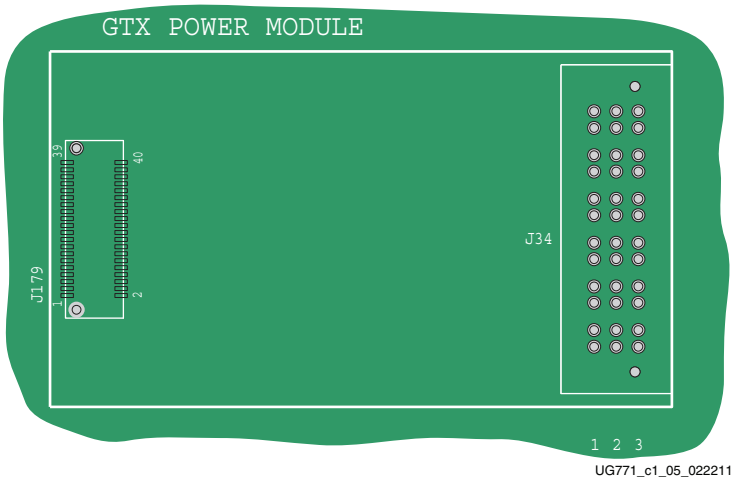

Figure 1-5: **Mounting Location, GTX Transceiver Power Module**

Table 1-4 describes the nominal voltage values for the MGTAVCC and MGTAVTT power rails. It also lists the maximum current ratings for each rail supplied by GTX modules included with the ML628 board.

Caution! The Intersil module features an MGTAVCC voltage adjust header, J1. Make sure to ***REMOVE*** any jumper across J1 before powering the board with the Intersil module installed. Failure to do so may damage the FPGA.

Table 1-4: **GTX Transceiver Power Module**

Power Supply Rail Net Name	Nominal Voltage	Maximum Current Rating
MGTAVCC	1.025V	10A
MGTAVTT	1.2V	6A

The GTX transceiver power rails also have corresponding input voltage jacks to supply each voltage independently from a bench-top power supply (The external jacks are shown in Table 1-4).

Caution! The GTX module ***MUST*** be removed when providing external power to the GTX transceiver rails.

Table 1-5: **GTX External Supply Jacks**

Power Supply Rail Net Name	External Supply Jack
MGTHAVCC	J279
MGTHAVCCRX	J280
MGTHAVTT	J282
MGTHAVCCPLL	J283

Active Heatsink Power Connector

An active heatsink is provided for the FPGA (Figure 1-6). A 12V fan is affixed to the heatsink and is powered from the 3-pin header J101.

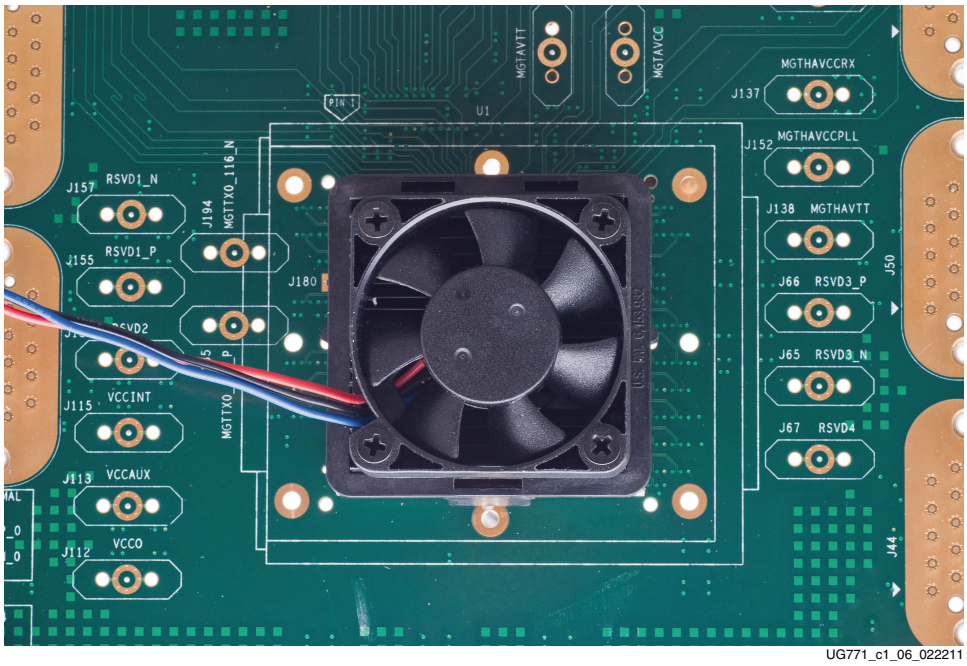

Figure 1-6: **Active Heatsink**

The fan power connections are detailed in Table 1-6 and shown in Figure 1-7.

Table 1-6: Fan Power Connections

Fan Wire	Header
Black	J101 - GND
Red	J101 - 12V
Blue	Not Connected

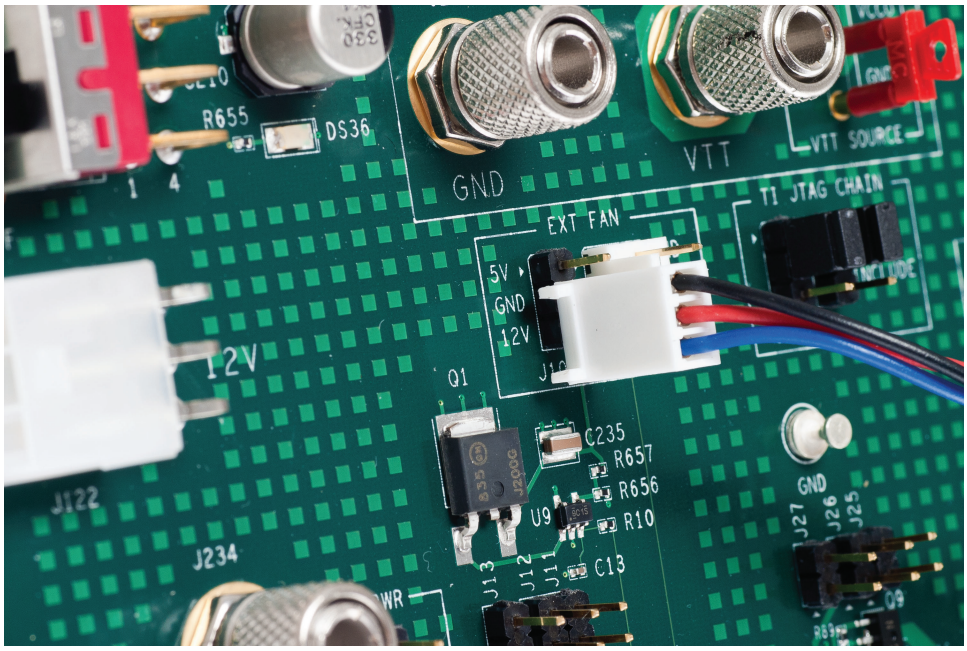

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Figure 1-7: **Fan Power Connector (J101)**

FPGA Configuration

[Figure 1-2, callout 2]

The FPGA is configured in JTAG mode only using one of the following options:

- Platform Cable USB
- Parallel Cable IV
- Parallel Cable III
- System ACE controller

Detailed information on the System ACE controller is available in DS080, *System ACE CompactFlash Solution*.

The FPGA is configured through one of the aforementioned cables by connecting the cable to the JTAG cable connector, J1.

The FPGA is configured through the System ACE controller by setting the 3-bit configuration address DIP switches (SW3) to select one of eight bitstreams stored on a CompactFlash memory card (see Configuration Address DIP Switches, page 19).

The JTAG chain of the board is illustrated in Figure 1-8 (the four System ACE interface isolation jumpers described in JTAG Isolation Jumpers are not shown). Shorting pins 1–2 on header J162 automatically bypasses the FMC modules, GTH transceiver power supply module and GTX transceiver power supply module in the chain.

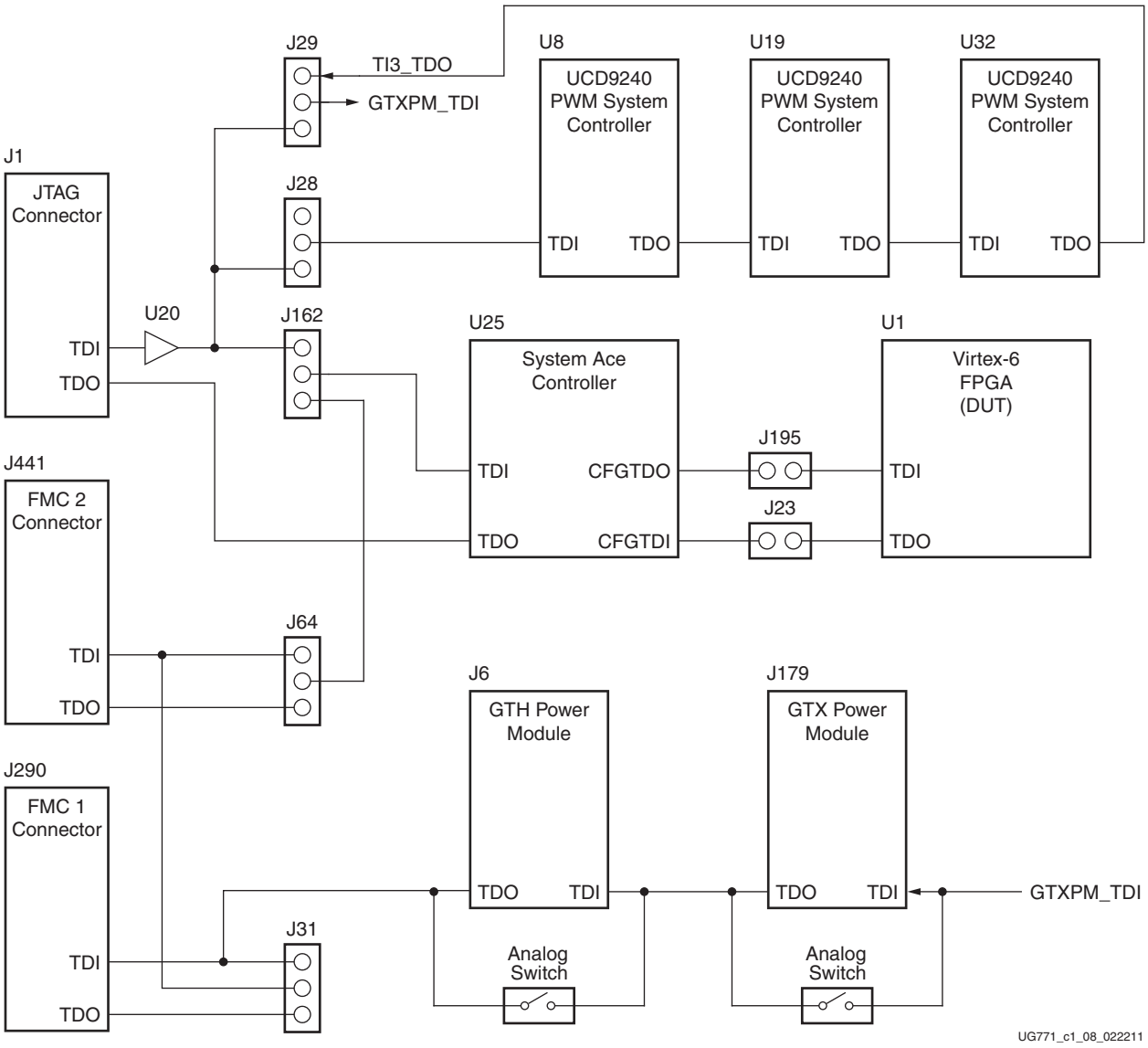

Figure 1-8: **JTAG Chain**

PROG_B Push Button

[Figure 1-2, callout 3]

Pressing the PROG push button (SW5) grounds the active-Low program pin of the FPGA.

DONE LED

[Figure 1-2, callout 4]

The DONE LED (DS6) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, DS6 lights indicating the FPGA is successfully configured.

INIT LED

[Figure 1-2, callout 5]

The INIT LED (DS20) lights during FPGA initialization.

System ACE Controller

[Figure 1-2, callout 6]

The onboard System ACE controller (U25) allows storage of multiple configuration files on a CompactFlash card. These configuration files can be used to program the FPGA. The CompactFlash card connects to the CompactFlash card connector (U24) located directly below the System ACE controller on the back side of the board.

System ACE Controller Reset

[Figure 1-2, callout 7]

Pressing push button SW2 (RESET) resets the System ACE controller. Reset is an active-Low input.

Configuration Address DIP Switches

[Figure 1-2, callout 8]

DIP switch SW3 selects one of the eight configuration bitstream addresses in the CompactFlash memory card. The switch settings for selecting each address are shown in Table 1-7.

Table 1-7: **SW3 DIP Switch Configuration**

Address	ADR2	ADR1	ADR0
0	O(1)	O	O
1	O	O	C(2)
2	O	C	O
3	O	C	C
4	C	O	O
5	C	O	C
6	C	C	O
7	C	C	C

Notes:

1. O indicates the open switch position (logic 0).
2. C indicates the closed switch position (logic 1).

JTAG Isolation Jumpers

[Figure 1-2, callout 9]

The group of four 2-pin headers shown in Figure 1-9 provide the option to isolate the FPGA JTAG interface from the System ACE controller by removing the shunts from all

four headers. The FPGA JTAG interface can also be driven directly from these headers by attaching the flying wire JTAG cable to pin 2 of each header. Figure 1-9 shows a more detailed representation of the isolation jumpers as part of the broader JTAG chain in Figure 1-8.

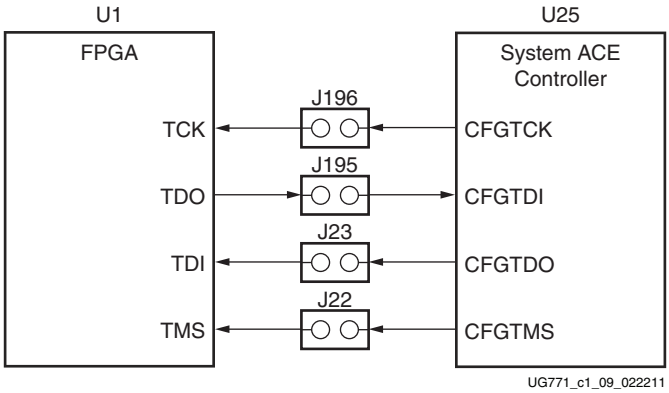

Figure 1-9: **JTAG Isolation Jumpers**

Table 1-8 indicates the FPGA pin name associated with each jumper.

Table 1-8: **JTAG Isolation Jumpers**

Reference Designator	FPGA Pin Name
J22	TMS
J23	TDI
J195	TDO
J196	TCK

200 MHz 2.5V LVDS Oscillator

[Figure 1-2, callout 10]

The ML628 board has one 2.5V LVDS differential 200 MHz oscillator (U7) connected to the FPGA global clock inputs. Table 1-9 lists the FPGA pin connections to the LVDS oscillator. The 200 MHz differential clock is enabled by placing two shunts (P, N) across J188 header pins 1–3 and 2–4 (LVDS).

Table 1-9: **LVDS Oscillator Global Clock Connections**

FPGA Pin	Net Name	U7 Pin
AK13	IIO_LVDS_GC_34_P	4
AK12	IO_LVDS_GC_34_N	5

Single-Ended SMA Global Clock Inputs

[Figure 1-2, callout 11]

The ML628 board provides two single-ended clock input SMA connectors that can be used for connecting to an external function generator. The FPGA clock pins are connected to the SMA connectors as shown in Table 1-10.

To use these clock inputs, remove jumpers across AFX SEL headers J186 and J187.

Table 1-10: **Single-Ended SMA Clock Connections**

FPGA Pin	Net Name	SMA Connector
AP33	CLK_1	J171
R31	CLK_2	J172

Differential SMA Global Clock Inputs

[Figure 1-2, callout 12]

The ML628 board provides two pairs of differential SMA transceiver clock inputs that can be used for connecting to an external function generator. The FPGA clock pins are connected to the SMA connectors as shown in Table 1-11.

Table 1-11: **Differential SMA Clock Connections**

FPGA Pin	Net Name	SMA Connector
AN33	CLK_DIFF_1_P	J167
AP33	CLK_DIFF_1_N	J168
J33	CLK_DIFF_2_P	J169
H33	CLK_DIFF_2_N	J170

SuperClock-2 Module

[Figure 1-2, callout 13]

The SuperClock-2 module connects to the clock module interface connector (J32) and provides a programmable, low-noise and low-jitter clock source for the ML628 board. The clock module maps to FPGA I/O by way of 24 control pins, 3 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-12 shows the FPGA I/O mapping for the SuperClock-2 module interface. The ML628 board also supplies 5V, 3.3V, and 2.5V input power to the clock module interface.

Table 1-12: **SuperClock-2 FPGA I/O Mapping**

FPGA Pin	Net Name	J32 Pin
B35	CM_LVDS1_P	1
B36	CM_LVDS1_N	3
C12	CM_LVDS2_P	9
C11	CM_LVDS2_N	11
BC33	CM_LVDS3_P	17
BD33	CM_LVDS3_N	19
A23	CM_GCLK_P	25
A24	CM_GCLK_N	27
G26	CM_CTRL_0	61

Table 1-12: **SuperClock-2 FPGA I/O Mapping *(Cont'd)***

FPGA Pin	Net Name	J32 Pin
G25	CM_CTRL_1	63
H23	CM_CTRL_2	65
J23	CM_CTRL_3	67
J25	CM_CTRL_4	69
K25	CM_CTRL_5	71
D26	CM_CTRL_6	73
E26	CM_CTRL_7	75
D25	CM_CTRL_8	77
E25	CM_CTRL_9	79
M25	CM_CTRL_10	81
M24	CM_CTRL_11	83
A25	CM_CTRL_12	85
B25	CM_CTRL_13	87
L25	CM_CTRL_14	89
L24	CM_CTRL_15	91
B24	CM_CTRL_16	93
C23	CM_CTRL_17	95
C24	CM_CTRL_18	97
D23	CM_CTRL_19	99
K23	CM_CTRL_20	101
L23	CM_CTRL_21	103
B26	CM_CTRL_22	105
C26	CM_CTRL_23	107
D24	CM_RST	66

User LEDs (Active High)

[Figure 1-2, callout 14]

DS10 through DS17 are eight active-High LEDs that are connected to user I/O pins on the FPGA as shown in Table 1-13. These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-13: **User LEDs**

FPGA Pin	Net Name	Reference Designator
N28	APP_LED1	DS17
P28	APP_LED2	DS16
K28	APP_LED3	DS15
L27	APP_LED4	DS14
K27	APP_LED5	DS13
K26	APP_LED6	DS12
P26	APP_LED7	DS11
R26	APP_LED8	DS10

User DIP Switches (Active High)

[Figure 1-2, callout 15]

The DIP switch SW7 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-14. These pins can be used to set control pins or any other purpose determined by the user.

Table 1-14: **User DIP Switches**

FPGA Pin	Net Name	Reference Designator
J29	USER_SW1	SW7
J28	USER_SW2	
R27	USER_SW3	
T27	USER_SW4	
H29	USER_SW5	
H28	USER_SW6	
L29	USER_SW7	
L28	USER_SW8	

User Push Buttons (Active High)

[Figure 1-2, callout 16]

SW5 and SW6 are active-High user push buttons that are connected to user I/O pins on the FPGA as shown in Table 1-15. These switches can be used for any purpose determined by the user.

Table 1-15: **User Push Buttons**

FPGA Pin	Net Name	Reference Designator
A27	USER_PB1	SW6
B27	USER_PB2	SW4

User Test I/O

[Figure 1-2, callout 17]

A standard 2 x 6, 100-mil pitch header (J285) brings out 6 FPGA I/O for test purposes. Table 1-16 lists these pins.

Table 1-16: **User Test I/O**

FPGA Pin	Net Name	J285 Pin
M26	USER_I0_1	2
N26	USER_I0_2	4
C28	USER_I0_3	6
C27	USER_I0_4	8
A29	USER_I0_5	10
A28	USER_I0_6	12

GTH Transceivers and Reference Clocks

[Figure 1-2, callout 19]

The ML628 board provides access to all GTH transceiver and reference clock pins on the FPGA as shown in Figure 1-10. The GTH transceivers are grouped into six sets of four RX-TX "lanes." Four lanes are referred to as a "Quad."

Note: Figure 1-10 is for reference only and might not reflect the current revision of the board.

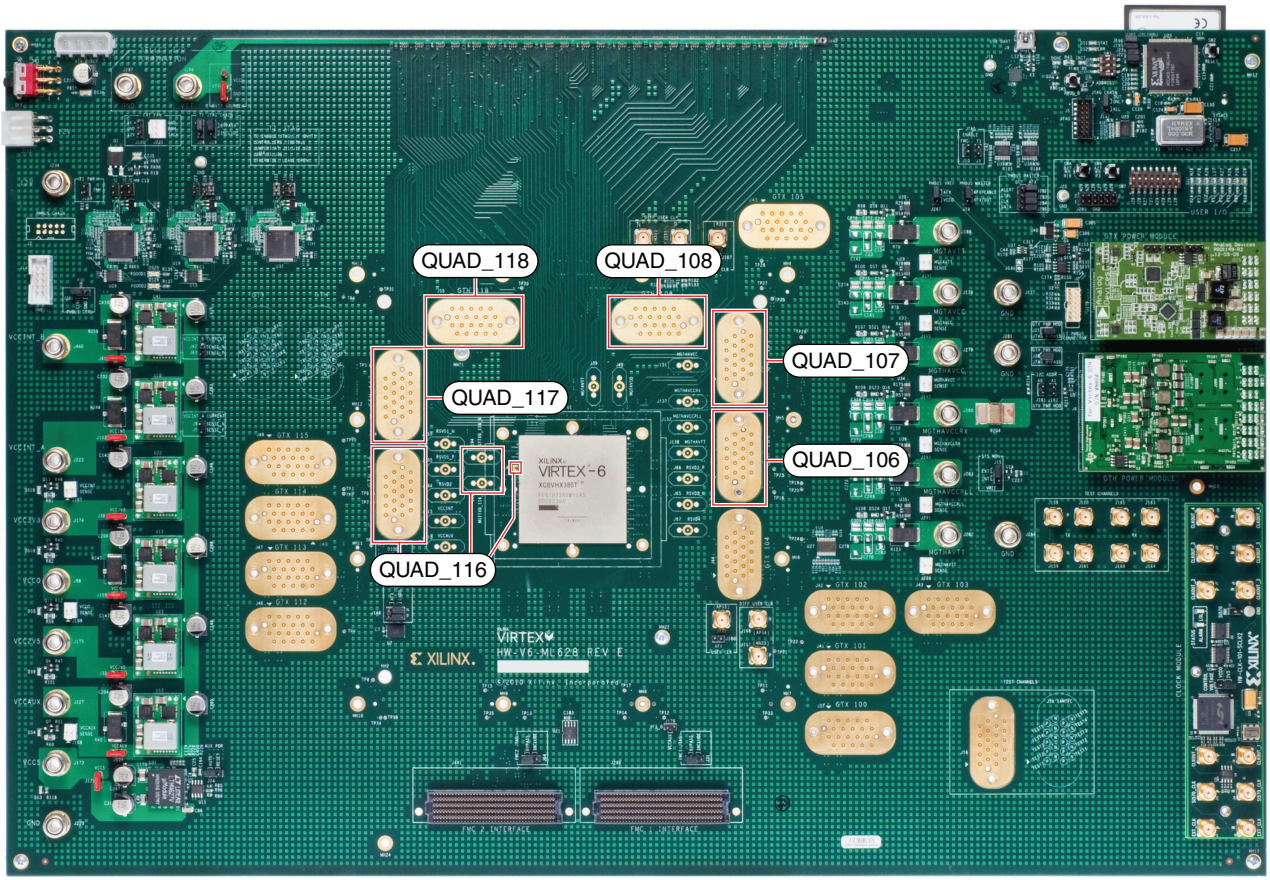

Figure 1-10: **GTH Quad Locations**

Each GTH Quad and its associated reference clock (CLK0) are routed from the FPGA to a connector pad which is designed to interface with Samtec BullsEye connectors such as the Samtec HDR-155805-01-BEYE cable assembly. Contact Samtec, Inc. for other cable assemblies . Figure 1-11 "A" shows the connector pad. Figure 1-11 "B" shows the connector pinout.

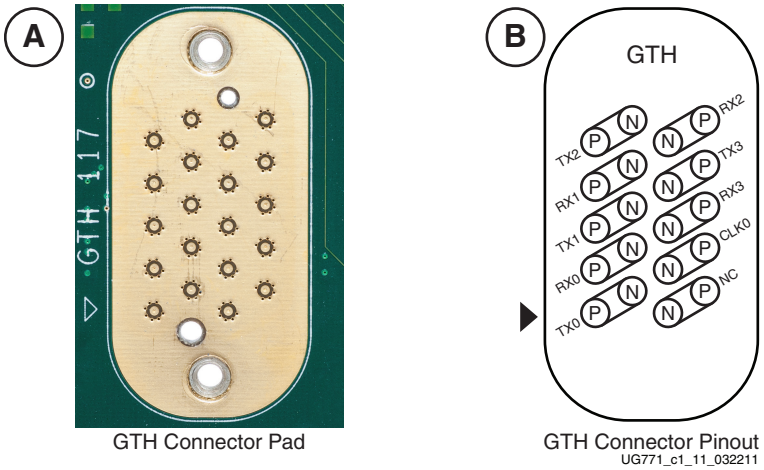

Figure 1-11: **A – GTH BullsEye Connector Pad. B – GTH BullsEye Connector Pad**