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VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board

User Guide

UG957 (v1.3) October 17, 2014

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/10/2012	1.0	Initial Xilinx release.
07/30/2013	1.1	Revised Table 1-16. Replaced the Master UCF listing with the Master XDC listing in Appendix C, Master Constraints File Listing. Updated links.
12/18/2013	1.2	Revised Table 1-7 through Table 1-12 and Table 1-17. Changed device number from XC7V485T-3 FFG1761E to XC7VX485T-3 FFG1761E and XC7V485T to XC7VX485T. Pair numbers changed in FPGA Mezzanine Card HPC Interface, page 30. Revised Figure 1-10. Changed title of Appendix C to Master Constraints File Listing. Updated references in Appendix D, Additional Resources. Updated the Declaration of Conformity link in Appendix E, Regulatory and Compliance Information.
10/17/2014	1.3	In FPGA Compatibility, page 5, “Unsupported interfaces are highlighted in this document” was removed. The number of GTX transceiver power modules supplied with the VC7203 board changed from four to three in 7 Series GTX Transceiver Power Module, page 13. The VC7203 Board XDC Listing changed. The module vendor websites changed in References, page 73, Bellnix was removed, and General Electric was added.

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Appendix E: Regulatory and Compliance Information

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Chapter 1

VC7203 Board Features and Operation

This chapter describes the components, features, and operation of the VC7203 Virtex®-7 FPGA GTX Transceiver Characterization Board. The VC7203 board provides the hardware environment for characterizing and evaluating the GTX transceivers available on the Virtex-7 XC7VX485T-3 FFG1761E FPGA. The VC7203 board schematic, bill-of-material (BOM), layout files and reference designs are available online at the Virtex-7 FPGA VC7203 Characterization Kit website.

FPGA Compatibility

The VC7203 board is provided with Virtex-7 XC7VX485T-3 FFG1761E FPGA. The board also supports all device densities (i.e., XC7VX330T, XC7V585T, XC7VX690T, XC7V1500T, and XC7V2000T devices) in the pin-compatible FFG1761, FLG1761, and FHG1761 packages. However, certain interfaces that are available in larger density devices might not be available in the XC7VX485T device (for example: GTX QUAD_111, GTX QUAD_112, FMC 3, and so on).

VC7203 Board Features

- Virtex-7 XC7VX485T-3 FFG1761E FPGA
- Onboard power supplies for all necessary voltages
- Power jacks for optional use of external power supplies
- Digilent USB JTAG programming port
- System ACE™ solution Secure Digital (SD) controller
- Power module supporting Virtex-7 FPGA GTX transceiver power requirements
- A fixed, 200 MHz 2.5V LVDS oscillator wired to multi-region clock capable (MRCC) inputs
- Two pairs of differential MRCC inputs with SMA connectors
- SuperClock-2 module supporting multiple frequencies
- Nine Samtec BullsEye connector pads for the GTX transceivers and reference clocks
- Power status LEDs
- General purpose DIP switches, LEDs, pushbuttons, and test I/O
- Three VITA 57.1 FPGA mezzanine card (FMC) high pin count (HPC) connectors
- USB-to-UART bridge
- I^2C bus
- PMBus connectivity to onboard digital power supplies

- Active cooling for the FPGA

The VC7203 board block diagram is shown in Figure 1-1.

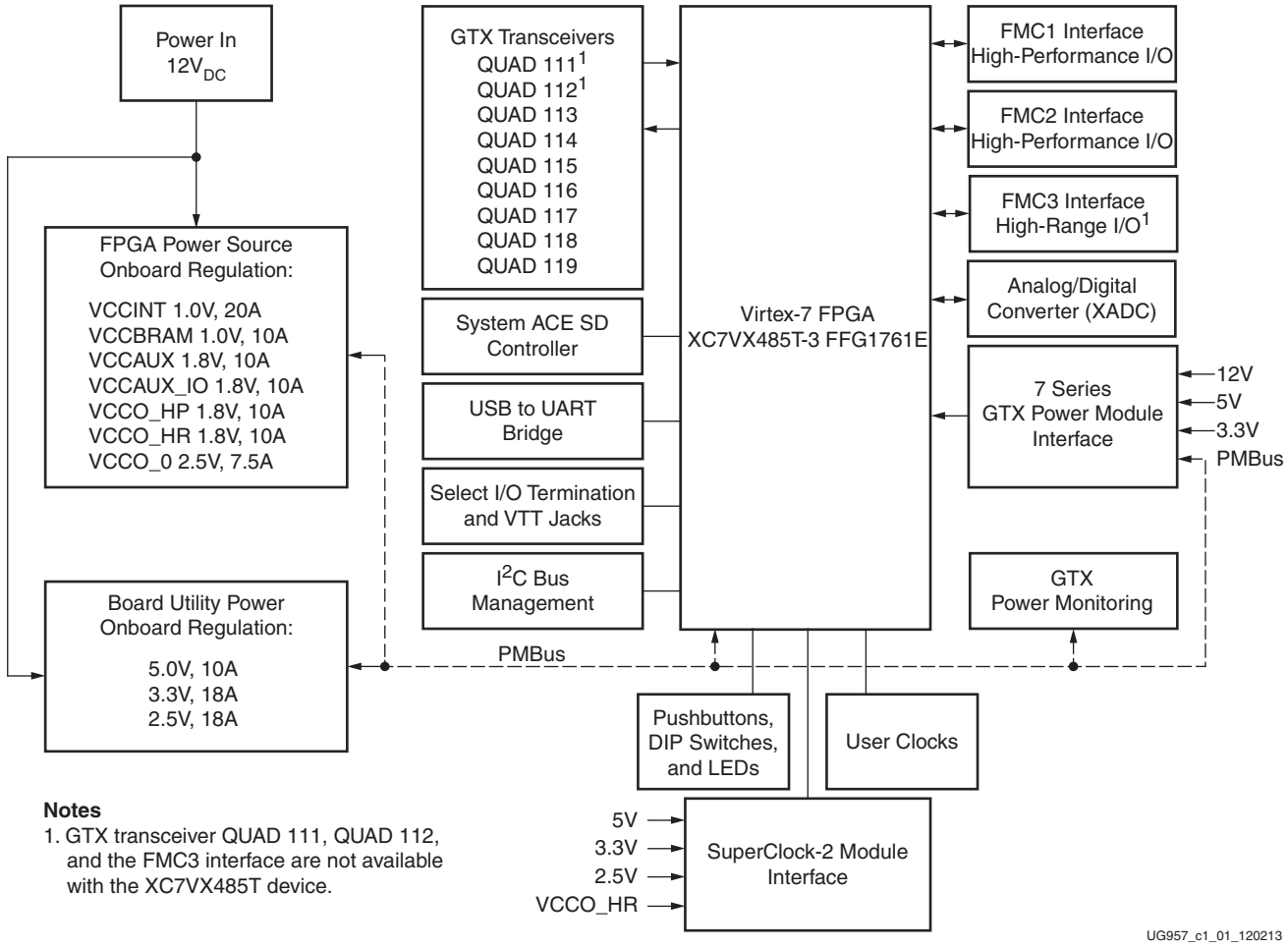


Figure 1-1: **VC7203 Board Block Diagram**

Detailed Description

Figure 1-2 shows the VC7203 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

Caution! The VC7203 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

Caution! Do not remove the rubber feet from the board. The feet provide clearance to prevent short circuits on the back side of the board.

Note: Figure 1-2 is for reference only and might not reflect the current revision of the board.

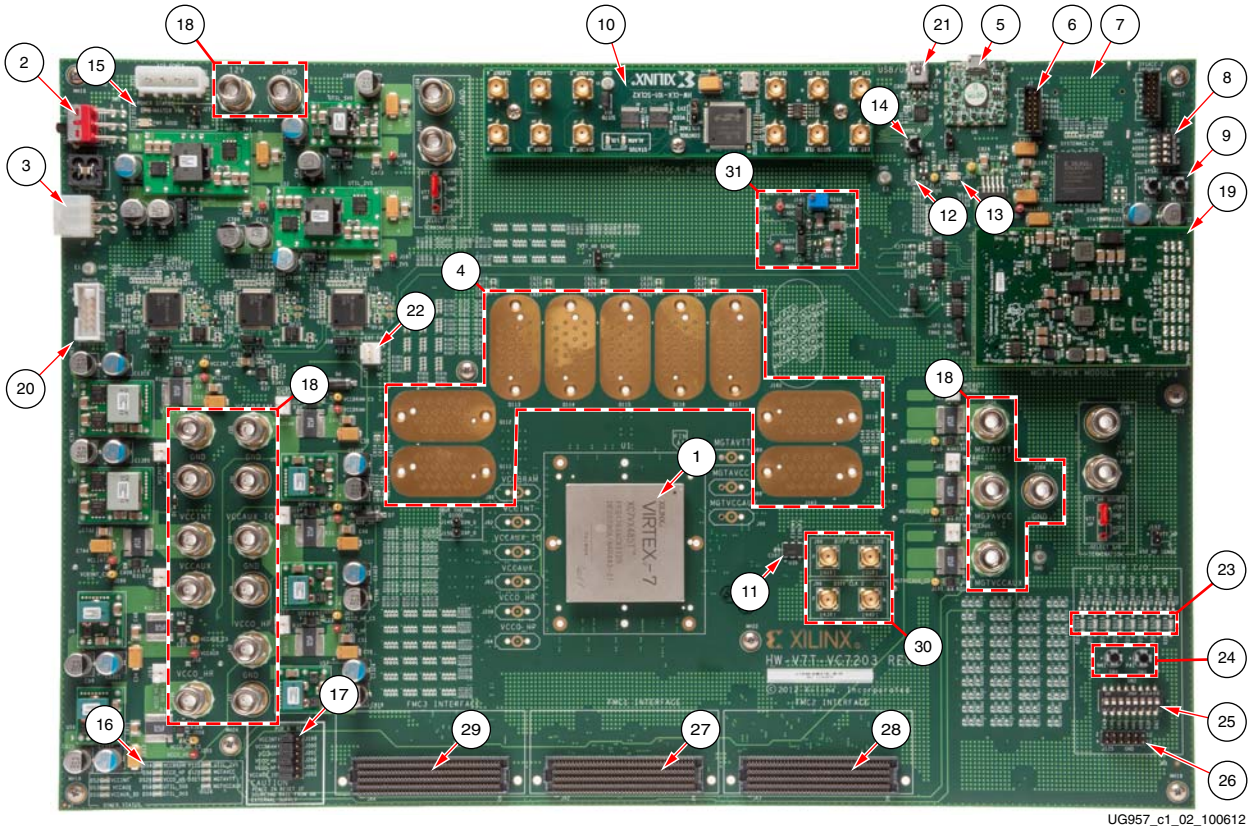


Figure 1-2: **VC7203 Board Features. Callouts Listed in Table 1-1**

Table 1-1: **VC7203 Board Feature Descriptions**

Figure 1-2 Callout	Reference Designator	Feature Description
1	U1	Virtex-7 XC7VX485T-3 FFG1761E FPGA, page 15
2	SW1	Power switch, page 9
3	J2	12V Mini-Fit connector, page 8
4	J84, J85, J86, J158, J159, J160, J161, J162, J163	GTX transceiver connector pads Q111 , Q112, Q113, Q114, Q115, Q116, Q117, Q118 and Q119, page 22
5	U8	USB JTAG connector (micro-B receptacle), page 15
6	J7	JTAG connector (alternate access for programming cables), page 15
7	J211	System ACE tool SD card connector (back-side of board), page 15
8	SW8	System ACE tool SD configuration address DIP switches, page 17
9	SW7	System ACE tool SD RESET button, page 17
10		SuperClock-2 module, page 19
11	U35	200 MHz 2.5V LVDS oscillator, page 18
12	DS21	FPGA DONE status LED, page 17
13	DS25	FPGA INIT_B status LED, page 17

Table 1-1: **VC7203 Board Feature Descriptions *(Cont'd)***

Figure 1-2 Callout	Reference Designator	Feature Description
14	SW3	FPGA PROG_B pushbutton, page 17
15	DS11	12V power status LED, page 9
16	DS2, DS3, DS4, DS5, DS6, DS8, DS9, DS10, DS26, DS27, DS28, DS29	Status LEDS for FPGA logic, transceiver and utility power,
17	J199, J200, J201 J202, J203 J204	Power regulation jumpers for onboard regulators
18	J28, J29, J31, J32, J33, J34, J35, J36, J37, J40, J104, J105, J106, J107, J177, J178, J196	External power supply jacks, page 12
19		GTX transceiver power supply module, page 13
20	J26	PMBUS connector, page 12
21	J79	Connector for USB to UART bridge (mini-B receptacle), page 29
22	J121	Power connector for active heatsink, page 13
23	DS13, DS14, DS15, DS16, DS17, DS18, DS19, DS20	User LEDs (active-High), page 20
24	SW4, SW5	User pushbuttons (active-High), page 21
25	SW2	User DIP switches (active-High), page 20
26	J125	User I/O header, page 20
27	JA2	FMC1 connector, page 30
28	JA3	FMC2 connector page 30
29	JA4	FMC3 connector1 page 30
30	J98, J99, J100, J101	SMA connectors to differential MRCC pins on FPGA, page 18
31	J141, J142, R233	Jumpers and potentiometer for XADC reference and analog supply set-up, page 44

Power Management

Board 12V Input Power

The VC7203 board receives 12V main power through J2 (callout 3, Figure 1-2) using the 12V AC adapter that ships with the board. J2 is a 6-pin (2 x 3), right angle, Mini-Fit connector.

Caution! When supplying 12V through J2, use only the power supply provided for use with this board (Xilinx part number 3800033).

Caution! Do **NOT** use a 6-pin, PC ATX power supply connector with J2. The pinout of the 6-pin, PC ATX connector is not compatible J2 and the board will be damaged if an attempt is made to power it from a PC ATX power supply connector.

12V power can also be provided through:

- Connector J131 which accepts an ATX hard drive, 4-pin, power plug
- Jacks J29 (12V) and J28 (ground) (callout 18, Figure 1-2)which can be connected to a bench-top power supply

Caution! Because jacks J29 and J28 provide no reverse polarity protection, use a power supply with a current limit set at 6A max.

Caution! Do **NOT** apply 12V power to more than a single input source. For example, do not apply power to J2 and J131 at the same time.

Power Switch

Main board power is turned on or off using switch SW1 (callout 2, Figure 1-2). When the switch is in the ON position, power is applied to the board and green LED DS11 illuminates (callout 15, Figure 1-2).

Onboard Power Regulation

Figure 1-3 shows the onboard power supply architecture.

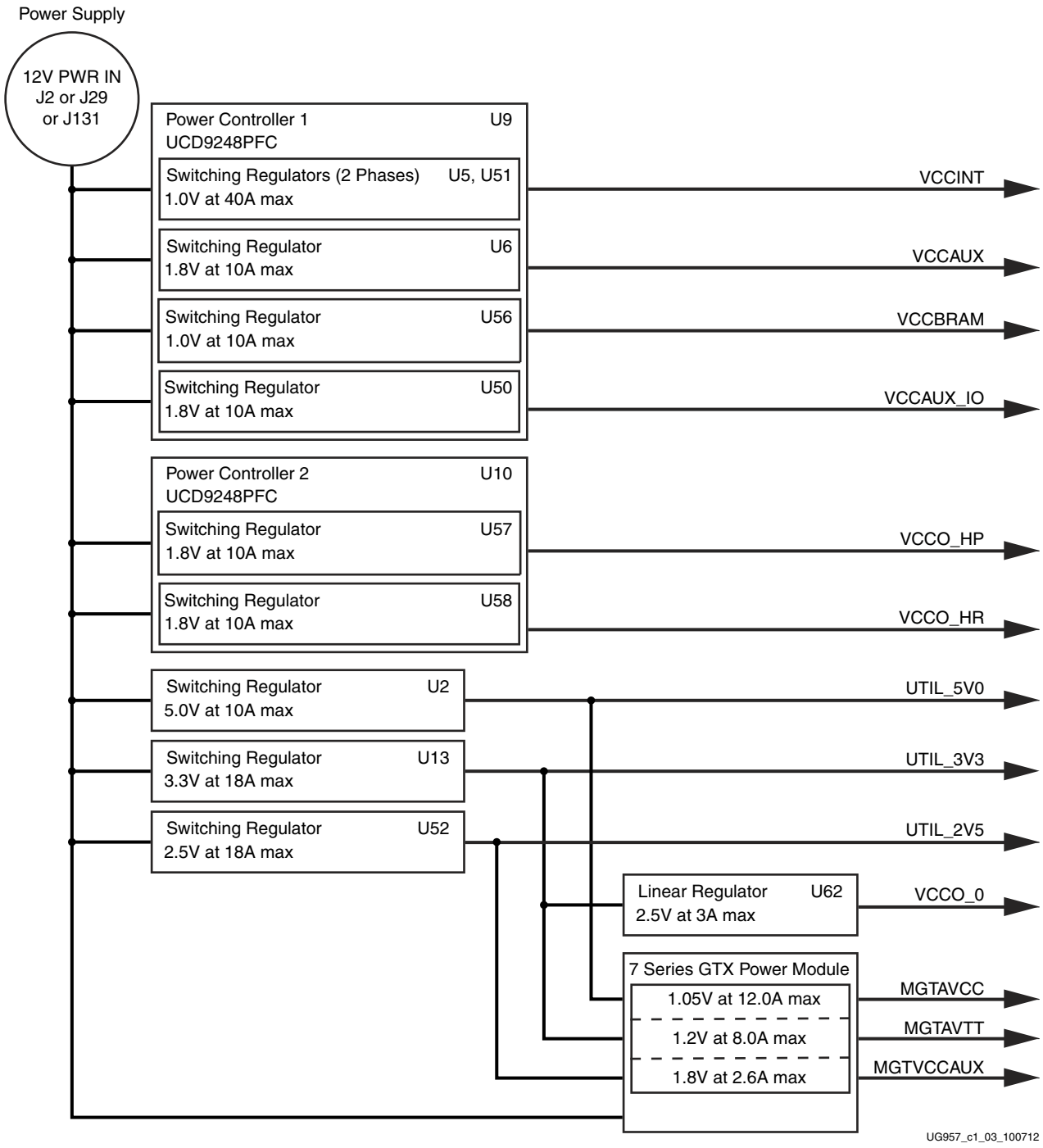


Figure 1-3: **VC7203 Board Power Supply Block Diagram**

The VC7203 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the FPGA logic and utility voltages listed in Table 1-2. The board can also be configured to use an external bench power supply for each voltage. See Using External Power Sources.

Table 1-2: **Onboard Power System Devices**

Device Part Number	Reference Designator	Description	Power Rail Net Name	Voltage
FPGA Logic				
UCD9248PFC	U9	Digital PWM system controller, PMBUS address 52		
PTD08A020W	U5, U51	Adjustable(1) switching regulator, 40A (two phases at 20A/phase), 0.6V to 3.6V	VCCINT	1.0V
PTD08A010W	U6	Adjustable(1) switching regulator, 10A, 0.6V to 3.6V	VCCAUX	1.8V
PTD08A010W	U56	Adjustable(1) switching regulator 10A, 0.6V to 3.6V	VCCBRAM	1.0V
PTD08A020W	U50	Adjustable(1) switching regulator, 40A (two phases @ 20A/phase), 0.6V to 3.6V	VCCAUX_IO	1.8V (default)
UCD9248PFC	U10	Digital PWM system controller, PMBUS address 53		
PTD08A010W	U57	Adjustable switching regulator, 10A, 0.6V to 3.6V	VCCO_HP	1.8V
PTD08A010W	U58	Adjustable switching regulator, 10A, 0.6V to 3.6V	VCCO_HR	1.8V (default)
Utility				
PTH12060W	U2	Fixed switching regulator, 10A	UTIL_5V0	5.0V
PTH12020W	U13	Fixed switching regulator, 18A	UTIL_3V3	3.3V
PTH12020W	U52	Fixed switching regulator, 18A	UTIL_2V5	2.5V
TPS75925	U62	Fixed LDO regulator, 3A	VCCO_0	2.5V
GTX Transceivers (monitoring only)				
UCD9248PFC(2)	U11	Digital PWM system controller, PMBUS address 54		
XADC(3)				
ADP123	U43	Fixed LDO regulator	VCCADC_ADP	1.8V
REF3012	U45	Fixed LDO regulator	VREF_3012	1.25V
System ACE Tool SD				
ADP123	U21	Fixed LDO regulator	VCC_1V2	1.2V

Notes:

1. The output voltages of regulators controlled by a UCD9248 can be reprogrammed using the Texas Instruments Fusion Digital Power Designer application (www.ti.com/tool/fusion_digital_power_designer). However, **extreme caution must be taken when attempting to modify any of the onboard regulators. An incorrectly programmed regulator can damage onboard components**.
2. The UCD9248PFC (U11) at Address 54 monitors MGTAVCC, MGTAVTT, and MGTVCCAUX rail voltage and current levels which can be observed in real time using the Texas Instruments Fusion Digital Power Designer application (see Monitoring Voltage and Current, page 12). Transceiver supply voltages cannot be changed from this controller.
3. For information on XADC see *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 1]

Using External Power Sources

Callout 18, Figure 1-2

Each voltage rail for the FPGA logic and GTX transceivers has an associated jack (or jacks) that can be used to provide power from an external source (Table 1-3). The jacks are binding posts that accept standard banana plugs.

Caution! Do **NOT** apply power to any of the FPGA logic power supply jacks without first disabling the associated regulator or regulators. Failing to disable the regulator can damage the board.

Each onboard FPGA Logic regulator can be disabled by using its respective Power Regulation jumper (callout 17, Figure 1-2) shown in Table 1-3. A regulator is disabled by moving its Power Regulation jumper from POR_B to RESET.

Table 1-3: **FPGA Logic and GTX Transceiver Rails**

	Power Rail Net Name	External Supply Jack(s)	Power Regulation Jumper
FPGA Logic	VCCINT	J32, J178	J199
	VCCAUX	J33	J201
	VCCBRAM	J35	J200
	VCCAUX_IO	J34	J203
	VCCO_HP	J40	J202
	VCCO_HR	J196	J204
GTX Transceiver	MGTAVCC	J105	None(1)
	MGTAVTT	J106	None(1)
	MGTVCCAUX	J107	None(1)

Notes:

1. The GTX power module must be removed before providing external power to any of the transceiver rails (see 7 Series GTX Transceiver Power Module, page 13).

Default Jumper and Switch Positions

A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.

Monitoring Voltage and Current

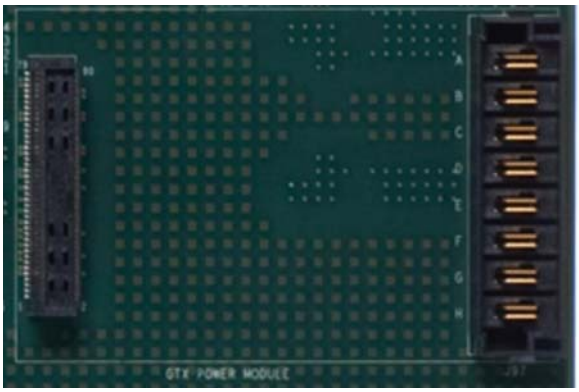
Voltage and current monitoring and control are available for FPGA logic and transceiver power rails through Texas Instruments' Fusion Digital Power graphical user interface (GUI). The three onboard TI power controllers (U9 at PMBUS address 52, U10 at PMBUS address 53, and U11 at PMBUS address 54) are wired to the same PMBus. The PMBus connector, J26 (callout 20, Figure 1-2), is provided for use with the TI USB Interface Adapter PMBus pod and associated TI GUI.

References

More information about the power system components used by the VC7203 board are available from the Texas Instruments digital power website [Ref 2].

7 Series GTX Transceiver Power Module

The 7 series GTX transceiver power module (callout 19, Figure 1-2) supplies MGTAVCC, MGTAVTT and MGTVCCAUX voltages to the FPGA GTX transceivers. Three 7 series GTX power modules from third-party vendors are provided with the VC7203 board for evaluation. Any one of the three modules can be plugged into connectors J66 and J97 in the outlined and labeled power module location shown in Figure 1-4.



UG957_C1_04_100712

Figure 1-4: **Mounting Location, 7 Series GTX Transceiver Power Module**

Table 1-4 lists the nominal voltage values for the MGTAVCC, MGTAVTT and MGTVCCAUX power rails. It also lists the maximum current rating for each rail supplied by 7 series GTX modules included with the VC7203 board.

Table 1-4: **7 Series GTX Transceiver Power Module**

GTX Transceiver Rail Net Name	Nominal Voltage	Maximum Current Rating
MGTAVCC	1.05V	12A
MGTAVTT	1.2V	8A
MGTVCCAUX	1.8V	2.6A

Each GTX transceiver rail comes with an associated jack that can be used to provide external power. These external supply jacks are shown in Table 1-3.

Caution! The 7 series GTX module **MUST** be removed when providing external power to the GTX transceiver rails.

Information about the 7 series GTX power supply modules included with the VC7203 kit is available from the vendor websites [Ref 3].

Active Heatsink Power Connector

Callout 22, Figure 1-2

An active heatsink (Figure 1-5) is provided for the FPGA. A 12V fan is affixed to the heatsink and is powered from the 3-pin friction lock header J121 (Figure 1-6).

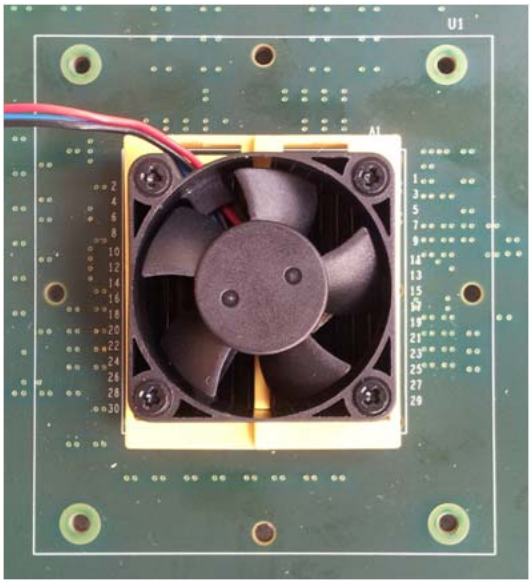


Figure 1-5: **Active FPGA Heatsink**

The fan power connections are detailed in Table 1-5:

Table 1-5: **Fan Power Connections**

Fan Wire	Header Pin
Black	J121.1 - GND
Red	J121.2 - 12V
Blue	J121.3 - NC

Figure 1-6 shows the heatsink fan power connector J121.

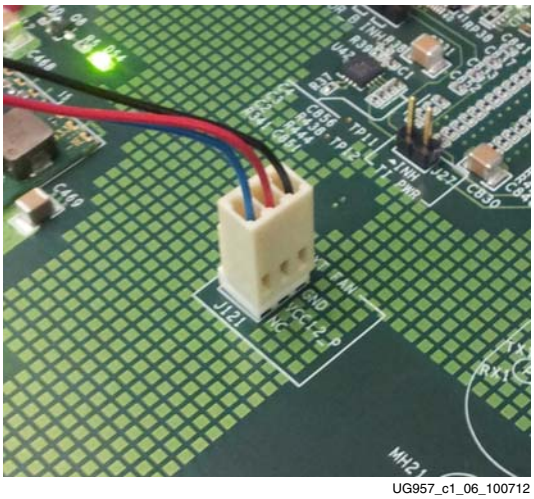


Figure 1-6: **Heatsink Fan Power Connector J121**

Virtex-7 FPGA

The VC7203 board is populated with the Virtex-7 XC7VX485T-3 FFG1761E FPGA at U1 (callout 1, Figure 1-2). For further information on Virtex-7 FPGAs, see *7 Series FPGAs Overview* (DS180) [Ref 4].

FPGA Configuration

The FPGA is configured through JTAG using one of the following options:

- USB JTAG connector (callout 5, Figure 1-2)
- System ACE tool SD (callout 7, Figure 1-2)
- JTAG cable connector (callout 6, Figure 1-2)

The VC7203 board comes with an embedded USB-to-JTAG configuration module (U8) which allows a host computer to access the board JTAG chain using a Standard A to Micro-B USB cable. Alternately, the FPGA can be configured through the System ACE tool from an SD memory card installed in J211 (see System ACE Tool SD Configuration Address DIP Switches, page 17). Finally, a JTAG connector (J7) is available to provide access to the JTAG chain using one of the Xilinx configuration cables—Platform Cable USB, Platform Cable USB II, or Parallel Cable IV (PCIV).

The JTAG chain of the board is illustrated in Figure 1-7. By default only the Virtex-7 FPGA and the System ACE SD tool controller are part of the chain (J1 jumper OFF). Installing the J1 jumper adds the FMC interfaces as well.

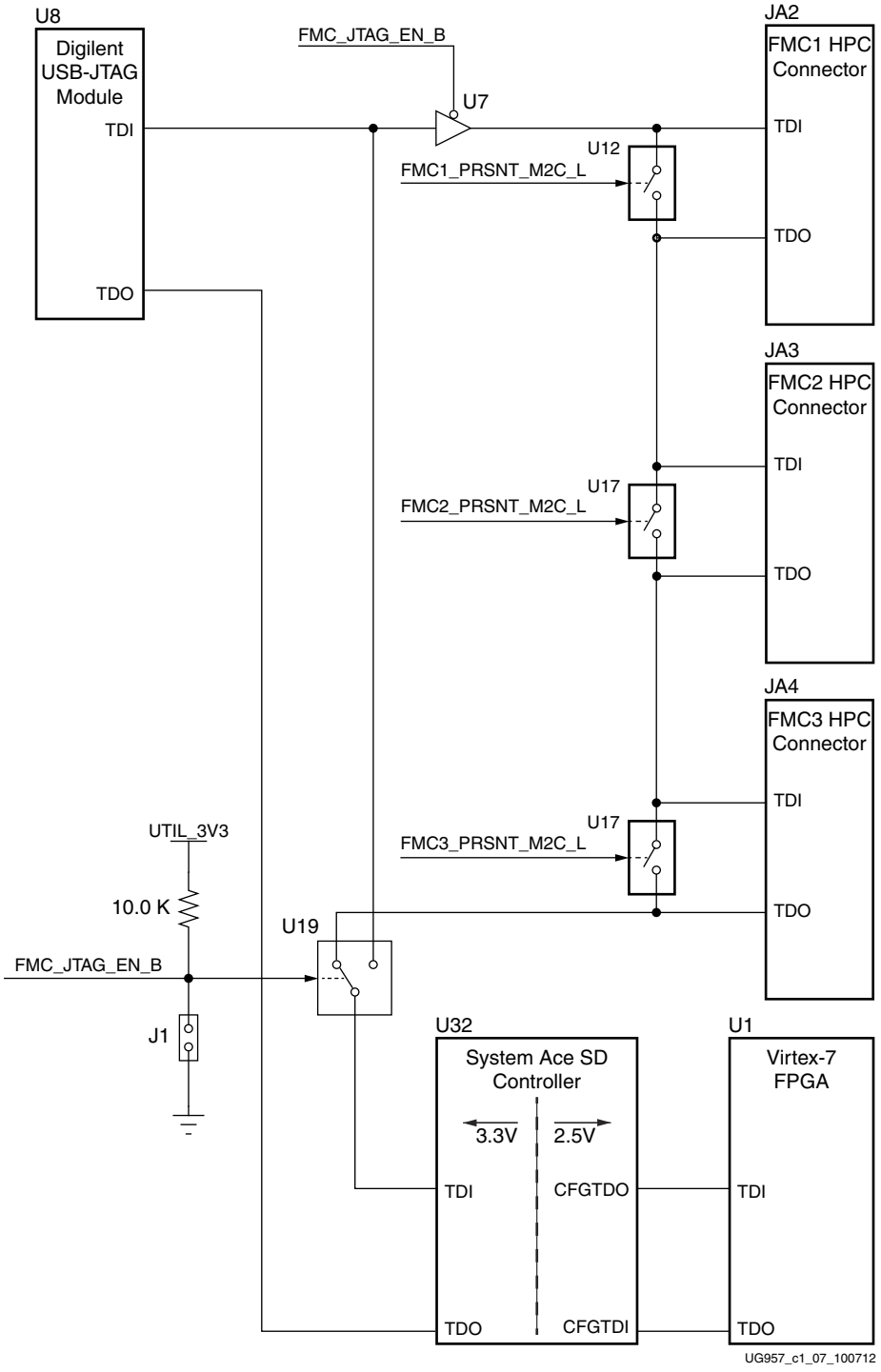


Figure 1-7: **JTAG Chain**

PROG_B Pushbutton

Pressing the PROG pushbutton SW3 (callout 14, Figure 1-2) grounds the active-Low program pin of the FPGA.

DONE LED

The DONE LED DS21 (callout 12, Figure 1-2) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, DS21 lights indicating the FPGA is successfully configured.

INIT LED

The dual-color INIT LED DS25 (callout 13, Figure 1-2) indicates the FPGA initialization status. During FPGA initialization the INIT LED illuminates RED. When FPGA initialization has completed the LED illuminates GREEN.

System ACE Tool SD Controller

The onboard System ACE tool SD controller U32 allows storage of multiple configuration files on an SD card. These configuration files can be used to program the FPGA. The SD card connects to the SD card connector J211 (callout 7, Figure 1-2) located directly below the System ACE SD controller on the back side of the board.

System ACE Tool SD Controller Reset

Pressing the SASD RESET pushbutton SW7 (callout 9, Figure 1-2) resets the System ACE tool SD controller. The reset pin is an active-Low input.

System ACE Tool SD Configuration Address DIP Switches

DIP switch SW8 shown in Figure 1-8 selects one of the eight configuration bitstream addresses in the SD memory card. A switch is in the ON position if set to the far right and in the OFF position if set to the far left. The MODE bit (switch position 4) is not used and can be set either ON or OFF. SW8 is shown in Figure 1-2 as callout 8.

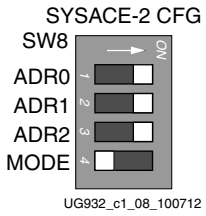


Figure 1-8: **Configuration Address DIP Switch (SW8)**

The switch settings for selecting each address are shown in Table 1-6.

Table 1-6: **SW8 DIP Switch Configuration**

Configuration Bitstream Address	ADR2	ADR1	ADR0
0	ON	ON	ON
1	ON	ON	OFF
2	ON	OFF	ON
3	ON	OFF	OFF
4	OFF	ON	ON
5	OFF	ON	OFF
6	OFF	OFF	ON
7	OFF	OFF	OFF

200 MHz 2.5V LVDS Oscillator

U35 (callout 11, Figure 1-2).

The VC7203 board has one 200 MHz 2.5V LVDS oscillator (U35) connected to multi-region clock capable (MRCC) inputs on the FPGA. Table 1-7 lists the FPGA pin connections to the LVDS oscillator.

Table 1-7: **LVDS Oscillator MRCC Connections**

FPGA (U1)				Schematic Net Name	Device (U35)		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
E19	SYSTEM CLOCK_P	Input	LVDS	LVDS_OSC_P	4	200 MHz LVDS oscillator	Output
E18	SYSTEM CLOCK_N	Input	LVDS	LVDS_OSC_N	5	201 MHz LVDS oscillator	Output

Differential SMA MRCC Pin Inputs

Callout 30, Figure 1-2.

The VC7203 board provides two pairs of differential SMA transceiver clock inputs that can be used for connecting to an external function generator. The FPGA MRCC pins are connected to the SMA connectors as shown in Table 1-8.

Table 1-8: **Differential SMA Clock Connections**

FPGA (U1)				Schematic Net Name	SMA Connector
Pin	Function	Direction	I/O Standard		
H19	USER CLOCK_1_P	Input	LVDS_25	CLK_DIFF_1_P	J99
G18	USER CLOCK_1_N	Input	LVDS_25	CLK_DIFF_1_N	J100
K39	USER CLOCK_2_P	Input	LVDS_25	CLK_DIFF_2_P	J98
K40	USER CLOCK_2_N	Input	LVDS_25	CLK_DIFF_2_N	J101

SuperClock-2 Module

Callout 10, Figure 1-2.

The SuperClock-2 module connects to the clock module interface connector (J82) and provides a programmable, low-noise and low-jitter clock source for the VC7203 board. The clock module maps to FPGA I/O by way of 24 control pins, 3 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-9 shows the FPGA I/O mapping for the SuperClock-2 module interface. The VC7203 board also supplies UTIL_5V0, UTIL_3V3, UTIL_2V5 and VCCO_HR input power to the clock module interface.

Table 1-9: **SuperClock-2 FPGA I/O Mapping**

FPGA (U1)				Schematic Net Name	J82 Pin		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
E12	Clock Recovery	Input	LVDS_25	CM_LVDS1_P	1	Clock Recovery	Output
D12	Clock Recovery	Input	LVDS_25	CM_LVDS1_N	3	Clock Recovery	Output
L12	Clock Recovery	Input	LVDS_25	CM_LVDS2_P	9	Clock Recovery	Output
L11	Clock Recovery	Input	LVDS_25	CM_LVDS2_N	11	Clock Recovery	Output
BA1	Clock Recovery	Output	LVDS	CM_LVDS3_P	17	Clock Recovery	Input
BB1	Clock Recovery	Output	LVDS	CM_LVDS3_N	19	Clock Recovery	Input
K19	Regional Clock	Input	LVDS_25	CM_GCLK_P	25	Global Clock	Output
J18	Regional Clock	Input	LVDS_25	CM_GCLK_N	27	Global Clock	Output
C19	Control I/O	In/Out	LVCMOS18	CM_CTRL_0	61	NC	—
B19	Control I/O	In/Out	LVCMOS18	CM_CTRL_1	63	NC	—
A16	Control I/O	In/Out	LVCMOS18	CM_CTRL_2	65	NC	—
A15	Control I/O	Output	LVCMOS18	CM_CTRL_3	67	DEC	Input
A20	Control I/O	Output	LVCMOS18	CM_CTRL_4	69	INC	Input
A19	Control I/O	Output	LVCMOS18	CM_CTRL_5	71	ALIGN	Input
B17	Control I/O	In/Out	LVCMOS18	CM_CTRL_6	73	NC	—
A17	Control I/O	In/Out	LVCMOS18	CM_CTRL_7	75	NC	—
B21	Control I/O	In/Out	LVCMOS18	CM_CTRL_8	77	NC	—
A21	Control I/O	In/Out	LVCMOS18	CM_CTRL_9	79	LOL	
C18	Control I/O	Output	LVCMOS18	CM_CTRL_10	81	INT_ALRM	Input
B18	Control I/O	Output	LVCMOS18	CM_CTRL_11	83	C1B	Input
D20	Control I/O	Output	LVCMOS18	CM_CTRL_12	85	C2B	Input
C20	Control I/O	Output	LVCMOS18	CM_CTRL_13	87	C3B	Input
F17	Control I/O	Output	LVCMOS18	CM_CTRL_14	89	C1A	Input
E17	Control I/O	Output	LVCMOS18	CM_CTRL_15	91	C2A	Input
D21	Control I/O	In/Out	LVCMOS18	CM_CTRL_16	93	NC	—

Table 1-9: **SuperClock-2 FPGA I/O Mapping *(Cont'd)***

FPGA (U1)				Schematic Net Name	J82 Pin		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
C21	Control I/O	Output	LVCMOS18	CM_CTRL_17	95	CS0_C3A	Input
D18	Control I/O	Output	LVCMOS18	CM_CTRL_18	97	CS1_C4A	Input
D17	Control I/O	In/Out	LVCMOS18	CM_CTRL_19	99	NC	—
F20	Control I/O	In/Out	LVCMOS18	CM_CTRL_20	101	NC	—
E20	Control I/O	In/Out	LVCMOS18	CM_CTRL_21	103	NC	—
K17	Control I/O	In/Out	LVCMOS18	CM_CTRL_22	105	NC	—
J17	Control I/O	In/Out	LVCMOS18	CM_CTRL_23	107	NC	—
J20	CM_RESET	Output	LVCMOS18	CM_RST	66	RESET_B	Input

User LEDs (Active-High)

Callout 23, Figure 1-2.

DS13 through DS20 are eight active-High LEDs that are connected to user I/O pins on the FPGA as shown in Table 1-10 These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-10: **User LEDs**

FPGA (U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	I/O Standard		
M37	User LED	Output	LVCMOS18	APP_LED1	DS19
M38	User LED	Output	LVCMOS18	APP_LED2	DS20
R42	User LED	Output	LVCMOS18	APP_LED3	DS17
P42	User LED	Output	LVCMOS18	APP_LED4	DS18
N38	User LED	Output	LVCMOS18	APP_LED5	DS16
M39	User LED	Output	LVCMOS18	APP_LED6	DS15
R40	User LED	Output	LVCMOS18	APP_LED7	DS13
P40	User LED	Output	LVCMOS18	APP_LED8	DS14

User DIP Switches (Active-High) and I/O Header

Callout 25, Figure 1-2.

The DIP switch SW2 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-11. These pins can be used to set control pins or any other purpose determined by the user. Six of the eight I/Os also map to 2 x 6 test header J125 providing external access for these pins (callout 26, Figure 1-2.).

Table 1-11: **User DIP Switches**

FPGA (U1)				Schematic Net Name	SW2 DIP Switch Pin	J125 Test Header Pin
Pin	Function	Direction	I/O Standard			
E42	User Switch	Input	LVCMOS18	USER_SW1	1	2
C40	User Switch	Input	LVCMOS18	USER_SW2	2	4
C41	User Switch	Input	LVCMOS18	USER_SW3	3	6
H40	User Switch	Input	LVCMOS18	USER_SW4	4	8
H41	User Switch	Input	LVCMOS18	USER_SW5	5	10
H39	User Switch	Input	LVCMOS18	USER_SW6	6	12
G39	User Switch	Input	LVCMOS18	USER_SW7	7	—
G41	User Switch	Input	LVCMOS18	USER_SW8	8	—

Figure 1-9 shows the user test I/O connector J125 (callout 26, Figure 1-2).

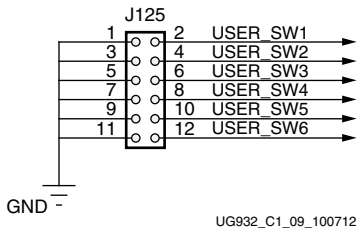


Figure 1-9: **User Test I/O**

User Pushbuttons (Active-High)

Callout 24, Figure 1-2.

SW4 and SW5 are active-High user pushbuttons that are connected to user I/O pins on the FPGA as shown in Table 1-12. These switches can be used for any purpose determined by the user.

Table 1-12: **User Pushbuttons**

FPGA (U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	I/O Standard		
P41	User Pushbutton	Input	LVCMOS18	USER_PB1	SW5
N41	User Pushbutton	Input	LVCMOS18	USER_PB2	SW4

GTX Transceivers and Reference Clocks

Callout 4, Figure 1-2.

The VC7203 board provides access to all GTX transceiver and reference clock pins on the FPGA as shown in Figure 1-10. The GTX transceivers are grouped into nine sets of four RX-TX *lanes*. Four lanes are referred to as a *Quad*.

Note: QUAD 111 and QUAD 112 do not connect to pins on the XCVX485T.

Note: Figure 1-10 is for reference only and might not reflect the current revision of the board.

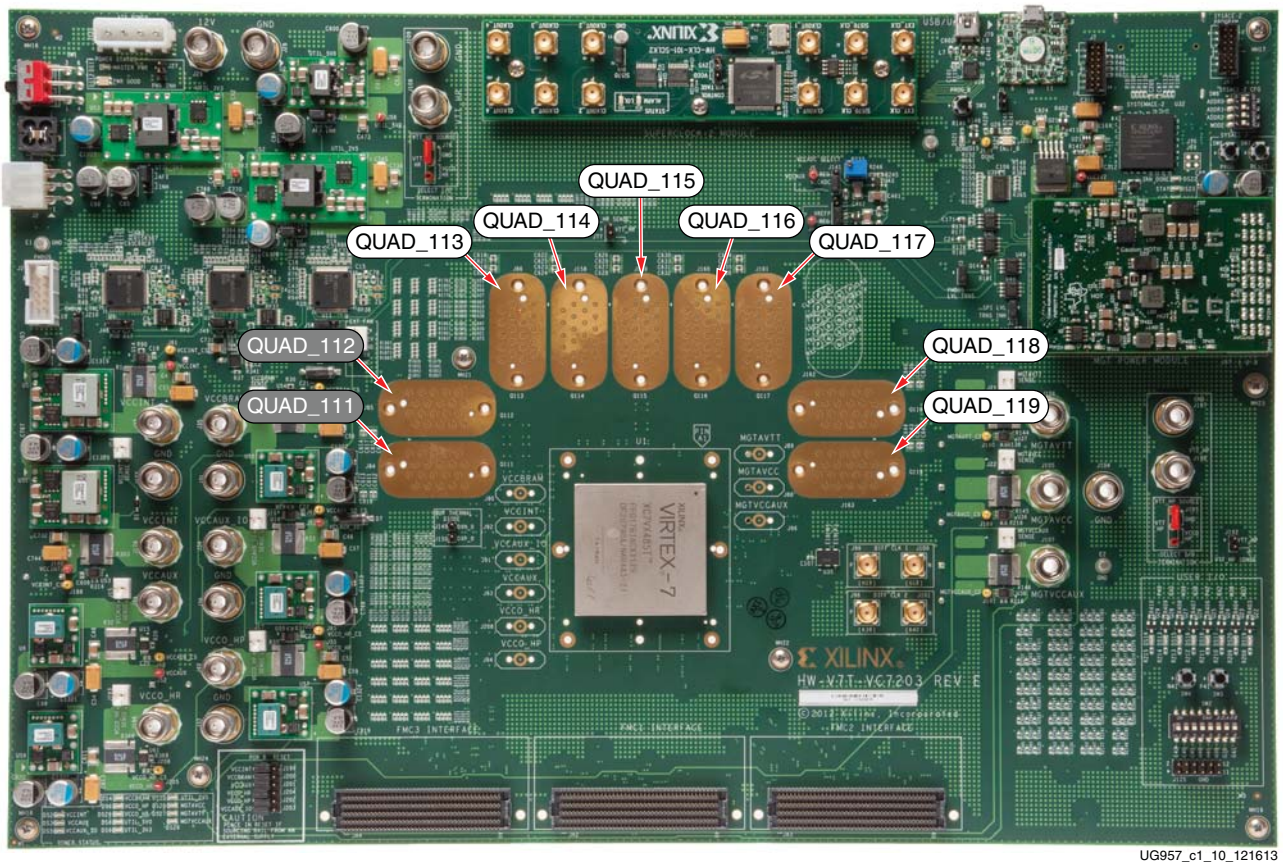


Figure 1-10: **GTX Quad Locations**

Each GTX Quad and its associated reference clocks (CLK0 and CLK1) are brought out to a connector pad which interfaces with Samtec BullsEye connectors used with the Samtec HDR-155805-01-BEYE cable assembly. Contact Samtec, Inc. for information about this or other cable assemblies. Figure 1-11 *A* shows the connector pad. Figure 1-11 *B* shows the connector pinout.

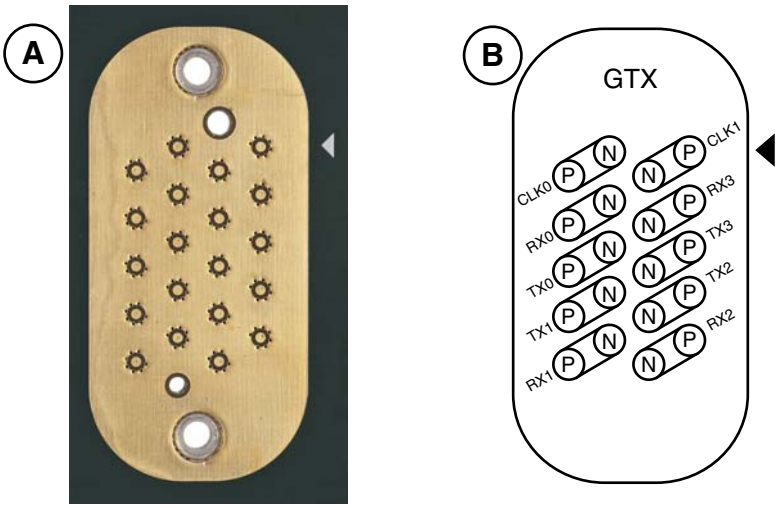


Figure 1-11: **A – GTX Connector Pad. B – GTX Connector Pinout**

Information for each GTX transceiver pin is shown in Table 1-13.

Table 1-13: **GTX Transceiver Pins**

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
BB4	111_TX0_P	111	J84	1,929
BB3	111_TX0_N	111	J84	1,929
BB8	111_RX0_P	111	J84	2,149
BB7	111_RX0_N	111	J84	2,148
BA2	111_TX1_P	111	J84	1,808
BA1	111_TX1_N	111	J84	1,808
BA6	111_RX1_P	111	J84	1,855
BA5	111_RX1_N	111	J84	1,855
AY4	111_TX2_P	111	J84	2,097
AY3	111_TX2_N	111	J84	2,097
AY8	111_RX2_P	111	J84	2,101
AY7	111_RX2_N	111	J84	2,100
AW2	111_TX3_P	111	J84	2,650
AW1	111_TX3_N	111	J84	2,650
AW6	111_RX3_P	111	J84	2,533
AW5	111_RX3_N	111	J84	2,532
AV4	112_TX0_P	112	J85	2,692
AV3	112_TX0_N	112	J85	2,692

Table 1-13: **GTX Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
AV8	112_RX0_P	112	J85	2,996
AV7	112_RX0_N	112	J85	2,996
AU2	112_TX1_P	112	J85	2,511
AU1	112_TX1_N	112	J85	2,511
AU6	112_RX1_P	112	J85	2,546
AU5	112_RX1_N	112	J85	2,545
AT4	112_TX2_P	112	J85	2,785
AT3	112_TX2_N	112	J85	2,785
AR6	112_RX2_P	112	J85	2,803
AR5	112_RX2_N	112	J85	2,803
AR2	112_TX3_P	112	J85	3,385
AR1	112_TX3_N	112	J85	3,385
AP8	112_RX3_P	112	J85	3,365
AP7	112_RX3_N	112	J85	3,365
AP4	113_TX0_P	113	J86	2,949
AP3	113_TX0_N	113	J86	2,949
AN6	113_RX0_P	113	J86	3,243
AN5	113_RX0_N	113	J86	3,243
AN2	113_TX1_P	113	J86	2,736
AN1	113_TX1_N	113	J86	2,736
AM8	113_RX1_P	113	J86	2,822
AM7	113_RX1_N	113	J86	2,822
AM4	113_TX2_P	113	J86	2,736
AM3	113_TX2_N	113	J86	2,736
AL6	113_RX2_P	113	J86	2,455
AL5	113_RX2_N	113	J86	2,455
AL2	113_TX3_P	113	J86	2,812
AL1	113_TX3_N	113	J86	2,812
AJ6	113_RX3_P	113	J86	2,892
AJ5	113_RX3_N	113	J86	2,892
AK4	114_TX0_P	114	J158	2,430
AK3	114_TX0_N	114	J158	2,430

Table 1-13: **GTX Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
AG6	114_RX0_P	114	J158	2,715
AG5	114_RX0_N	114	J158	2,714
AJ2	114_TX1_P	114	J158	2,180
AJ1	114_TX1_N	114	J158	2,180
AF4	114_RX1_P	114	J158	2,181
AF3	114_RX1_N	114	J158	2,181
AH4	114_TX2_P	114	J158	2,207
AH3	114_TX2_N	114	J158	2,207
AE6	114_RX2_P	114	J158	2,160
AE5	114_RX2_N	114	J158	2,160
AG2	114_TX3_P	114	J158	2,570
AG1	114_TX3_N	114	J158	2,571
AD4	114_RX3_P	114	J158	2,570
AD3	114_RX3_N	114	J158	2,570
Y2	115_TX0_P	115	J83	2,805
Y1	115_TX0_N	115	J83	2,806
AA4	115_RX0_P	115	J83	2,898
AA3	115_RX0_N	115	J83	2,898
V2	115_TX1_P	115	J83	2,525
V1	115_TX1_N	115	J83	2,523
Y6	115_RX1_P	115	J83	2,489
Y5	115_RX1_N	115	J83	2,489
U4	115_TX2_P	115	J83	2,549
U3	115_TX2_N	115	J83	2,549
W4	115_RX2_P	115	J83	2,308
W3	115_RX2_N	115	J83	2,309
T2	115_TX3_P	115	J83	2,840
T1	115_TX3_N	115	J83	2,840
V6	115_RX3_P	115	J83	2,933
V5	115_RX3_N	115	J83	2,933
P2	116_TX0_P	116	J84	2,677
P1	116_TX0_N	116	J84	2,677