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Virtex-7 FPGA VC7222 GTH and GTZ Transceiver Characterization Board

User Guide

UG965 (v1.4) February 11, 2015

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/25/2013	1.0	Initial Xilinx release.
01/30/2013	1.0.1	Corrected callout links located throughout the body text back to Table 1-1, page 7. Added answer record link in References, page 61.
07/23/2013	1.1	In Table 1-4, changed nominal voltage to 1.075 V. In Figure 1-3, changed MGTZAVCC and MGTZVCCL voltages to 1.075V. Added a footnote about critical signals to Table 1-20 and Table 1-21. In Appendix C, replaced user constraints file (UCF) with Xilinx Design Constraints (XDC) information. Updated links.
09/20/2013	1.1.1	Updated the *Virtex-7 FPGA VC7222 IBERT Getting Started Guide (Vivado Design Suite)* (UG971) link in Appendix D, Additional Resources.
12/18/2013	1.2	Revised Table 1-7 through Table 1-12, Table 1-18, and Table 1-19. Rearranged rows in Table 1-21. Updated references in Appendix D, Additional Resources. Updated the Declaration of Conformity link in Appendix E, Regulatory and Compliance Information.
08/21/2014	1.3	The number of 7 series GTH power modules from third-party vendors supplied with the VC7222 board changed from four to two. Appendix C was renamed Master Constraints File Listing. Intersil and Lineage vendors were removed from References, page 61.
02/11/2015	1.4	Two power modules are provided with the VC7222 board—Texas Instruments PMP6577 and Bellnix BPE-37 (for 7 Series GTH Transceiver Power Module, page 13 and 7 Series GTZ Transceiver Power Module, page 15. Updated VC7222 Board XDC Listing, page 47.

Table of Contents

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Chapter 1

VC7222 Board Features and Operation

This chapter describes the components, features, and operation of the Virtex®-7 FPGA VC7222 GTH and GTZ Transceiver Characterization Board. The VC7222 board provides the hardware environment for characterizing and evaluating the GTH and GTZ transceivers available on the Virtex-7 XC7VH580T-G2HCG1155E FPGA. The VC7222 board schematic, bill-of-material (BOM), layout files, and reference designs are available online at the Virtex-7 FPGA VC7222 Characterization Kit documentation website.

VC7222 Board Features

- Virtex-7 XC7VH580T-G2HCG1155E FPGA
- Onboard power supplies for all necessary voltages
- Terminal blocks for optional use of external power supplies
- Digilent USB JTAG programming port
- System ACE™ SD controller
- Power module supporting Virtex-7 FPGA GTH transceiver power requirements
- Power module supporting Virtex-7 FPGA GTZ transceiver power requirements
- A fixed, 200 MHz 2.5V LVDS oscillator wired to multi-region clock capable (MRCC) inputs
- Two pairs of differential MRCC inputs with SMA connectors
- SuperClock-2 module supporting multiple frequencies
- Six Samtec BullsEye connector pads for the GTH transceivers and reference clocks
- Two Samtec BullsEye connector pads for the GTZ transceivers and two pairs of SMA connectors for GTZ transceiver reference clocks
- Power status LEDs
- General purpose DIP switches, LEDs, pushbuttons, and test I/O
- Two VITA 57.1 FPGA mezzanine card (FMC) high pin count (HPC) connectors
- USB-to-UART bridge
- I2C bus
- PMBus connectivity to onboard digital power supplies
- Active cooling for the FPGA

The VC7222 board block diagram is shown in Figure 1-1.

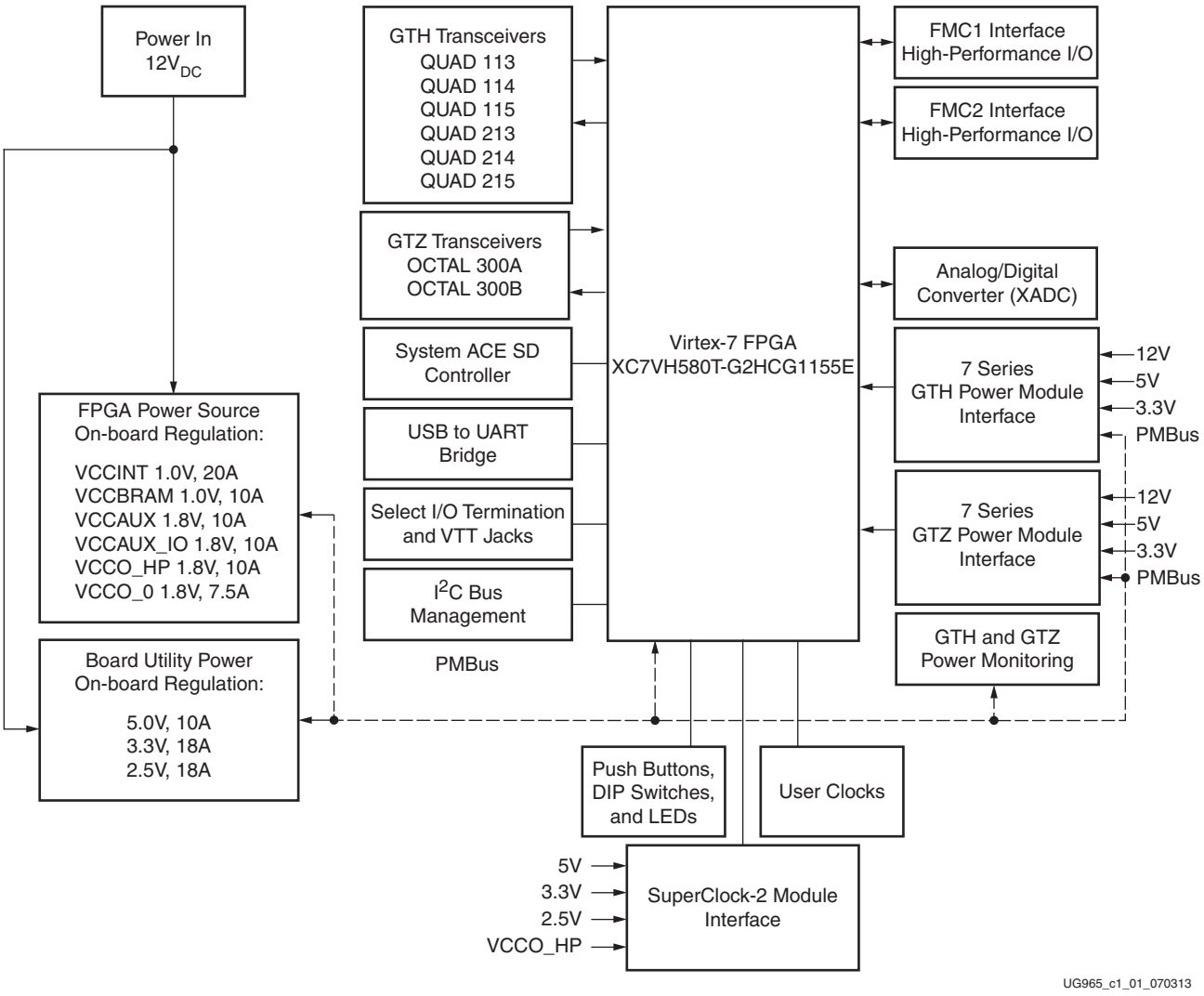

Figure 1-1: **VC7222 Board Block Diagram**

Detailed Description

Figure 1-2 shows the VC7222 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in Table 1-1 and later sections.

The VC7222 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

Caution! Do not remove the rubber feet from the board. The feet provide clearance to prevent short circuits on the back side of the board.

Note: Figure 1-2 is for reference only and might not reflect the current revision of the board.

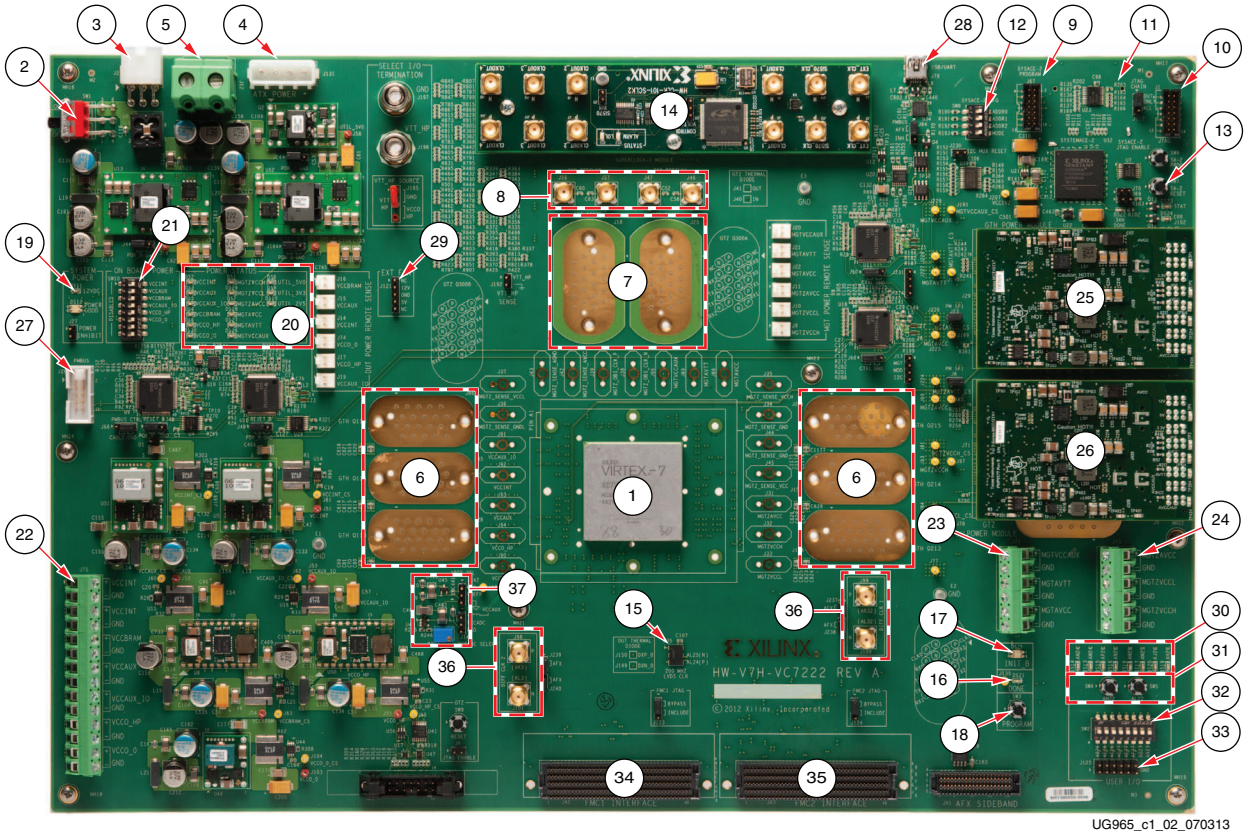

Figure 1-2: **VC7222 Board Features. Callouts Listed in Table 1-1**

Table 1-1: **VC7222 Board Feature Descriptions**

Figure 1-2 Callout	Reference Designator	Feature Description
1	U1	Virtex-7 XC7VH580T-G2HCG1155E FPGA
2	SW1	Power switch
3	J2	12V Mini-Fit connector
4	J131	12V ATX Connector
5	J12	12V Euro-Mag Connector
6	J28, J85, J86, J158, J159, J241	GTH transceiver connector pads Q113, Q114, Q115, Q213, Q214 and Q215
7	J18, J25	GTZ transceiver connector pads O300A and O300B
8	J46, J47, J56, J57	GTZ transceiver reference clock SMAs
9	U57	USB JTAG connector (micro-B receptacle)
10	J1	JTAG connector (alternate access for programming cables)
11	J30	System ACE SD card connector (back-side of board)
12	SW8	System ACE SD configuration address DIP switches

Table 1-1: **VC7222 Board Feature Descriptions *(Cont'd)***

Figure 1-2 Callout	Reference Designator	Feature Description
13	SW7	System ACE SD RESET button
14		SuperClock-2 module
15	U35	200 MHz 2.5V LVDS oscillator
16	DS21	FPGA DONE status LED
17	DS25	FPGA INIT_B status LED
18	SW3	FPGA PROG_B pushbutton
19	DS11	12V power status LED
20	DS1, DS2, DS3, DS4, DS5, DS6, DS7, DS8, DS9, DS10, DS26, DS27, DS28, DS29, DS30	Status LEDS for FPGA logic, transceiver and utility power
21	SW10	Core power regulation enable switches
22	J75	Core power terminal block
23	J72	GTH transceiver power terminal block
24	J73	GTZ transceiver power terminal block
25		GTH transceiver power supply module
26		GTZ transceiver power supply module
27	J26	PMBUS connector
28	J79	Connector for USB to UART bridge (mini-B receptacle)
29	J121	Power connector for active heatsink
30	DS13, DS14, DS15, DS16, DS17, DS18, DS19, DS20	User LEDs (active high)
31	SW4, SW5	User pushbuttons (active high)
32	SW2	User DIP switches (active high)
33	J125	User I/O header
34	JA2	FMC1 connector
35	JA3	FMC2 connector
36	J98, J99, J100, J101	SMA connectors to differential MRCC pins on FPGA
37	J141, J142, R233	Jumpers and potentiometer for XADC reference and analog supply set-up

Power Management

Board 12V Input Power

VC7222 board receives 12V main power through J2 (callout 3, Figure 1-2) using the 12V AC adapter that ships with the board. J2 is a 6-pin (2 x 3), right angle, Mini-Fit connector.

Caution! When supplying 12V through J2, use only the power supply provided for use with this board (Xilinx part number 3800033).

Caution! Do **NOT** use a 6-pin, PC ATX power supply connector with J2. The pinout of the 6-pin, PC ATX connector is not compatible J2 and the board will be damaged if an attempt is made to power it from a PC ATX power supply connector.

12V power can also be provided through:

- Connector J131 which accepts an ATX hard drive, 4-pin, power plug
- Euro-Mag terminal block J12 which can be connected to a bench-top power supply

Caution! Because terminal block J12 provides no reverse polarity protection, use a power supply with a current limit set at 6A max.

Caution! Do **NOT** apply 12V power to more than a single input source. For example, do not apply power to J2 and J131 at the same time.

Power Switch

Main board power is turned on or off using switch SW1 (callout 2, Figure 1-2). When the switch is in the ON position, power is applied to the board and green LED DS11 illuminates (callout 19, Figure 1-2).

Onboard Power Regulation

Figure 1-3 shows the onboard power supply architecture.

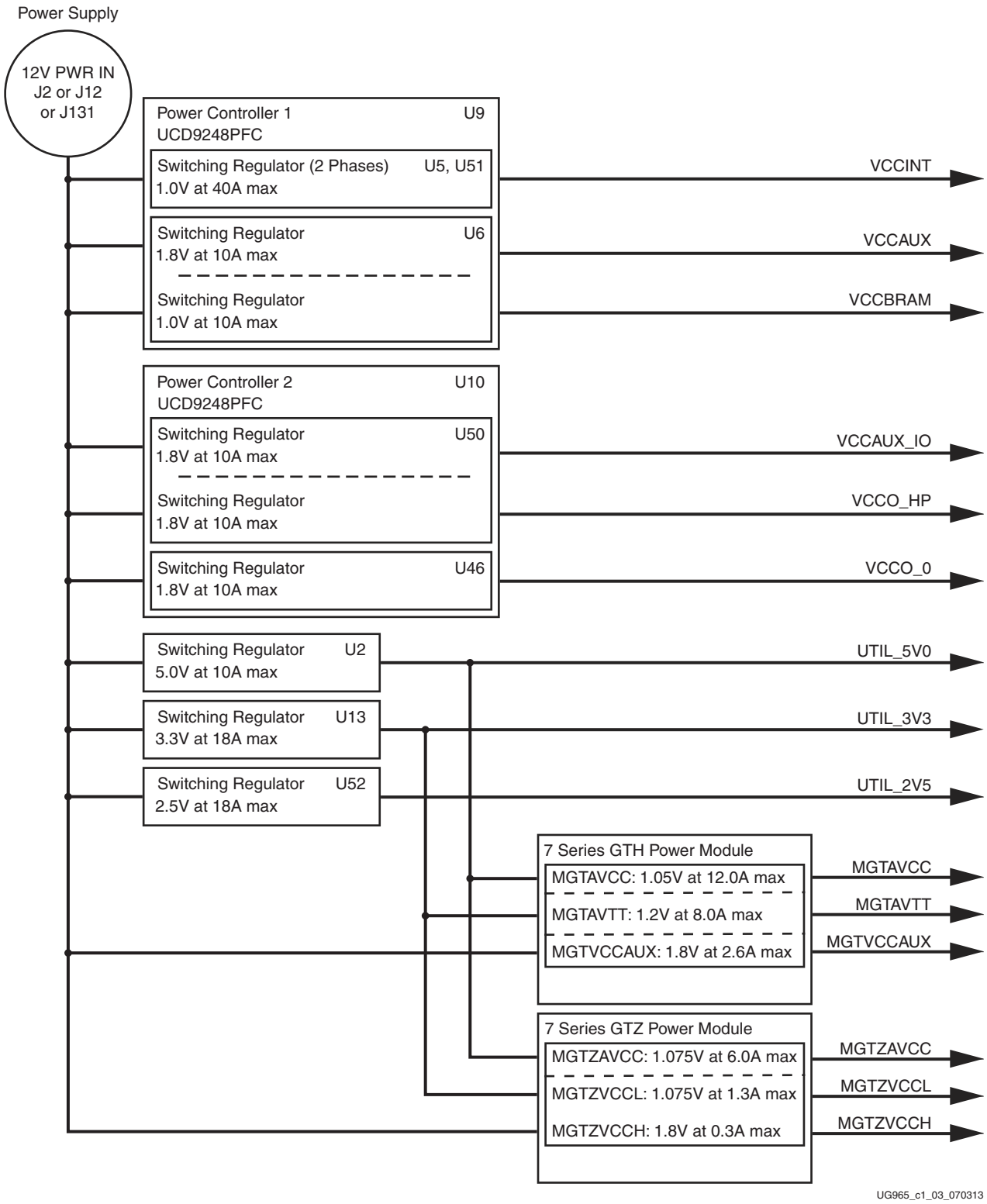

Figure 1-3: **VC7222 Board Power Supply Block Diagram**

The VC7222 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the FPGA logic and utility voltages listed in

Table 1-2. The board can also be configured to use an external bench power supply for each voltage. See Using External Power Sources.

Table 1-2: **Onboard Power System Devices**

Device	Reference Designator(s)	Description	Power Rail Net Name	Voltage
Core Power				
UCD9248PFC	U9	PMBus compliant digital PWM system controller (address = 52)		
PTD08A020W	U5, U51	Adjustable(1) switching regulator, 40A (two phases at 20A/phase), 0.6V to 3.6V	VCCINT	1.0V
PTD08D210W (V_{OUT}A)	U6	Adjustable(1) switching regulator, Dual 10A, 0.6V to 3.6V	VCCAUX	1.8V
PTD08D210W (V_{OUT}B)		Adjustable(1) switching regulator, Dual 10A, 0.6V to 3.6V	VCCBRAM	1.0V
UCD9248PFC	U10	PMBus compliant digital PWM system controller (address = 53)		
PTD08D210W (V_{OUT}A)	U50	Adjustable(1) switching regulator, Dual 10A, 0.6V to 3.6V	VCCAUX_IO	1.8V
PTD08D210W (V_{OUT}B)		Adjustable(1) switching regulator, Dual 10A, 0.6V to 3.6V	VCCO_HP	1.8V
PTD08A006W	U46	Adjustable(1) switching regulator, 10A, 0.6V to 3.6V	VCCO_0	1.8V
GTH Transceivers (monitoring only)				
UCD9248PFC(2)	U11	PMBus compliant digital PWM system controller (address = 54)		
GTZ Transceivers (monitoring only)				
UCD9248PFC(3)	U18	PMBus compliant digital PWM system controller (address = 55)		
Utility				
PTH12060W	U2	Fixed switching regulator, 10A	UTIL_5V0	5.0V
PTH12020W	U13	Fixed switching regulator, 18A	UTIL_3V3	3.3V
PTH12020W	U52	Fixed switching regulator, 18A	UTIL_2V5	2.5V
XADC(4)				
ADP123	U43	Fixed LDO regulator	VCCADC_ADP	1.8V
REF3012	U45	Fixed LDO regulator	VREFP_3012	1.25V
System ACE SD				
ADP123	U21	Fixed LDO Regulator	VCC1V2	1.2V

Notes:

1. The output voltages of regulators controlled by a UCD9248 can be reprogrammed using the Texas Instruments Fusion Digital Power Designer application (www.ti.com/tool/fusion_digital_power_designer). However, **extreme caution must be taken when attempting to modify any of the onboard regulators. An incorrectly programmed regulator can damage onboard components**.
2. The UCD9248PFC (U11) at Address 54 monitors MGTAVCC, MGTAVTT, and MGTVCCAUX rail voltage and current levels which can be observed in real time using the Texas Instruments Fusion Digital Power Designer application (see Monitoring Voltage and Current, page 13). Transceiver supply voltages cannot be changed from this controller.
3. The UCD9248PFC (U18) at Address 55 monitors MGTZAVCC, MGTZVCCL, and MGTZVCCH rail voltage and current levels which can be observed in real time using the Texas Instruments Fusion Digital Power Designer application (see Monitoring Voltage and Current, page 13). Transceiver supply voltages cannot be changed from this controller.
4. For information on XADC see *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 1].

Using External Power Sources

The maximum output current rating for each power regulator is listed in Table 1-2. If a design exceeds this value on any core power rail, power for that rail must be supplied externally through the 14-position core power terminal block J75 shown in Figure 1-4 (callout 22, Figure 1-2) using a supply capable of providing the required current.

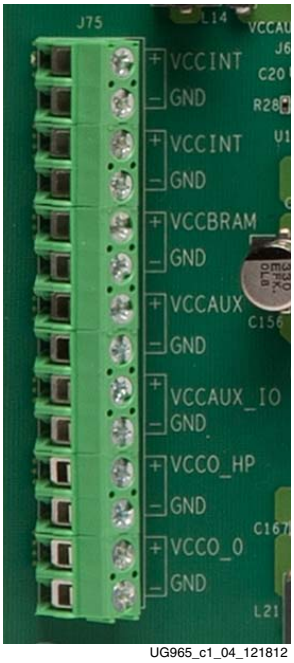

Figure 1-4: **Core Power Terminal Block J75**

Caution! The SW10 power regulator enable switch (callout 21, Figure 1-2) (see Disabling Onboard Power) must be set to the OFF position before turning ON the main power switch (SW1) and applying external power to the corresponding rail input pin on the core power terminal block J75 (callout 22, Figure 1-2).

Caution! The core power terminal block J75 has a maximum load current contact rating of 24A.

Disabling Onboard Power

Each core power regulator can be disabled through the 8-position regulator enable DIP switch, SW10 as shown in Figure 1-5. A switch in the ON position means the rail is supplied by an onboard regulator. Setting a switch in the opposite (OFF) position disables onboard power for that rail. SW10 is shown in Figure 1-2 as callout 21.

Figure 1-5: **Core Power Regulator Enable Switches SW10**

Default Jumper and Switch Positions

A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper and Switch Settings.

Monitoring Voltage and Current

Voltage and current monitoring and control are available for FPGA core and transceiver power rails through Texas Instruments' Fusion Digital Power graphical user interface (GUI). The four onboard TI power controllers (U9 at PMBUS address 52, U10 at PMBUS address 53, U11 at PMBUS address 54, and U18 at PMBUS address 55) are wired to the same PMBus. The PMBus connector, J26 (callout 27, Figure 1-2), is provided for use with the TI USB Interface Adapter PMBus pod and associated TI GUI.

References

More information about the power system components used by the VC7222 board are available from the Texas Instruments digital power website [Ref 2].

7 Series GTH Transceiver Power Module

The 7 series GTH transceiver power module (callout 25, Figure 1-2) supplies MGTAVCC, MGTAVTT and MGTVCCAUX voltages to the FPGA GTH transceivers. Two 7 series GTH power modules from third-party vendors are provided with the VC7222 board for evaluation, Texas Instruments PMP6577 and Bellnix BPE-37. Either of the two GTH modules can be plugged into connectors J29 and J102 in the outlined and labeled power module location shown in Figure 1-6.

Caution! To ensure proper operation, do not plug a GTZ power module into the GTH power module location shown in Figure 1-6. Pay close attention when connecting the GTH or the GTZ power modules to the board. Both power modules have the same mechanical footprint and can be plugged into either the GTH or GTZ board interface.

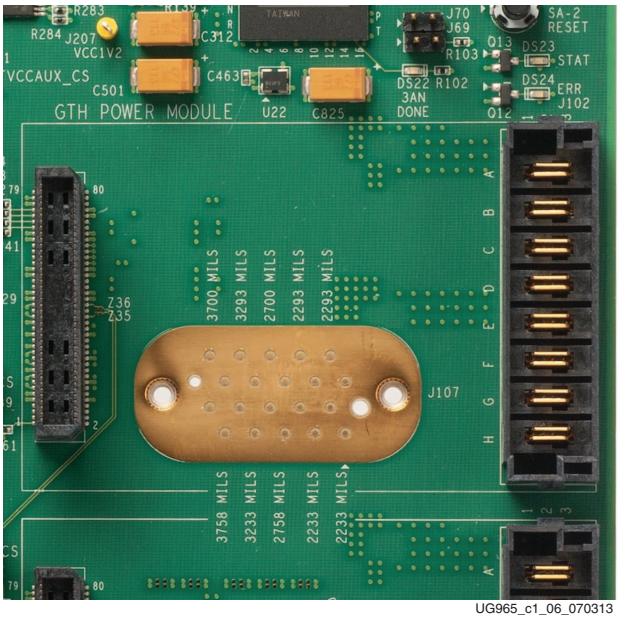

Figure 1-6: **Mounting Location, 7 Series GTH Transceiver Power Module**

Table 1-3 lists the nominal voltage values for the MGTAVCC, MGTAVTT and MGTVCCAUX power rails. It also lists the maximum current rating for each rail supplied by 7 series GTH modules included with the VC7222 board.

Table 1-3: **7 Series GTH Transceiver Power Module**

GTH Transceiver Rail Net Name	Nominal Voltage	Maximum Current Rating
MGTAVCC	1.05V	12A
MGTAVTT	1.2V	8A
MGTVCCAUX	1.8V	2.6A

The GTH transceiver power rails also have corresponding inputs on the GTH transceiver power terminal block J72 as shown in Figure 1-7 to supply each voltage independently from a bench-top power source. J72 is shown in Figure 1-2 as callout 23.

Figure 1-7: **GTH Transceiver Power Terminal Block J72**

Caution! The 7 series GTH module **MUST** be removed when providing external power to the GTH transceiver rails.

Information about the 7 series GTH power supply modules included with the VC7222 Characterization Kit is available from the vendor websites [Ref 3].

7 Series GTZ Transceiver Power Module

The 7 series GTZ transceiver power module (callout 26, Figure 1-2) supplies MGTZAVCC, MGTZVCCL and MGTZVCCH voltages to the FPGA GTZ transceivers. Two 7 series GTZ power modules from third-party vendors are provided with the VC7222 board for evaluation, Texas Instruments PMP6577 and Bellnix BPE-37. Either of the two GTZ modules can be plugged into connectors J5 and J71 in the outlined and labeled power module location shown in Figure 1-8.

Caution! To ensure proper operation, do not plug a GTH power module into the GTZ power module location shown in Figure 1-8. Pay close attention when connecting the GTH or the GTZ power modules to the board. Both power modules have the same mechanical footprint and can be plugged into either the GTH or GTZ board interface.

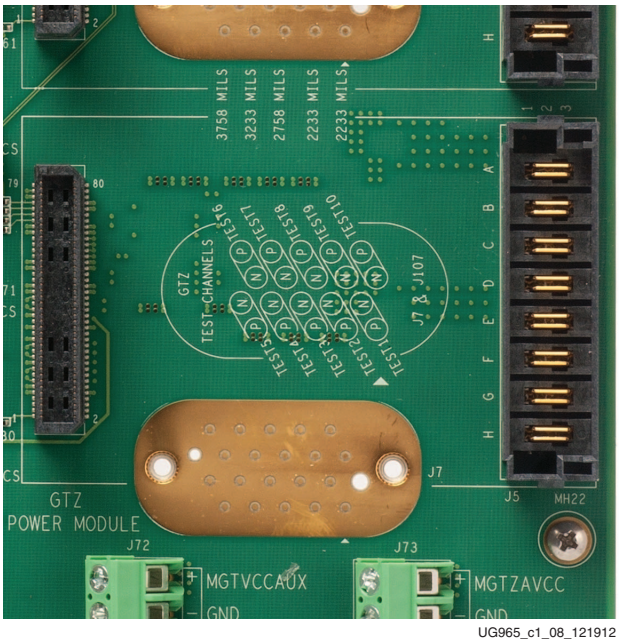

Figure 1-8: **Mounting Location, 7 Series GTZ Transceiver Power Module**

Table 1-4 lists the nominal voltage values for the MGTZAVCC, MGTZVCCL and MGTZVCCH power rails. It also lists the maximum current rating for each rail supplied by 7 series GTZ modules included with the VC7222 board.

Table 1-4: **7 Series GTZ Transceiver Power Module**

GTZ Transceiver Rail Net Name	Nominal Voltage	Maximum Current Rating
MGTZVCC	1.075V	6A
MGTZVCCL	1.075V	1.3A
MGTZVCCH	1.8V	0.300A

The GTZ transceiver power rails also have corresponding inputs on the GTZ transceiver power terminal block J73 as shown in GTZ Transceiver Power Terminal Block J73 Figure 1-9 to supply each voltage independently from a bench-top power source. J73 is shown in Figure 1-2 as callout 24.

Figure 1-9: **GTZ Transceiver Power Terminal Block J73**

Caution! The 7 series GTZ module MUST be removed when providing external power to the GTZ transceiver rails.

Caution! The GTZ transceiver power terminal block J73 has a maximum load current contact rating of 24A.

Information about the two 7 series GTZ power supply modules included with the VC7222 kit is available from the vendor websites [Ref 3].

Active Heat Sink Power Connector

Callout 29, Figure 1-2

An active heat sink (Figure 1-10) is provided for the FPGA. A 12V fan is affixed to the heats ink and is powered from the 3-pin friction lock header J121 (Figure 1-11).

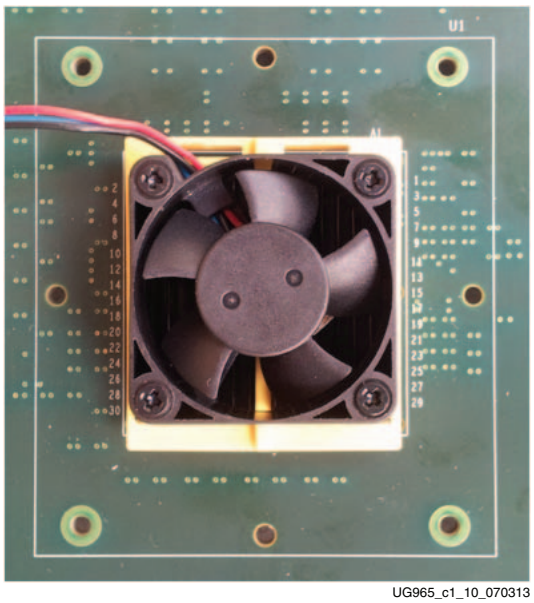

Figure 1-10: **Active FPGA Heatsink**

The fan power connections are detailed in Table 1-5:

Table 1-5: **Fan Power Connections**

Fan Wire	Header Pin
Black	J121.1 - GND
Red	J121.2 - 12V
Blue	J121.3 - NC

Figure 1-11 shows the heats ink fan power connector J121.

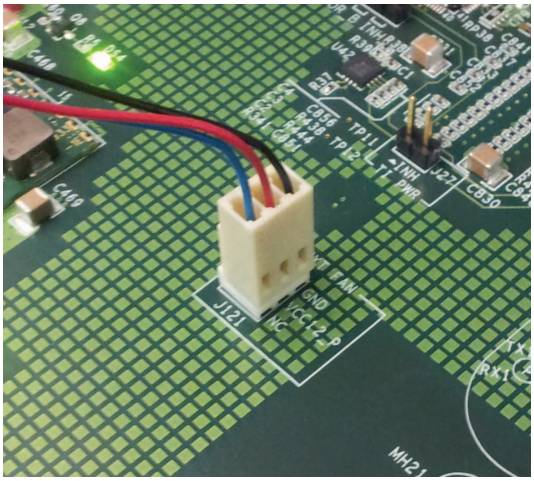

Figure 1-11: **Heatsink Fan Power Connector J121**

Virtex-7 FPGA

The VC7222 board is populated with the Virtex-7 XC7VH580T-G2HCG1155E FPGA at U1 (callout 1, Figure 1-2). For further information on Virtex-7 FPGAs, see *7 Series FPGAs Overview* (DS180) [Ref 5].

FPGA Configuration

The FPGA is configured via JTAG using one of the following options:

- USB JTAG connector (callout 9, Figure 1-2)
- System ACE SD (callout 11, Figure 1-2)
- JTAG cable connector (callout 10, Figure 1-2)

The VC7222 board comes with an embedded USB-to-JTAG configuration module (U57) which allows a host computer to access the board JTAG chain using a standard A to micro-B USB cable. Alternately, the FPGA can be configured via System ACE from a Secure Digital (SD) memory card installed in J30 (see System ACE SD Configuration Address DIP Switches, page 20). Finally, a JTAG connector (J1) is available to provide access to the JTAG chain using one of Xilinx's configuration cables—Platform Cable USB, Platform Cable USB II or Parallel Cable IV (PCIV).

The JTAG chain of the board is illustrated in Figure 1-12. By default only the Virtex-7 FPGA and the System ACE SD controller are part of the chain (J112 jumper OFF). Installing the J112 jumper adds the FMC interfaces as well.

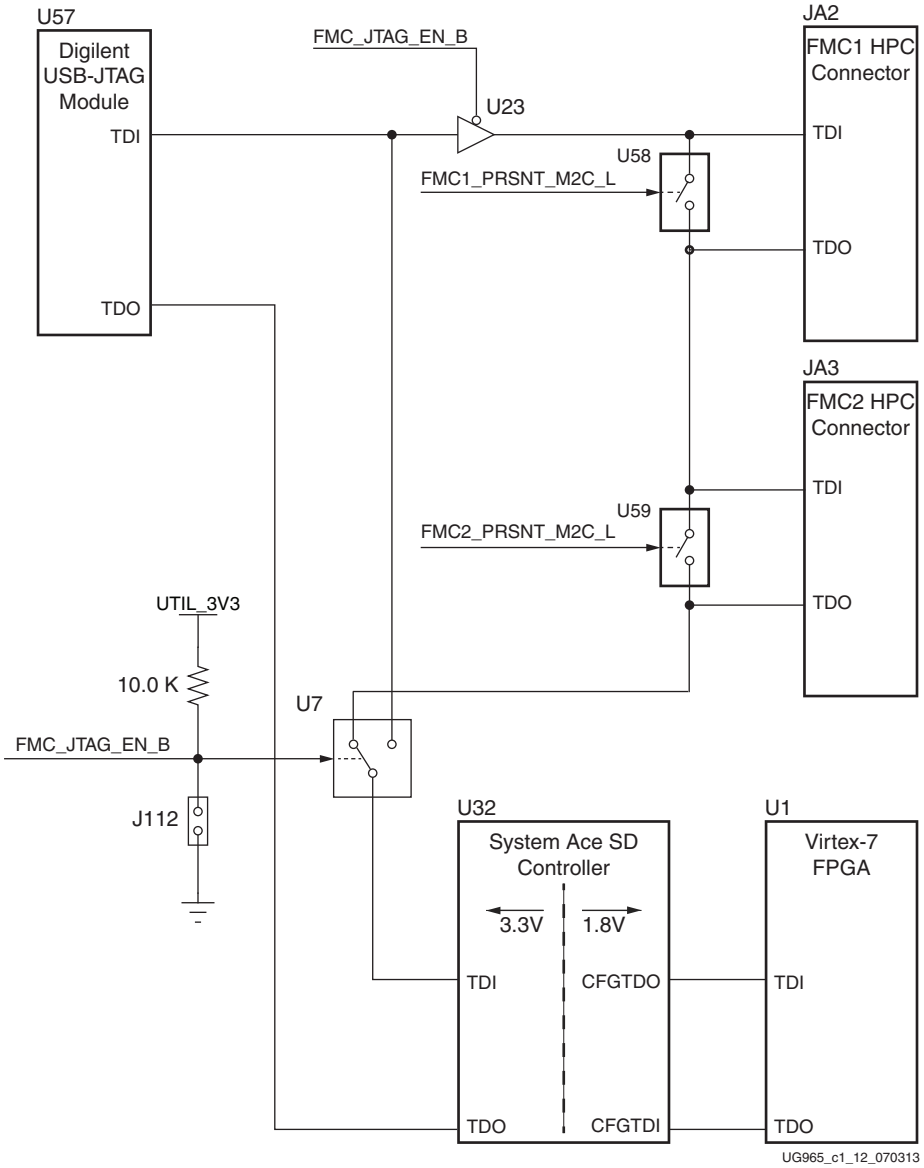

Figure 1-12: **JTAG Chain**

PROG_B Pushbutton

Pressing the PROG pushbutton SW3 (callout 18, Figure 1-2) grounds the active-Low program pin of the FPGA.

DONE LED

The DONE LED DS21 (callout 16, Figure 1-2) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, DS21 lights indicating the FPGA is successfully configured.

INIT LED

The dual-color INIT LED DS25 (callout 17, Figure 1-2) indicates the FPGA initialization status. During FPGA initialization the INIT LED illuminates RED. When FPGA initialization has completed the LED illuminates GREEN.

System ACE SD Controller

The onboard System ACE SD controller U32 allows storage of multiple configuration files on a Secure Digital (SD) card. These configuration files can be used to program the FPGA. The SD card connects to the SD card connector J30 (callout 11, Figure 1-2) located directly below the System ACE SD controller on the back side of the board.

System ACE SD Controller Reset

Pressing the SASD RESET pushbutton SW7 (callout 13, Figure 1-2) resets the System ACE SD controller. The reset pin is an active-Low input.

System ACE SD Configuration Address DIP Switches

DIP switch SW8 shown in Figure 1-13 selects one of the eight configuration bitstream addresses in the SD memory card. A switch is in the ON position if set to the far right and in the OFF position if set to the far left. The MODE bit (switch position 4) is not used and can be set either ON or OFF. SW8 is shown in Figure 1-2 as callout 12.

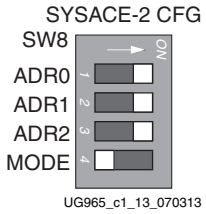

Figure 1-13: **Configuration Address DIP Switch (SW8)**

The switch settings for selecting each address are shown in Table 1-6.

Table 1-6: **SW8 DIP Switch Configuration**

Configuration Bitstream Address	ADR2	ADR1	ADR0
0	ON	ON	ON
1	ON	ON	OFF
2	ON	OFF	ON
3	ON	OFF	OFF
4	OFF	ON	ON
5	OFF	ON	OFF
6	OFF	OFF	ON
7	OFF	OFF	OFF

200 MHz 2.5V LVDS Oscillator

U35 (callout 15, Figure 1-2).

The VC7222 board has one 200 MHz 2.5V LVDS oscillator (U35) connected to multi-region clock capable (MRCC) inputs on the FPGA. Table 1-7 lists the FPGA pin connections to the LVDS oscillator.

Table 1-7: **LVDS Oscillator MRCC Connections**

FPGA (U1)				Schematic Net Name	Device (U35)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
AL24	SYSTEM CLOCK_P	Input	LVDS	LVDS_OSC_P	4	200 MHz LVDS oscillator	Output
AL25	SYSTEM CLOCK_N	Input	LVDS	LVDS_OSC_N	5	201 MHz LVDS oscillator	Output

Differential SMA MRCC Pin Inputs

Callout 36, Figure 1-2.

The VC7222 board provides two pairs of differential SMA transceiver clock inputs that can be used for connecting to an external function generator. The FPGA MRCC pins are connected to the SMA connectors as shown in Table 1-8.

Table 1-8: **Differential SMA Clock Connections**

FPGA (U1)				Schematic Net Name	SMA Connector
Pin	Function	Direction	IOSTANDARD		
AK32	USER CLOCK_1_P	Input	LVDS	CLK_DIFF_1_P	J99
AL32	USER CLOCK_1_N	Input	LVDS	CLK_DIFF_1_N	J100
AK3	USER CLOCK_2_P	Input	LVDS	CLK_DIFF_2_P	J98
AL3	USER CLOCK_2_N	Input	LVDS	CLK_DIFF_2_N	J101

SuperClock-2 Module

Callout 14, Figure 1-2.

The SuperClock-2 module connects to the clock module interface connector (J82) and provides a programmable, low-noise and low-jitter clock source for the VC7222 board. The clock module maps to FPGA I/O by way of 24 control pins, 3 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-9 shows the FPGA I/O mapping for the SuperClock-2 module interface. The VC7222 board also supplies UTIL_5V0, UTIL_3V3, UTIL_2V5 and VCCO_HP input power to the clock module interface.

Table 1-9: **SuperClock-2 FPGA I/O Mapping**

FPGA (U1)				Schematic Net Name	J82 Pin		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
AK8	Clock recovery	Input	LVDS	CM_LVDS1_P	1	Clock recovery	Output
AL8	Clock recovery	Input	LVDS	CM_LVDS1_N	3	Clock recovery	Output
AE6	Clock recovery	Input	LVDS	CM_LVDS2_P	9	Clock recovery	Output
AF5	Clock recovery	Input	LVDS	CM_LVDS2_N	11	Clock recovery	Output
AG1	Clock recovery	Output	LVDS	CM_LVDS3_P	17	Clock recovery	Input
AH1	Clock recovery	Output	LVDS	CM_LVDS3_N	19	Clock recovery	Input
AJ11	Regional clock	Input	LVDS	CM_GCLK_P	25	Global clock	Output
AJ10	Regional clock	Input	LVDS	CM_GCLK_N	27	Global clock	Output
AF8	Control I/O	In/Out	LVCMOS18	CM_CTRL_0	61	NC	-
AH9	Control I/O	In/Out	LVCMOS18	CM_CTRL_1	63	NC	-
AH8	Control I/O	In/Out	LVCMOS18	CM_CTRL_2	65	NC	-
AJ9	Control I/O	Output	LVCMOS18	CM_CTRL_3	67	DEC	Input
AJ8	Control I/O	Output	LVCMOS18	CM_CTRL_4	69	INC	Input
AM10	Control I/O	Output	LVCMOS18	CM_CTRL_5	71	ALIGN	Input
AM9	Control I/O	In/Out	LVCMOS18	CM_CTRL_6	73	NC	-
AF12	Control I/O	In/Out	LVCMOS18	CM_CTRL_7	75	NC	-
AF9	Control I/O	In/Out	LVCMOS18	CM_CTRL_8	77	NC	-
AG9	Control I/O	In/Out	LVCMOS18	CM_CTRL_9	79	LOL	
AG12	Control I/O	Output	LVCMOS18	CM_CTRL_10	81	INT_ALRM	Input
AH12	Control I/O	Output	LVCMOS18	CM_CTRL_11	83	C1B	Input
AP10	Control I/O	Output	LVCMOS18	CM_CTRL_12	85	C2B	Input
AP9	Control I/O	Output	LVCMOS18	CM_CTRL_13	87	C3B	Input
AK12	Control I/O	Output	LVCMOS18	CM_CTRL_14	89	C1A	Input
AL12	Control I/O	Output	LVCMOS18	CM_CTRL_15	91	C2A	Input
AN12	Control I/O	In/Out	LVCMOS18	CM_CTRL_16	93	NC	-
AN11	Control I/O	Output	LVCMOS18	CM_CTRL_17	95	CS0_C3A	Input
AN9	Control I/O	Output	LVCMOS18	CM_CTRL_18	97	CS1_C4A	Input

Table 1-9: **SuperClock-2 FPGA I/O Mapping *(Cont'd)***

FPGA (U1)				Schematic Net Name	J82 Pin		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
AN8	Control I/O	In/Out	LVCMOS18	CM_CTRL_19	99	NC	-
AN13	Control I/O	In/Out	LVCMOS18	CM_CTRL_20	101	NC	-
AP13	Control I/O	In/Out	LVCMOS18	CM_CTRL_21	103	NC	-
AM12	Control I/O	In/Out	LVCMOS18	CM_CTRL_22	105	NC	-
AM11	Control I/O	In/Out	LVCMOS18	CM_CTRL_23	107	NC	-
AE8	CM_RESET	Output	LVCMOS18	CM_RST	66	RESET_B	Input

User LEDs (Active High)

Callout 30, Figure 1-2.

DS13 through DS20 are eight active-High LEDs that are connected to user I/O pins on the FPGA as shown in Table 1-10 These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-10: **User LEDs**

FPGA (U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	IOSTANDARD		
AH26	User LED	Output	LVCMOS18	APP_LED1	DS19
AJ26	User LED	Output	LVCMOS18	APP_LED2	DS20
AM25	User LED	Output	LVCMOS18	APP_LED3	DS17
AM26	User LED	Output	LVCMOS18	APP_LED4	DS18
AN26	User LED	Output	LVCMOS18	APP_LED5	DS16
AP26	User LED	Output	LVCMOS18	APP_LED6	DS15
AM24	User LED	Output	LVCMOS18	APP_LED7	DS13
AN24	User LED	Output	LVCMOS18	APP_LED8	DS14

User DIP Switches (Active High) and I/O Header

Callout 32, Figure 1-2.

The DIP switch SW2 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-11. These pins can be used to set control pins or any other purpose determined by the user. Six of the eight I/Os also map to 2 x 6 test header J125 providing external access for these pins (callout 33, Figure 1-2.).

Table 1-11: **User DIP Switches**

FPGA (U1)				Schematic Net Name	SW2 DIP Switch Pin	J125 Test Header Pin
Pin	Function	Direction	IOSTANDARD			
AD26	User switch	Input	LVCMOS18	USER_SW1	1	2
AE26	User switch	Input	LVCMOS18	USER_SW2	2	4
AC26	User switch	Input	LVCMOS18	USER_SW3	3	6
AC27	User switch	Input	LVCMOS18	USER_SW4	4	8
AE27	User switch	Input	LVCMOS18	USER_SW5	5	10
AF27	User switch	Input	LVCMOS18	USER_SW6	6	12
AG27	User switch	Input	LVCMOS18	USER_SW7	7	-
AH27	User switch	Input	LVCMOS18	USER_SW8	8	-

Figure 1-14 Shows the user test I/O connector J125 (Callout 26, Figure 1-2).

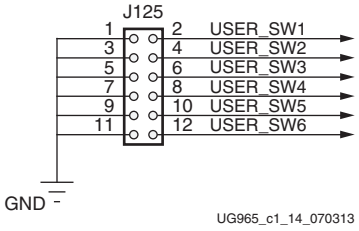

Figure 1-14: **User Test I/O**

User Pushbuttons (Active High)

Callout 31, Figure 1-2.

SW4 and SW5 are active-High user pushbuttons that are connected to user I/O pins on the FPGA as shown in Table 1-12. These switches can be used for any purpose determined by the user.

Table 1-12: **User Pushbuttons**

FPGA (U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	IOSTANDARD		
AL22	User pushbutton	Input	LVCMOS18	USER_PB1	SW5
AM22	User pushbutton	Input	LVCMOS18	USER_PB2	SW4

GTH Transceivers and Reference Clocks

Callout 6, Figure 1-2.

The VC7222 board provides access to all GTH transceiver and reference clock pins on the FPGA as shown in Figure 1-15. The GTH transceivers are grouped into six sets of four RX-TX *lanes*. Four lanes are referred to as a *Quad*.

Note: Figure 1-15 is for reference only and might not reflect the current revision of the board.

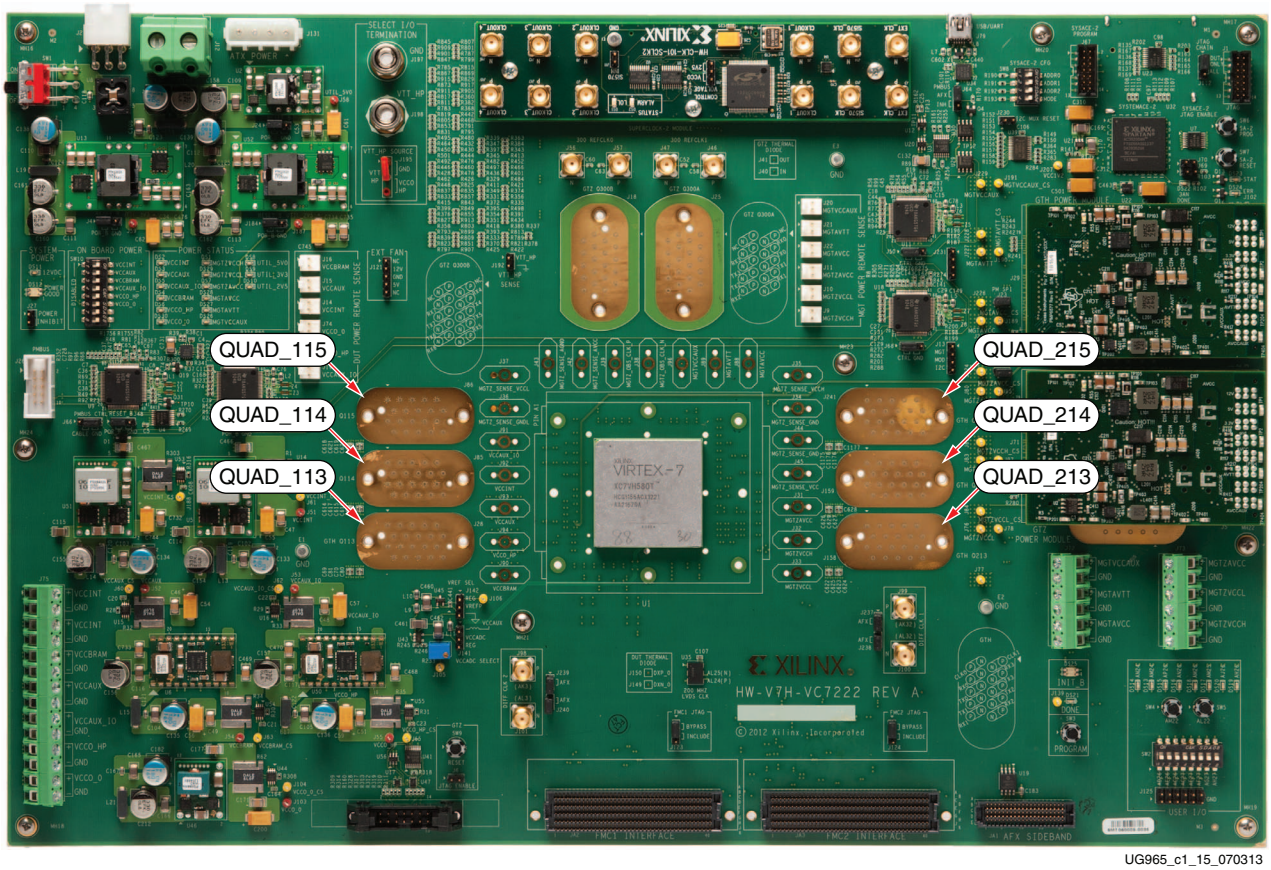

Figure 1-15: **GTH Quad Locations**